International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 07 Issue: 05 | May 2020 www.irjet.net p-ISSN: 2395-0072

Signal Integrity Issues in Digital System Design

B M Uday Prakash[1], Nagesh M[2], Sampath Kumar Reddy[3], Manoj Kumar D A[4], Prof. Pavan Kumar E[5]

[1-5]*Department of Electronics and Communication, Sai Vidya Institute of Technology, Bengaluru, India*

Abstract - *As far as today circuits or design is concerned most of them are digital even though they are also susceptible to signal integrity issues but when it comes to speed and performance they play a vital role. As the number of active element (transistors) increases there by following Moore's law, the signal integrity issues becomes a major issue that the designer or the researcher should look into.*

These signal integrity issues that occur in any digital circuits are interchannel crosstalks,reflection etc. while some signal integrity issues are electromagnetic compatibility due to which there may be delay distortion leading to dispersion in the transmitted signals.

In this paper we firstly have started with history of signal integrity followed by the SI analysis and principle and the paper also deals about various SI issues that normally occur and lastly we have concluded the use of various simulation tools in order to detect and overcome those signal integrity issues so that circuit and layout designers can accurately run their high speed systems with compatible buffer.

Key Words: **Signal Integrity (SI), Printed Circuit Board (PCB), Integrated Circuit(IC), Programmable Logic Device (PLD), Application Specific Integrated Circuit (ASIC), Electromagnetic (EM), Input/output Buffer Information Specification (IBIS)**

1. INTRODUCTION

A Signal basically convey some data/information in the form electric signal hence they are a strong function of time .It may be a time varying electromagnetic wave carrying information. These signals are usually analog and digital in nature. An analog signal is a continuous time varying signal, such as an audio signal or speech signal. But the disadvantage is that they are highly subjected to electronic noise and distortion in a medium, there by the SNR gradually Reduces. Thereby it will be difficult for signal analyzers to find out these degradation in analog signal. Their shape

Changes continuously with respect to time there by making difficult to process them, as they move from point A to point B the noise power keeps on increasing while signal power keeps on reducing. At a point the SNR becomes equal to 1 where in both signal power and noise power becomes equal there by the elimination of noise becomes a critical task. Where exactly digital signals are constructed with only 1s and 0s and contains a sequence of discrete values, they also get affected by noise but the process such as truncation and rounding off makes it easier to eliminate the noise as shown in fig 1.

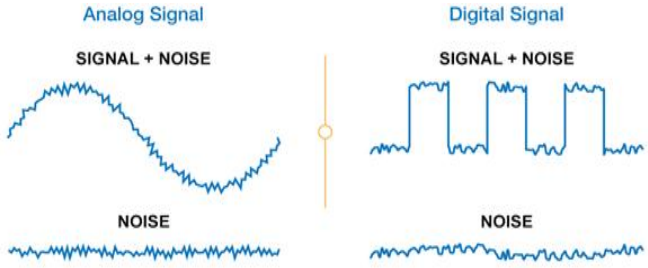

Fig-1: Noise content in signals

However by now we may know that signal integrity issues such as noise distortion, crosstalk occurs in both analog and digital .In some of the case analog to digital convertors are used to convert analog signal into digital signal via sampling, quantization and etc. In the present generation all our processors /controllers which we are using are high speed thus the circuit designer must play a vital role in reducing the signal integrity issues.

The signal integrity mainly deals with two characteristics of the signal.1) timing 2) quality of signal. Of course signals are transmitted But a question arise whether the signal at receiving end is same quality as that of transmitted one? And whether it has been received at right time or is there some delay?

There by because of this issues the performance and overall functionality of system starts degrading. The signal integrity issues analysis helps in a fast and complete efficient transmission of data.

Some major signal integrity issues addressed are:

1. Crosstalk: a signal transmitted on one track or channel has some undesired effect on other channel signal.
2. Distortion: these are some changes that in turn change the original signal pattern.
3. Reflection noise: it mainly occurs due to impedance mismatch due to imperfection in the medium /channel.

In case of a digital system where information is transmitted in terms of logic 1 referred as 5v in analog and logic 0 referred as 0v in analog .certain reference voltage levels are considered at the input if it is above the reference level (Vih) it is considered as logic high and if it falls below (Vil) then it is termed as logic low, as shown in Fig: 2

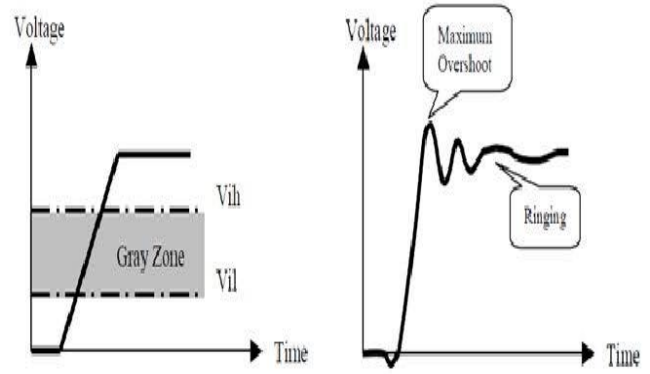

Fig-2: Digital Representation and the Shape of signal [1]

In case of an analog data the receiving gate must perform sampling and obtain binary coded information. This is done by triggering at rising edge or at falling edge of the clock, the data must be in a stable state when the gates starts to latch in. if any delay experienced in data, will result in failure of data transmission as shown in Fig :3

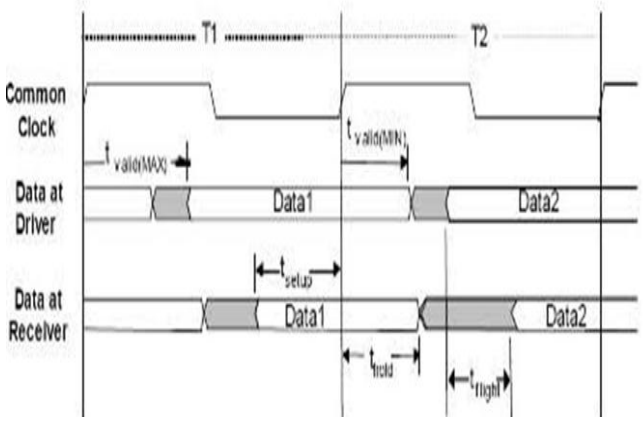

Fig-3: Sampling Process of a signal [1]

Thus everything depends on timing and also the physical shape of signal.the simulation tools are used to detect these issues and correct them.

2. SIGNAL INTEGRITY ANALYSIS

As far as PCB concepts is concerned , signal basically is termed as the changing between low and high logic levels hence they consume some time while changing hence the term real signals. When taken an consideration of a signal propagating from source to destination on a PCB where in both source and destination lie on different IC as shown in Fig: 4. Then any change in signal must propagate from the source driver, through the bond wire, package lead frame and pin of the source IC, along the PCB trace, through the pin, lead frame and bond wire of destination IC and into the receiver, while propagating through this path there is a chance that noise gets added and signal gets distorted. That's the reason in many core of embedded systems such as PLD's, off the shelf components there is no control over the path.

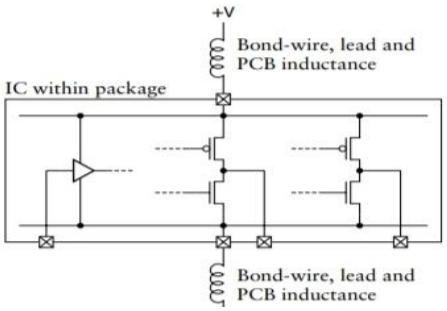

Fig-4: Propagation of Signals [1]

It is a basic thing that a change in signal values causes a change in the current flowing through the PCB trace, due to this there is a change in EM field around trace, likewise if distinct signals within a parallel bus are connected along paths of different lengths, change in elements of the bus, may not arrive concurrently thereby there is an incorrect sampling at the receiver.

In this era of technology we are always connected all the time through various high speed digital computational systems.

This SI issue will be a vital factor to guarantee the reliable operation of these systems. Fig: 5 shows the SI design flow which has been tightly integrated into each design st

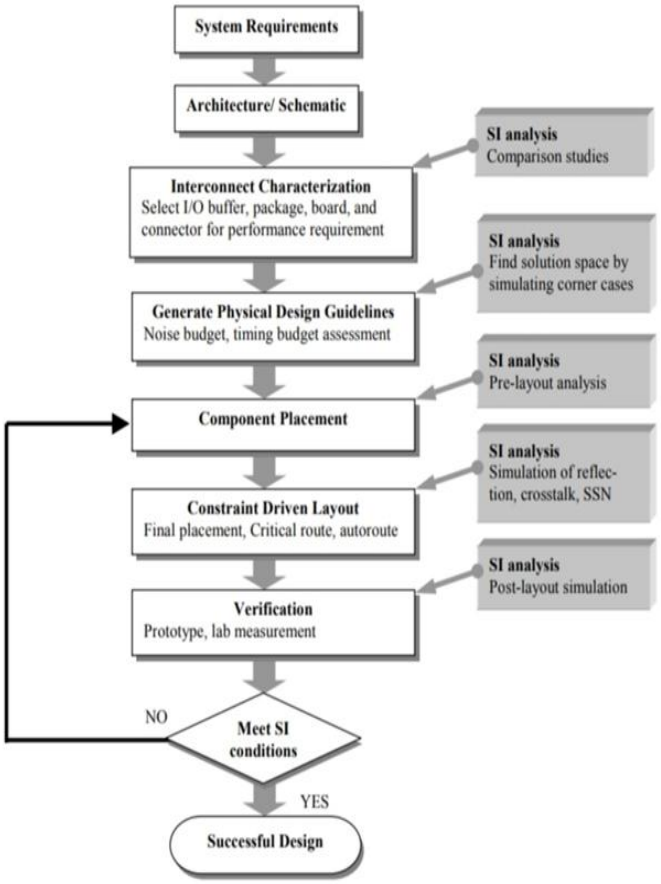

Fig-5: Design Flow

The first is the pre route stage, where the SI can be used to select technology for the pin assignment, nets, topologies, with all designs. With various design parameters taken into account, the SI simulations on different corners will formulate a set of optimized guidelines for physical design of later stage. The SI analysis at this stage is also called constraint driven SI signal. It mainly ensures the SI of physical layout, which follows the routing constraints for noise and timing budget, will not exceed the maximum allowable noise levels.

Thus an in-depth pre route SI analysis will cut down the redesign Operations and routing operations thereby reducing design cycle.

The past route SI analysis checks the extent of correctness of the SI design and constraint obtained. It checks if there are SI violations present in the design such as reflection noise, ringing, crosstalk and ground bounce. It may also look into SI problems that were overlooked in the pre route stage, because post route mainly deals with physical layout data rather than models thus producing more accurate simulation results.

In the design process of any complex PCB /circuits, the physical design is generated by layout engineers. With the trend for high speed systems and chips increasing day by day, the system engineers are getting involved in SI by employing various guidelines and constraints. But these systems engineers are not able to give solutions to all SI problems because their each design team will have specialized SI engineers who carries out all electrical characterization and also develop layout guidelines by running SI simulation software's which must be sensitive enough to model individual interconnections. The SI engineers will generate a set of design rules which will generate a set of design rules which will be for warded to layout and design engineers must employ these set of rules generated by SI engineers and then perform their actual task. Once the layout designer is ready with the placement/routing plan with employed SI rules they must generate a physical design based on this along with a report of any violations / SI issues found in a system using SI tools.

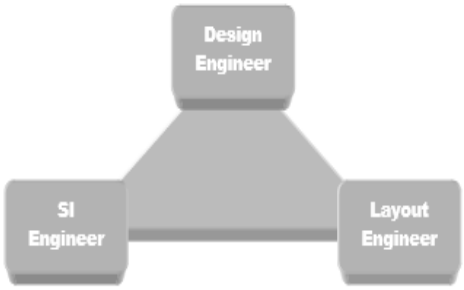

Fig-6: Design Team [1]

3. SIGNAL INTEGRITY PRINCIPLE:

In a digital system SI analysis are done in three levels is logic. Circuit theory and EM fields. In these 3 level the logic level is the highest priority, where SI issues can be easily identified. EM field is the low level priority. Where other levels are built upon. In most of the SI problem are EM field, such as reflection, crosstalk and ground bounce etc.

Circuit theory is based on only interconnect modeling.

As compared to circuits analysis EM is more accurate because in a EM fields occurs a wave propagation, reflection coupling and resonance will occur in the circuit package during the signal transaction. EM wave analysis is more accurate than the circuit analysis, where circuit analysis obtain a good SI solutions at low frequency. The mainly SI analysis is carried out in circuit simulators are SPICE, for nodal analysis, and solve voltage and current in the RLC circuit. In SI issues

signal rise time is a very important and also transmission line theory is also important in the EM fields.

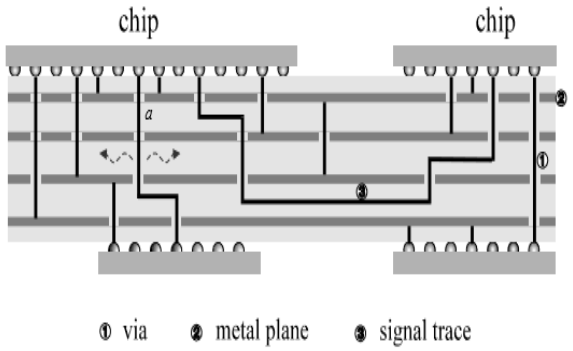

Fig-7: Interconnections and Signal flow in a Package [1]

4. SI ISSUES IN DIGITAL SYSTEM:

4.1 Rise Time and SI

Living in an era of Nano technology today there is a wide scope of improvement in the chip fabrication technology due to which the channel length of transistors are scaled into sub-micron range, thereby incorporating billions of transistors on a single chip. Hence these logic operate at a much higher speed. Their rise time and fall time are on the order of hundreds of picoseconds. Since most of SI issues are timing related (DV/DT) and (DI/DT) hence phenomena such as crosstalk, power ground switching, ringing, jitter becomes even more worsen. Systems with high clock frequency have shorter rise time. Therefore will have more SI challenges. A 20MHz operated system will get some SI issues that a 200MHz system gets, when some modern logic with fast rise time is used.

4.2 Transmission lines, Reflection, Cross talk:

In any chip packages or PCB's, a trace with its reference plans forms a transmission line. There can also be sandwiched between two metal planes. Another type of transmission lines can be a pair of parallel conducting wires spaced uniformly in a cable or a pair of metal planes with a wire attached.

These transmission lines forms the base which through which the signals will be propagating. These lines are basically characterized by certain features such as resistance(R), capacitance(C), inductors(L), conductance(G), delay, impedance which can be analytically obtained in case of a parallel plate transmission line while in other types of lines usually we need a empirical formulas , 2D electromagnetic field analysis.

Another after recurring issue is the reflection which falls under the transmission effects. In a high speed time critical digital systems even the smallest of the tracks suffers from these effects. This effects of reflection causes delay, ringing. The cause for reflection is the impedance mismatch phenomena as the signal changes its impedances keeps on varying in terms of (manufacturing variations, design considerations) making a field for reflection to occur. Even when the load impedance, reflection occurs. Since any signal propagating is mainly associated with two fields 1].the magnetic field due to current 2].the electric field due to voltage when they experience impedance mismatch, it creates a room for reflection to occur.

Any high speed systems are powered by wide number of transmission lines running parallel resulting in electromagnetic cross coupling there by causing cross talk effects. That goes on to affect the signal in an adjacent track. It can occur in micro sized circuits within computers and audio equipment to Nano sized circuits within a system.

In case of switching of lines simultaneously from low to high and vice versa it may impact the timing. Thus the cross talk is directly related with the rise time, spacing between the lines and how long these lines run parallel to each other.

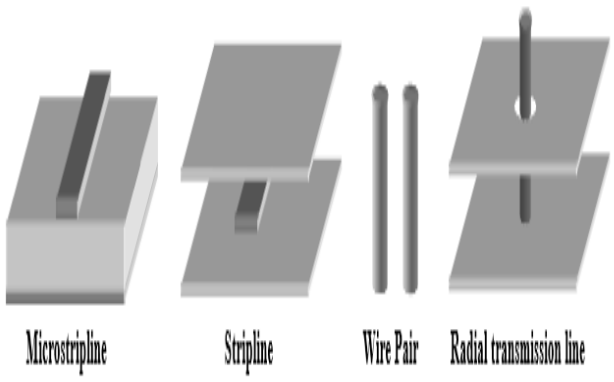

Fig-8: Transmission Line [1]

4.3 Power/Ground Noise:

Power ground noise is one of the most difficult Electromagnetic effect to be modeled in SI analysis because of complexity of the power/ground noise. Mainly in chip packaging and printed circuits board power/ground noise planes are formed from power distribution network. Switching simultaneously can cause voltage fluctuation between power and ground planes. That's the reason they occupy 30% of noise in any high speed digital system.

Switching simultaneous noise (SSN) or power/ground noise or delta-I noise will slow down the signal due to the imperfect return path and it will also cause logical error disturbs the data in the latch.

The power/ground plains are distributed circuits the physical behavior of SSN is an EM problem in nature. To perfectly simulate SSN we have to consider certain parameters are:-

1] Wave propagation

2] Edge radiation

3] Via coupling

4] Package resonance

The effective inductor modeling which is valid only at low frequency limit shown Fig (a).

The wire antenna model shown in Fig (b) which calculate the current in conducting wires by the method of moments.

The popular 2D capacitor/inductor mesh model has been used in circuit similar to model power/ground planes by many companies as shown in Fig (c).

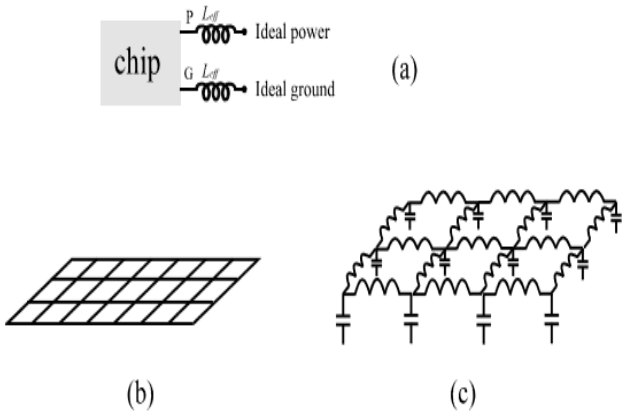

Fig-9: Modellings in Power/Ground Noise

4.4 Jitter:

Jitter is a non desirable characteristics in a high speed digital system domain the main characteristics of jitter are a critical challenge in the high speed system assign. Jitter is a deviation of a digital signal in a ideal position. The jitter can be measured in terms of timing jitter and amplitude jitter.

The main fundamental components of a jitter are deterministic jitter and random jitter.

The deterministic jitter causes due to EM interference, crosstalk and grounding problems the jitter mainly classified as amplitude jitter and phase jitter. The variations in amplitude is called amplitude jitter. The variation in timing is called phase jitter.

SI TOOLS SOLVERS:

Simulation tools having an advantage and disadvantage. Simulation tools are having a graphical input.
For a simulation tools what can be expected from a good tool are:-
1] Comfortable initiative input of the circuit.
2] Correct error messages.
3] Robust execution of the simulation.
4] Support from the manufacturer etc..
Some examples of simulation tools are:- PSpice, mat lab, saber, CASPOC, PSIM, IBIS etc.
Any simulation tool mainly contains the 2D field solvers for extracting resistance, inductance, capacitance and conductance of single # parallel transmission lines and also 3D field solvers for modeling of receivers and drivers these SI tools takes physical layout as input data, and simulation results in time domain and frequency domain.

4.5 IBIS over SPICE:

Although SPICE simulations are very accurate, but when it comes to transient simulation analysis it is very slow. An alternative to SPICE is IBIS. INTEL manufactured IBIS to allow customers access to accurate buffers. The core of the IBIS has all the information predefined in the form of a look up table. This attracts the vendors of the IC's as all the inbuilt transistor level information is not revealed and is represented as like a black box.

SIMULATIONS IN IBIS:

The Input/output Buffer Information Specification (IBIS) is a standard used to describe the analog behavior of the Input/output of any Integrated Circuit (IC). With the light of IBIS, simulation tool sellers can perfectly fit agreeable buffers in SI simulations.

Up gradation of chip and package design has resulted in the need for new models for integrated circuit drivers and receivers. These tools are capable of maintaining suitable veracity and speed in the simulation of transmission lines and SI related effects such as crosstalk and power and ground bounce (noise). Simulation of digital I/O buffers and PCB's,

can be done in either the traditional approach which makes use of transistor level models, which is useful when small-scale simulations or analysis of some minor particular part of network is the target of the simulation. At the same time this approach would be very time consuming for simulations of large number of buffers and their interconnections. To overcome this drawback, behavioral models such as I/O Buffer Information Specification (IBIS) are introduced. The data required for this model can be obtained from circuit simulations. Simulations with behavioral models can be executed faster than that of the transistor level models.

IBIS thus not only helps in faster simulation speed that can be used to reduce the delays but also helps in the elimination of non-convergence. IBIS does not reveals any sensitive information about the design technology and the background fabrication processes, thereby helps the intellectual property to be protected.

The IBIS based behavioral model provides the DC current vs. voltage characteristics along with all timing related information (rise time and fall time) of the driver output voltage and packaging data of the I/O buffer. IBIS behavioral model presentation of a device as shown in Fig:10 provides information about the I/V characteristics of the power and ground clamp diodes of the buffer, the input /output die capacitance (Ccomp) and the attributes of the package (the values of lead inductance , resistance and capacitance.

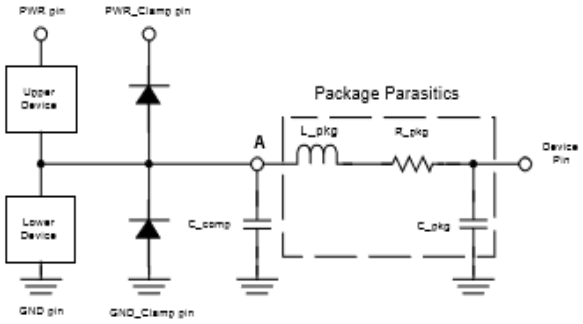

Fig-10: Behavioral Model

Tool Kit for Interactive Network Analysis (TINA), a SPICE-based electronic design software supports IBIS 4.2 version. Here not only it converts IBIS models to macros that can be used in any circuits but also to describe the analog behavior in a much better way.

A concept of correcting and fixing SI issue between a TEXAS device TMS320C6748 DSP and an ADS1259 delta-sigma ADC is depicted with all procedures-
1. Select the model to be imported
2. Then select the model PBFZP18LL_X50_PI and Typ value set.
3. Conversion from IBIS to SPICE macro takes place shown in Fig 11.

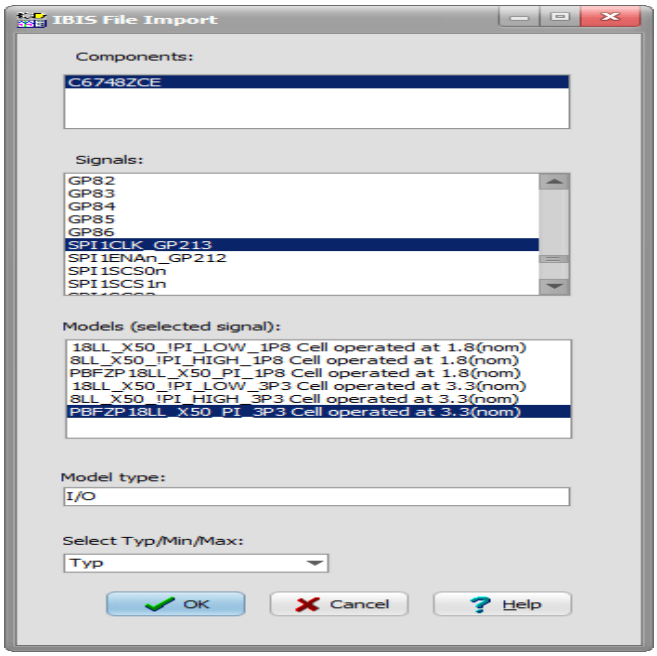

Fig-11: Import module for conversion

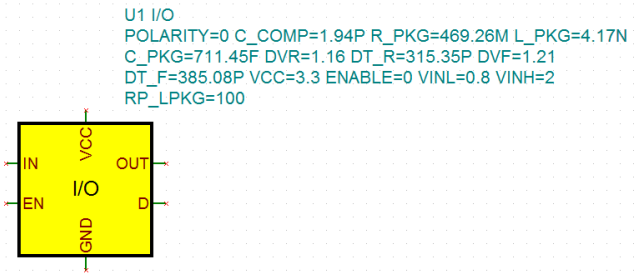

Fig-12: Converted model

4. SPI1CLK_GP213 is the clock signal for dsp kit to drive clock input of an AD convertor, TEXAS device ADS1259.

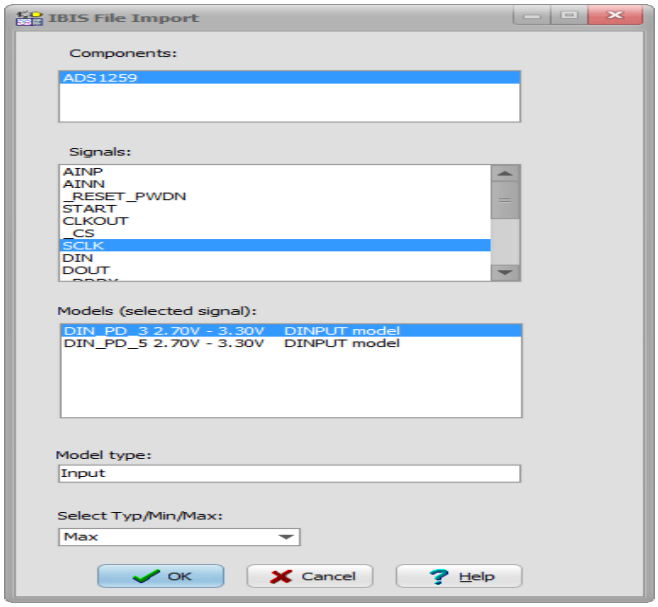

Fig-13: Clock Signal Selection

5. Connect the DSP output buffer to input of ADC via a transmission line. Required power source and voltage generator create clock signal shown in Fig 14.

6. Adjust the line parameters to a few inches of micro strip trace routed on a PCB, producing 500ps delay and 90ohms impedance.

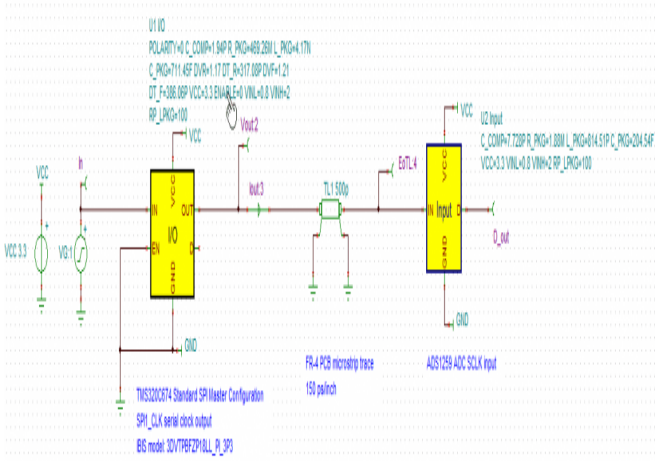

Fig-14: Interconnections

7. on clicking Analysis Transient: The DSP transmits the clock signal where the impedance mismatch create reflections.

8. Thus at the ADC side (pin EoTL), the voltage is beyond the ground and the supply voltage there by violating the predefined maximum rating of the digital input.

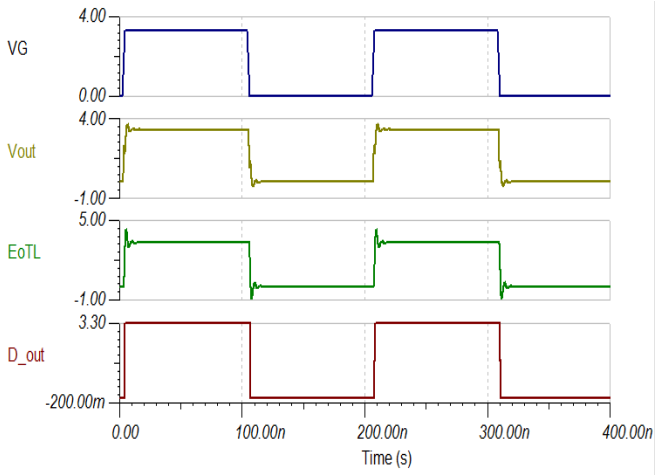

Fig-15: Before Simulation

9. To avoid these overshoots match the impedance of output to that of the trace impedance by inserting a resistor between the output and the trace as shown in Fig 16.

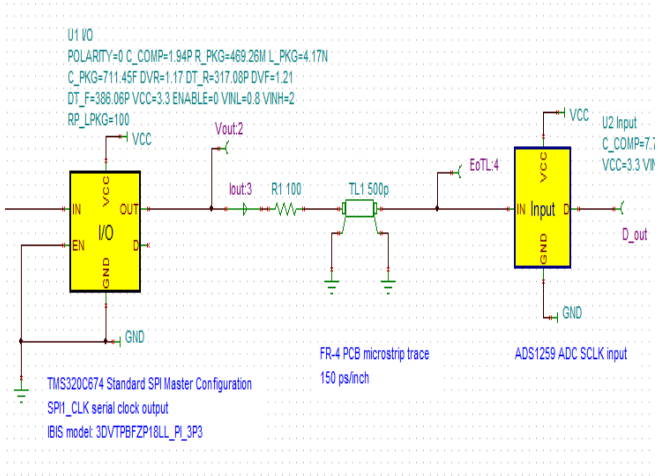

Fig-16: Circuit modification

10. Run the transient and compare the results.

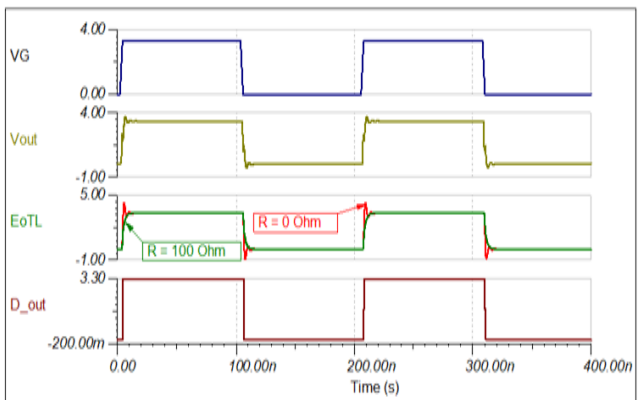

Fig-17: Simulated Output

Thus IBIS models helps us to deal with critical issues in any simulation.

CONCLUSION AND FUTUREWORK:

In this paper IBIS simulation tools is proposed to reduce the signal integrity issues. Starting with concepts of SI and issues that degrades our performance of the system to the SI tools to overcome and analyze these issues. Not only IBIS but wide number of tools produced from various company that can stimulate any high speed digital systems. Designers can also accompany electromagnetic band gap structure for the reduction of the signal integrity.

ACKNOWLEDGMENT:

We would like to thank our college Sai Vidya Institute of Technology affiliated to VTU, Belgavi, approved by AICTE, New Delhi for giving us a opportunity to publish this paper and make it successful.

REFERENCES:

[1]https://www.csee.umbc.edu/csee/research/vlsi/reports/si_chapter.pdf

[2] Tai-Yu Chou, "Signal Integrity Analysis in ASIC Design", ASIC & EDA, pp.70-81, May 1994.

[3] Rob Kelley, "Choosing the Right Signal Integrity Tool", Electronic Design, pp. 78-80, September 1995.

[4] Lisa Maliniak, "Signal Analysis: A Must For PCB Design Success", Electronic Design, pp. 69-81, September 1995.

[5] Andrew F. Peterson, "Computer-Aided Engineering Tools for Electronic Packaging Analysis", IEEE Topical Meeting on Electrical Performance of Electronic Packaging, Short Course, October 1996.

[6] M. Bedouani, "High Density Integrated Circuit Design: Simultaneous Switching Ground/Power Noises Calculation for Pin Grid Array Packages," 43rd Electronic Components & Technology Conference, Conference Proceedings, pp. 1039-1044, June 1-4, 1993, Orlando, FL., USA.

[7] Ying Wang and Han Ngee Tan, "The Development of Analog SPICE Behavioral Model Based on IBIS Model", Proceedings of the Ninth Great Lakes Symposium on VLSI, March, 1999.

[9] W. Hobbs, A. Muranyi, R. Rosenbaum and D. Telian, Intel Corporation, "IBIS: I/O buffer Information Specification Overview", http://www.vhdl.org, January 14, 1994.

[10]Digital Design-An Embedded System Approach Using VERILOG by Peter J.Ashenden