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Implementation of Universal Reversible Logic Gate using Mentor Graphics Tools

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Abstract - *: Reversible logic is becoming one of the best effective emerging design technology having its application in low power CMOS, quantum computing, cryptography and nano technology [1].Conventional circuits are irreversible in nature and dissipates power for each bit loss in circuit[2].It can be reduced by inverse property of reversible logic gates, all the input vectors can be retrieved from output vectors[3].Reversible logic gives zero amount of heat dissipation[5].Reversible computation plays an crucial role in low power circuit design and efficient energy recycling[4].This paper proposes a reversible design of 4x4 URL(Universal Reversible logic) gate implemented using mentor graphics tool with 130nm technology, operated at threshold voltage of 1V. Here we calculated the power dissipation and delay for URL gate. This gate includes XOR, NAND, and NOR logical operations, employed in applications like ATPG, fault detection, BIST, Various logic circuit implementations etc.*

***Key Words*: Reversible logic gates, power dissipation, ATPG, fault detection.**

1. INTRODUCTION

In modern VLSI design, power dissipation is the critical limiting factor for more complex circuits. According to the Landauer's principle, every conventional combinational circuits dissipates KTln2 Joules of energy for one bit loss of data, where K is Boltzmann's constant and T is absolute temperature[1].R.Landauer's presented high technique circuitries and systems formulated through irreversible hardware will result in dissipation of energy because of loss of data[9]. Reversible logic has received great attention in the recent years due to their ability to scale back the power dissipation which is the main requirement in low power VLSI design [6].Reversible logic circuits have theoretically zero internal power dissipation as they do not loose information [2].The circuit operates in a backward direction, allows reproducing the inputs from the outputs and consume zero power [1]. It realizes the network cascade of given reversible gates and ensure that cost is low, where fan out and feedback are not permitted [7].

A reversible gate is an n-bit function that maps each possible input vector to a unique output vector[1].According to Bennett no energy would dissipate from a system if it might be ready to return to its initial state from its final state[3].The important challenges of designing reversible circuits are to lower the number of gates, garbage outputs, delay and quantum cost. Any reversible circuit should be designed with minimum number of reversible logic gates. They provide cost effective solution to the exponentially increasing needs of industrial electronics. A basic structure of reversible gate is shown in Fig1.

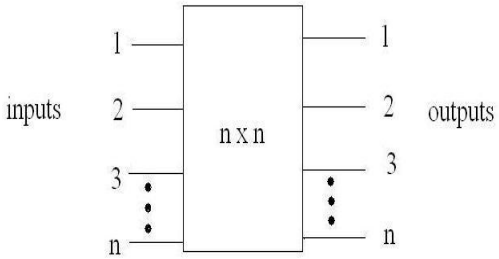

Fig1: Basic structure of reversible Logic gate

Characteristics:

1. A reversible gate must have equal number of input and output vectors i.e., 2x2,3x3…….n x n.

2. For every input pattern, there must be a unique output pattern.

3. Each output must be used once.

4. Loops and feedbacks are forbid in reversible designing.

2. REVERSIBLE LOGIC GATES

A reversible gate is a memory-less logic element that realizes an injective logic function. Here we investigate basic properties of reversible logic gates and circuits, which are needed in the further discussion. Reducing the whole amount of garbage signals is an crucial problem in designing reversible logic circuits [8].According to reversible networks no fan out and no feedback constraint condition and limitation, reversible logic synthesis is to use reversible logic gate given to implement the relevant reversible logic network meanwhile make the price as low as possible. Reversible logic gate cascade is one of the key issue of the reversible logic synthesis[10].

Constant input: This refer to the input, which is maintained as constant at either 0 or 1 so as to achieve appropriate logic function[1].

Garbage output: The output of the gate, which is not given as a input of another gate is referred as garbage output. For better performance, number of garbage outputs must be minimum [1].

Quantum cost: This refers to the cost of the circuit in terms of cost of primitive gates i.e., the quantity of primitive gates like 1x1 and 2x2 required for the realization of a reversible gates/circuits[1].

Some of the most popular reversible logic gates which are implemented previously are Fredkin gate, Feynman gate, Peres gate, Toffoli gate, TR gate.

3. UNIVERSAL REVERSIBLE LOGIC GATE

URL gate is a 4X4 reversible logic gate shown in Fig 2.The input vectors are I(A,B,C,D) and output vectors are Q(P,Q,R,S).The outputs are defined as P=A, Q=A⊕B, R=(BC)', S=(C+D)'.

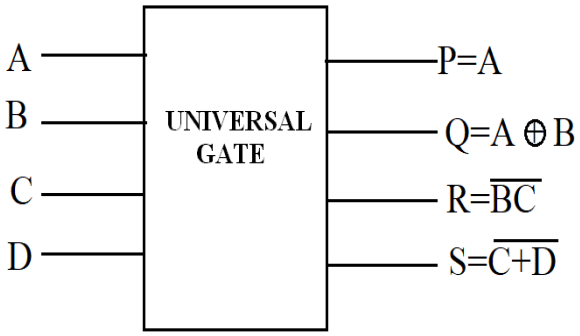

Fig 2: URL gate includes NAND, NOR, XOR gates.

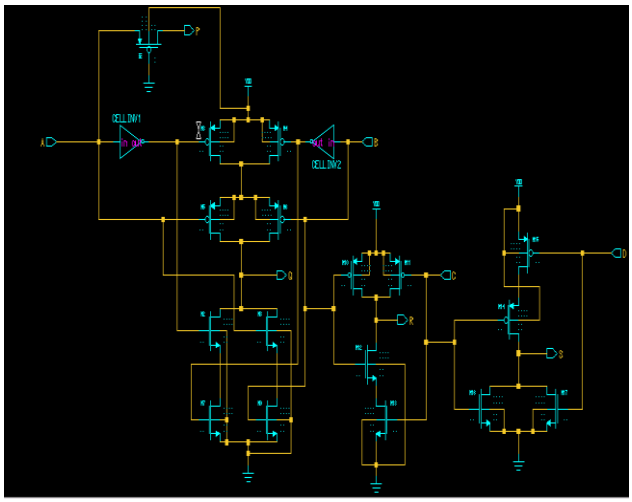

Fig 2(a): CMOS realization of URL gate

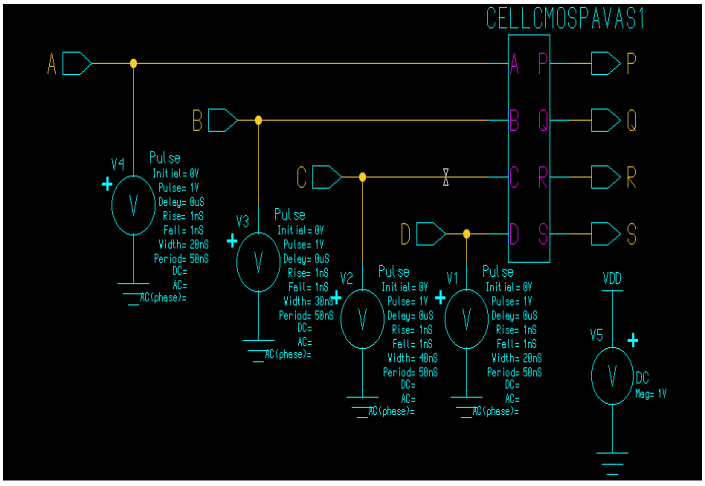

Fig 2(b): Symbol representation of URL gate

SIMULATION RESULTS:

Here the URL reversible gate are simulated by using mentor graphics tool with 130nm technology, operated at threshold voltage of 1V.We computed the parameters like total power dissipation, delay for the logical operations.

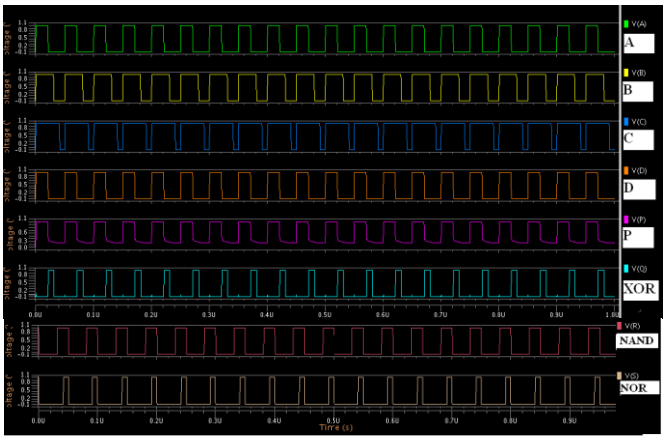

Fig 2(c): simulation results of URL gate

Table-1: Simulation Result Observation

S.No.	Reversible gate	Power dissipation	Delay
1.	URL gate	5.2076 NWATTS	P=A=28.831NS Q=28.831 NS R=35.894 NS S=31.056 NS

4. APPLICATIONS:

Reversible computing may have applications in computer security and transactions processing, but the most future benefits will be felt very well in those areas which require high energy efficiency, speed and performance, it includes areas like:

- Low power CMOS.
- Quantum computing.
- Nano technology.
- Optical computing.
- Built in self-test.
- ATPG.

5. CONCLUSION

The reversible circuits form the fundamental building blocks of quantum computers. This paper presents the primitive reversible gate which is implemented with CMOS realization using Mentor Graphics 130nm Technology and helps researchers/designers in designing higher complex computing circuits using this URL reversible gate. Also we calculated the various parameters which has total power dissipation and delay, which proves that this URL Gate is giving better results compared to conventional CMOS logic Gates.

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BIOGRAPHIES

K.Venkateswarlu received M.Tech (VLSI) from VNRVJIET affiliated to JNTUH in 2009. He has published several conference and journal papers. His research interests include Low Power and Ultra Low Power Static Random Access Memory (SRAM) design, Low Power and Energy Efficient logic design, reliable and fault tolerant static and dynamic CMOS circuit and system design, and VLSI implementation of digital systems.

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