International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 07 Issue: 05 | May 2020 www.irjet.net p-ISSN: 2395-0072

GNRFET DESIGN OF N-BIT TERNARY ALU

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Abstract-*The Intend of three valued logic gates is essential for advancing the performance in provisions of static power dynamic power and time delay. The designing of digital circuits are usually performed on only two logic values in binary format, although by taking one more logic value, Multiple Valued Logic (MVL) is developed for gates GNRFET circuits can give high performance, consumes low energy and equivalent consistency at related operating points to scale CMOS circuits that is high vulnerable to defects and variations. So, GNRFET circuits are favoured in nanoelectronics. The TNAND and TNOR are basic logic gates that are to be executed first to understand the working and performance of GNRFET based ternary logic gates. Afterwards, half adder and multiplier are designed using these gates. The simulation, arithmetic circuit designs and the performance parameters such as power and delay are observed by using Synopsys HSPICE tool. These results are used for implementation.*

1. INTRODUCTION

In general three valued computer systems are known as ternary logic systems. This is a group of systems called MVL (Multi Valued Logic). This project involves the design of simple ternary logic gates and their implementations – a half adder and a multiplier. Rise in VLSI technology these days is attributed to the reduced size of transistors.. Integrated circuits that use technology CMOS (Complementary Metal – Oxide – Semiconductor) have begun to lose their reputation due to scaling beyond 32 nm. This has contributed to the development of a variety of emerging technologies. Graphene Nano-Ribbon Field Effect Transistor - GNRFET is one such technology Basic ternary logic gates and arithmetic circuits were designed and implemented using CMOS and GNRFETs within this project. All these circuits are simulated using the Synopsys HSPICE method and parameters such as dynamic and static control, propagation delay to compare the results of CMOS and GNRFET circuits were calculated[1][4]

The goal of this project is to develop ternary logic gates using GNRFETs. Due to the availability of various efficient tools, binary logic was widely utilized. Although this is real, it is also a fact that with the rapid advancement of technology and inventions these days, it will be beneficial to have a multi-value logic system that has a different level – 'maybe' apart fromBoth rates - yes and no. For binary logic architecture, the ternary logic system is the alternative with simplicity and energy efficiency, which play a vital role in the architecture of modern digital devices with the decrease in transistor size, CMOS transistors have increasing numbers of disadvantages. It is therefore desirable to use another form of transistor available, such as GNRFET[1]. The design of ternary logic gates is usually carried out using 32 nm of scaled technology to create the circuits that work at a minimum Voltage which consumes very little power in comparison with devices designed with other technologies. These simulations are carried out on the Synopsys HSPICE System. We equate the output of ternary logic gates and arithmetic circuits based on the CMOS and GNRFET.

1.1 MOTIVATION

The big downside of graphene is that it lacks band gap. Researchers give Diamond, graphite, graphene, nanotubes, and fullerenes in different forms of carbon allotropes. Graphene is ordered on a honeycomb lattice a two-dimensional substance with one atom-thick structure. Wonderful Graphene Electronics properties consider it an alternative silicon candidate in electronic devices such as field-effect transistors, tunnel barriers and quantum dots. Planar graphene structure due to processing with more traditional complementary metal oxide semiconductor (CMOS) technology gives it a significant advantage over carbon nanotubes (CNTs). Three ways to open graphene band gaps:use of graphenenano-ribbon, bilayer graphene, and add graphene strain. Graphenenano-ribbon will open up to 400meV of bandgap. In this paper we design the circuit using graphenenano-ribbon FETs. Armchair-edge (AGNRs) and zigzag-edge (ZGNRs) are the two graphenenano-ribbon types as shown in the figure 2 AGNRs are considered to be the semiconductor and their electrical properties depend on the width of the string, whereas ZGNRs are metallic and magnetic. AGNR was thus used for the wireless circuits. Single-layer graphene lattice consists of regular hexagons at each corner, with a carbon atom. A GNR (W_{ch}) width is defined as:

$$W_{ch}=(N-1)\text{sqrt}(3)d_{cc}/2$$

Where N represents the dimer line numbers as shown in Figure 1, N is the number of dimer lines in the direction of the armchair and dcc=0.144 nm is the length of the carbon-carbon bond. The electronic properties of the

nano-ribbon armchair differ depending on the number of atoms at the bottom. Type AGNR N= 3P+1 and N=3P are semiconductors while Type AGNR N=3P+2 is metallic[2]

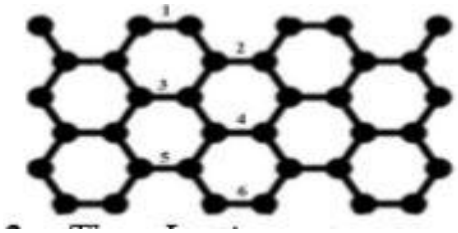

Fig 1: The Lattice structure of an armchair GNR with N=6

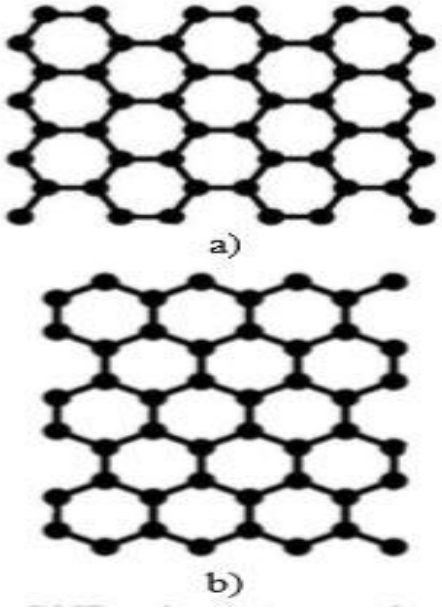

Fig 2: GNR-edge a. armchairedge,b.zigzagedge

Graphenenano-ribbon has the bandgap, depending on the width of the nano-ribbon. The GNRFETs SPICE compatible circuit model was used for the simulations of the circuits. GNRFET could be a promising tool for the design of multi-valued logic (MVL) voltagemode circuits. More than two levels of logic are specified in the multiple-evaluated logic depending on the number of levels, ternary (level=3) or quaternary (level=4) logic styles. The complicated method could be done quicker and with fewer steps of computation. MVL designs reduce the size of big chips and overcome the CMOS technology problem. In the binary logic many complex applications like estimation, analysis procedures decision systems and process control are not feasible. Moreover, the entire dissipation of power can be reduced by converting a concept from the binary to the ternary or quaternary families. Raychowdary et al. made use of CNTFET and resistors to construct a ternary logic gate. The resistors were removed by Lin et al. using active CNTFETs. In a dynamic structure was proposed to incorporate a dynamic ternary logic based on the complete model technique Moaiyeri et al. developed CNTFET-based quaternary maximum (Q_{Max}) and minimum (Q_{Min}) circuits. They found that their designs give the effect of process variations a very high robustness. CNTFET-based quaternary full adders have been developed by Moaiyeri et al. They showed that this proposed design decreases average demand and static power consumption considerably. Kim et al. performed ternary graphene field effect transistors (TGFET) and p-type TGFET experimentally to demonstrate ternary inverter circuits. Their results, at room temperature, indicate three distinct current states in one unit. The multi-valued logic circuits can be implemented by one or more than one voltages of the power supply. Increasing the number of power supply sources will also lead to uncertainty in interconnections, reduced electricity usage and higher production costs. For multi-valued logic circuits we use one source of power supply. The law of stress division is then applied to generate different voltages for different logic values[3]

2. GRAPHENE NANO RIBBON FIELD EFFECT TRANSISTOR

Graphene is an ideal material to build up nano electronic devices because of their electrical and physical properties. Graphene has a great usage in manufacture of flexible electronic applications because of its thin and robust lattice. When Graphene Nano Ribbons Field Effect Transistor (GNRFET) fabrication method is observed, the compatibility and integrability of GNRFETs with the existing Si technology came to light. The major advantage in the Schotky barrier type known as 'SB-GNRFET' is that – it does not need any doping material in its terminals or its channel. Hence, it reduces the technical complexity in fabrication and eliminates the need for doping variation. Modeling and simulations through computer are helpful in providing physical insights into GNRFETs and in analyzing the performance of futuristic GNRFET based circuits. Thin robust and planar lattice structure of graphene makes it easy, manageable and measurable for large manufacturing and integrating with attained CMOS technology fabrication.[5]

For this reason, graphene is a material used to manufacture easily adjustable and transparent electronics. The 2D graphene is a semi-metal without a band gap. The gap between two bands can be obtained by using narrow graphene Nano-Ribbon (GNR). Recent experiments show that all sub-10 nm GNR are semiconducting due to the edge effect which will fetch for more electronic device applications.

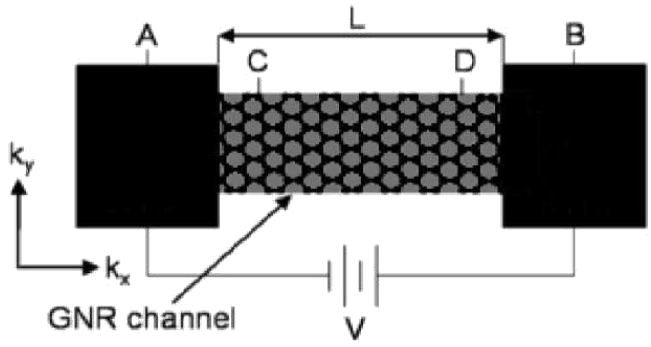

Fig 3:GNRFET-channel

GNRFET is Graphene Nano Ribbon Field Effect Transistor which can be condensed to GNRs, are segments of graphene with ultra-fragile broadness. Graphene Ribbons were introduced as theoretical model by Mitsutaka Fujita and co-authors to examine the edge and nano-scale size effect in Graphene. A Graphene Nano ribbon Field-Effect Transistor denotes a FET that either requires only one graphene sheet or a collection of graphene sheets as the channel material rather than a bulk of silicon in the conventional MOSFET structure. In the year 2004, there have been major progresses in GNRFETs which promised to be an alternative material to substitute to the future silicon electronics. The graphene offers a higher conductance when compared with Cu for interconnects in the devices at anometers range. The properties which are obtained from the graphene interconnects are: higher carrier mobility at normal temperature, thermal conductivity, greater mechanical strength, decreased capacitance coupling between the adjacent wires, width- dependent transport gap, temperature coefficient, and ballistic transport. When line widths of the graphenenano ribbons are decreased less than 8 nm, the resistivity of GNR's is negligible. On top of that, the usage of graphene in the interconnects improves the life of high-performance devices then the silicon-based integrated circuit technology.[5]

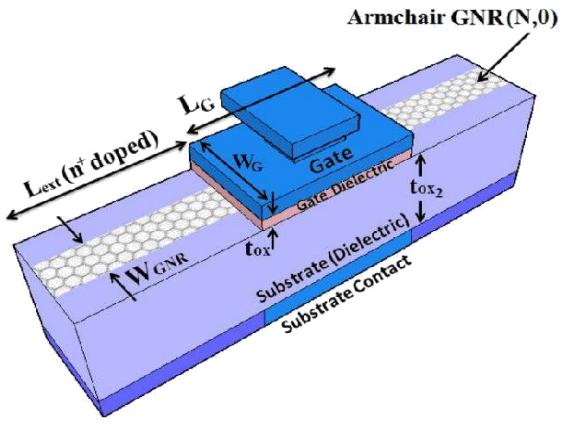

Fig 4:GNRFET

DRAWBACKS OF CMOS:

- CMOS technology requires a large number of transistors and the process is complicated.
- Silicon becomes hot very fast which is a big issue as it may lead to melt down of a computer chip.
- CMOS circuits are susceptible to damage by static electricity.
- PMOS size should be large enough to achieve electrical symmetry.

ADVANTAGESOFGNRFETS

- Use graphene powder, GNRFET's can be used to increase the performance of electrical batteries
- These FET's can also be used to manufacture high-frequency electronic devices.
- High current carrying power of GNRFET's.
- Graphene GNRFETs are made of high tensile strength and are the thinnest material ever available.

VOLTAGE LEVELSFORTERNARYLOGIC

Throughout the past few decades, binary logic technology has underwritten numerous studies and advances. Binary logic system is strong and efficient; however, it is not a perfect logic system since it occupies a wide area of the circuit chip.

Multi Valued Logics came into being as an alternative to surmounting the shortcomings of the binary logic system. Any scheme of logic with more than two states is called multi-value systems.

Voltage level	Logic value
0	0
1/2Vdd	1
Vdd	2

The structure of 3-Valued logic is called Ternary. Multi Valued Logics have numerous states of input and output. A ternary logic system that switches between three logic states '0', '1' and '2.'To build ternary gates from one power supply with V_{dd} voltage, logic level '2' and ground power supply level '0' and half of logic level input voltage '1' is used. The logic states in ternary logic system are described as

0 - False
1 –undefined
2 - True

Ternary logic provides some major advantages in constructing the digital device over the binary logic. Further information can be transmitted over a given set of lines or stored for a given register length, the size of the interconnections can be reduced, the chip area can be reduced and error detection and error correction code can be used further efficiently using Ternary Logic. In addition, the memory requirement would be reduced dramatically.[6]

3. ANALYSIS OF SIMULATION RESULTS

The simulation results for the CMOS and GNRFET circuits are shown in tables 2,3 and 4 below.From these findings it can be observed that the power absorbed by GNRFET circuits is smaller than that of CMOS circuits. In GNRFET-based circuits the time delay is also less than in CMOS circuits

Table -2: Simulation results for ternary inverters

	STANDARD TERINARY INVERTER		POSITIVE TERINARY INVERTER		NEGATIVE TERINARY INVERTER	
	GNRFET	CMOS	GNRFET	CMOS	GNRFET	CMOS
STATIC POWER	6.831e-08	1.351e-04	1.809e-110	1.133e-11	1.628e-12	7.069e-09
DYNAMIC POWER	1.351e-03	1.351e-03	1.809e-11	1.133e-10	1.628e-11	7.069e-08

Table -3: Simulation results for ternary logic gates

	TNAND Gate		TNOR Gate	
	GNRFET	CMOS	GNRFET	CMOS
STATIC POWER	3.40e-10	2.424e-08	8.471e-09	2.951e-07
DYNAMIC POWER	3.345e-08	2.028e-07	2.233e-05	1.517e-04

Table -4: Simulation results for ternary arithmetic circuit

	HALF ADDER		MULTIPLIER	
	GNRFET	CMOS	GNRFET	CMOS
STATIC POWER	1.349e-06	4.460e-06	7.113e-08	1.482e-07
DYNAMIC POWER	3.327e-05	9.230e-05	1.530e-06	6.314e-06
TIME DELAY	5.158e-11	1.153e-08	2.055e-08	1.140e-08

4. CONCLUSIONS

Ternary logic architecture is implemented using both CMOS transistors and GNRFETs. Designed are Ternary Inverters, TNAND and TNOR gates, Half Adder and Multiplier circuits.

It can be observed that circuits using GNRFETs consume less power and have less delay compared to those using CMOS transistors resulting in GNRFETs having great potential in low-power applications manufacturing.

The output waveforms of circuits using GNRFETs may also be found to be smoother than those using CMOS transistors.

GNRFET circuits give higher efficiency, lower energy consumption and comparable reliability to scaled CMOS circuits which are more prone to variations and defects at similar operating points. Thus GNRFET circuits in nano-electronics are favored.

ACKNOWLEDGEMENT

We express our earnest gratitude to our Guide, **V.Kumaraswamy,** for his constant support, encouragement, guidance and motivating us in our endeavor and helping us to realize our full potential. We are grateful for his cooperation and variable suggestions.

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