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Hardware Implementation of Synchronous Forward Converter with Active Clamp Reset Technique

Triveni K T[1], Rudranna Nandihalli[2], B K Singh [3]

[1]*PG Student, Department of Electrical and Electronics Engineering, RV College of Engineering, Bengaluru*
[2]*Professor and HoD, Department of Electrical and Electronics Engineering, RV College of Engineering, Bengaluru*
[3]*Senior Manager, Design and Engineering, Centum Electronics Limited, Bengaluru*

Abstract - *Various sectors like telecom, industrial, automotive, military and aerospace require regulated power supplies. SMPS is chosen over linear power supplies for obtaining regulated outputs. Various topologies of SMPS are available for medium power applications. Forward converter topology is selected for the work. The efficiency of the forward converter with output current more than 10A is less due to the conduction losses in the diode at the secondary side. The use of MOSFET in place of the diode in high current application (>10A) reduces the conduction losses. This technique of synchronous rectification is adopted at the secondary side of Forward converter. There is accumulation of flux after each switching cycle finally resulting in core saturation. A tertiary winding is used to reset the core after each switching cycle. But a sufficient time has to be allocated for the core reset, as a result duty cycle in such converters is limited to 50%. This drawback is overcome by adopting an active clamp reset technique. The active clamp circuit reduces the stress on the main switch and improves the performance of the converter. The converter is designed for total output power of 150W. The 150W synchronous rectified forward converter of 5V/30A output is designed with a clamp circuit and self-driven synchronous rectifier. The closed-loop implementation is provided by the type II controller. UC2825 PWM controller is used for generating PWM pulses for main MOSFET and active clamp MOSFET. The UC2715 complementary driver is used to drive the synchronous MOSFETs.*

Key Words: Forward converter, Active clamp, Synchronous rectifiers, Voltage stress, UC2825 PWM controller, UC2715 driver**.**

1. INTRODUCTION

With advancements in electronics, there has been a drastic increase in the need for power supplies. A regulated input voltage is required for the proper operation of many electronic circuits. Power supplies are the intermediate stage between the power source and the electric or electronic load. The disadvantages of traditional linear power supplies are overcome by switched-mode power supplies. Reduced size and high efficiency are the advantages of switched-mode power supplies [1].

Among the isolated converters, Forward converters are generally used for applications requiring lower load voltages and higher load currents [2]. The active clamp circuit consists of capacitor and MOSFET. This active clamp MOSFET reduces the stress on the main MOSFET and improves the overall efficiency of the converter [3]. The principle of synchronous rectification is adopted at the secondary side to overcome the conduction losses due to the Schottky diodes [4].

1.1 Active clamp technique

The clamp circuit comprises of an active MOSFET and capacitor. In the active clamp reset technique, accumulated residual energy in the primary winding is absorbed to charge the capacitor of the active clamp circuit. During the discharge period of the clamp capacitor, power is fed back to the source. As a result, the overall converter efficiency is improved [4].

1.2 Synchronous Rectification

In many applications diodes are used for rectification. Due to the diode conduction losses the overall power loss increases. The conduction losses are high in applications having higher current ratings. MOSFET 's corresponding forward voltage drop is very small relative to the forward voltage drop in the diode. Hence, diodes at the secondary side are replaced by MOSFETs. In the secondary side a self-operating strategy is used to power the synchronous MOSFETs [5].

2. SCHEMATIC REPRESENTATION OF CONVERTER

The proposed schematic representation of the converter is as shown in Fig 1.

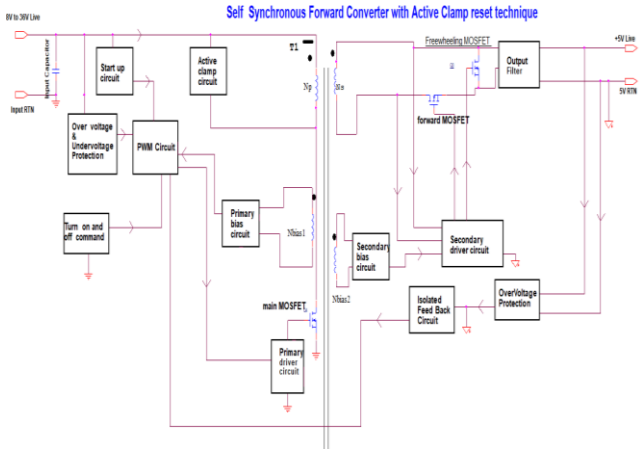

Fig 1 Schematic Representation of the Converter

The input live and return lines supply power to the converter. The main transformer is connected between live and return lines. The secondary side of the transformer comprises synchronous MOSFETs, filter and load circuit. The startup circuit consists of a TL431 regulator to provide fixed voltage to power the PWM IC and driver IC. The active clamp block enables the complete reset of the transformer core before the start of the next switching cycle. The bias winding is also energized along with the secondary winding during the energy transfer from the supply side to the load side. The bias winding develops sufficient voltage to power the PWM and driver IC. The startup circuit is disconnected after the bias winding develops the required voltage to power PWM IC and driver IC. UC2825 PWM IC provides complimentary gate pulses to main MOSFET and active clamp MOSFET through the driver IC. Self-driven synchronous rectification is employed at the secondary side [6]. The gate drives for the forward and freewheeling MOSFETS are directly obtained from the transformer secondary voltage. During the switch-on period of primary MOSFET, the forward MOSFET is driven into conduction. During the switch-off period, freewheeling MOSFET provide a path for the load current. Protection against input overvoltage and undervoltage is provided. Under these conditions, an active high signal is provided to the shutdown terminal of PWM IC. A portion of the output voltage is transferred to the feedback circuit via a resistive voltage divider circuit. The PWM controller in the primary side is supplied with the output of feedback circuit.

Table 1: Functions of various blocks

Sl. No	BLOCK	FUNCTION
1	Bias Circuit	To supply power to the IC after the startup circuit is disconnected
2	Startup circuit	To supply power to the PWM and driver IC until the bias circuit is activated
3	Turn on and off command	Used to turn on and off the converter externally
4	PWM Circuit	To set the operating frequency and generate gate signals for controlled output
5	Driver circuit	To supply gate signals with required current to switch on the MOSFET
6	Active clamp circuit	To reduce the voltage stress and for the transformer core reset.
7	Feedback isolation	Magnetic isolation for the error feedback signal
8	Protection circuits	Provide protection against overvoltage and under voltages
9	Output filter	To filter the ripple content at the output side

The proposed converter specifications are mentioned as follows.

Minimum Input voltage (Vin_{min}) : 18V
Nominal input voltage : 28V
Maximum input voltage (Vinmax) : 50V
Efficiency (η) : >80%
Line regulation : ±1%
Load regulation : ±1%
Maximum voltage ripple : 100mV
Maximum Duty ratio (Dmax) : 65%
Output voltage (Vo) : 5V
Output current (Io) : 30A

3. DESIGN OF COMPONENTS

The chosen transformer core has flux density Bm of 0.12 T and core cross sectional area Ac = 144mm⁴

- Calculation of Primary turns

$$N_P = \frac{Vin_{min} \times D_{max}}{B_m A_c \times 10^{-6} F_{sw}} = 4 \quad (1)$$

- Calculation of Secondary turns

$$\frac{N_s}{N_p} = \frac{Vout}{Vin_{min} \times D_{max}} = 0.42 \quad (2)$$
$$Ns = 0.42 \times 3.584 = 2$$

- Calculation of Minimum duty cycle

$$Dmin = \frac{Vo}{K . V_{inmax}} = 0.208 \quad (3)$$

- Calculation of Output inductance

$$L_o = \frac{Vo*(1-Dmin)*Ts}{\Delta iL} = 4\mu H \quad (4)$$

- Calculation of Output Capacitance

$$C_o = \frac{1-Dmin}{(8*L*Fsw^2*\Delta Vo)} = 105uF \quad (5)$$

- Calculation of Clamp Capacitance

$$Cclamp = \frac{(1-Dmin)^2 \Delta Imag}{1.6*Vinmax*Fsw} = 17.54nF \quad (6)$$

4. HARDWARE IMPLEMENTATION

The proposed converter is implemented with the proposed design methodology. The converter is implemented using a three-layer printed circuit board. The PCB is tested for the correct circuit paths and continuity is checked at different ground points. The selected components are assembled in the verified circuit board according to the component designation. Fig 2 shows the upper view of the PCB.

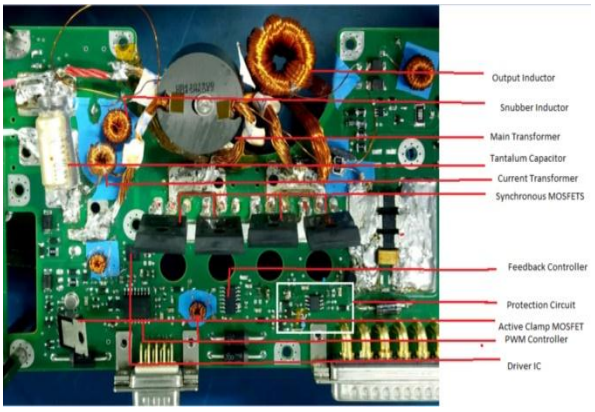

Fig 2 Upper view of PCB

The lower view of the PCB is as shown in Fig 3.

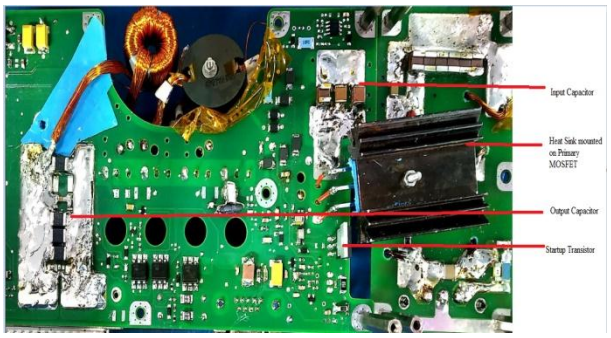

Fig 3 Lower view of PCB

The hardware setup for testing is as shown in Fig 4.

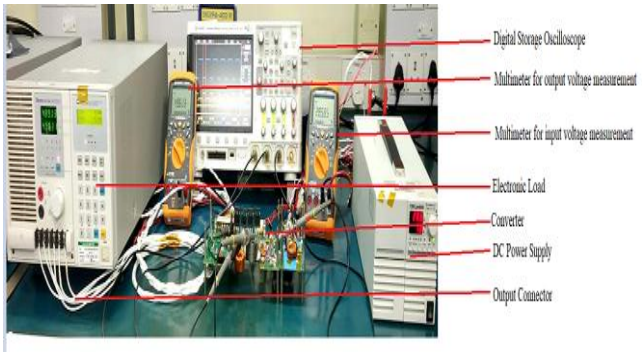

Fig 4 Hardware setup

A linear regulated DC power supply supplies power to the converter. A Multimeter is connected in series between DC supply and converter input for input current measurement. Similarly, a multimeter is connected in parallel across the input terminals for the voltage measurement. A digital oscilloscope of storage is employed to collect the waveforms of the various components. For various constant current output settings, a programmable electronic load is placed at the output terminals to power the converter.

The DC power supply is turned ON. Nominal input voltage is provided to the converter. The required amount of load is applied in increments through the electronic load. The corresponding values recorded in the input side and output side multimeters are noted. The gate and drain voltage waveforms of MOSFETs are captured using DSO. The readings are recorded by applying the load in increments until the full load condition is reached. The converter efficiency is assessed for the complete spectrum of input voltages. At the instant the input voltage exceeds the specified overvoltage value, the overvoltage protection circuit is activated. The PWM pulse generation from the controller is terminated and the output side multimeter reads zero value.

5. RESULTS AND WAVEFORMS

From the design specifications, the limit on line and load regulation is 1%.

5.1 Calculation of Line regulation:

$$\%\text{line regulation} = \frac{Vo(vinmax) - Vo(vinmin)}{Vo(nominal)} * 100$$

The line regulation of the converter at 50% load is shown in Table 2.

Table 2: Readings at 50% load

Input voltage (volts)	Input current (Amps)	Output voltage (volts)	Output current (Amps)	%Line regulation
18	4.48	4.817	15	0.228
28	2.9716	4.8162		
36	2.3735	4.819		
50	1.664	4.828		

Table 3 shows the line regulation of the converter at 100% load.

Table 3: Readings at 100% load

Input voltage (volts)	Input current (Amps)	Output voltage (volts)	Output current (Amps)	%Line regulation
18	9.4	4.8173	30	0.197
28	5.9	4.8202		
36	4.5	4.8224		
50	3.36	4.8268		

5.2 Calculation of Load regulation:

$$\%Load\ regulation = \left(\frac{Vo(minload) - Vo(maxload)}{Vo(nomload)}\right) * 100$$

The input voltage is kept constant at 28V. The converter readings are obtained for various load conditions as shown in Table 4.

Table4: Readings at nominal voltage

Input voltage (volts)	Input current (Amps)	Output voltage (volts)	Output current (Amps)	%Load regulation
28	1.9357	4.8153	10	0.1016
	2.8911	4.8162	15	
	3.86	4.8184	20	
	5.926	4.8202	30	

The load regulation of the converter at maximum input voltage of 50V is as shown in Table 5.

Table 5: Readings at maximum voltage

Input voltage (volts)	Input current (Amps)	Output voltage (volts)	Output current (Amps)	%Load regulation
50	1.1677	4.8262	10	0.0124
	1.692	4.828	15	
	2.236	4.8294	20	
	3.3637	4.8268	30	

The percentage line and load regulations are well within the specified values of 1%.

5.3 Calculation of Efficiency:

The efficiency of the converter at 50% load condition for different input voltage is as shown in Table 6.

Table 6: Efficiencies at 50% load condition.

Input voltage (volts)	Input current (Amps)	Output voltage (volts)	Output current (Amps)	Efficiency (η) in %
18	4.48	4.817	15	0.896
28	2.9716	4.8162	15	0.8681
36	2.3735	4.819	15	0.870
50	1.664	4.828	15	0.871

The specified efficiency is > 80 %. The converter at half load condition has efficiency of more than 80%. The readings of the converter are recorded at full load for different input voltage and the corresponding efficiencies are noted as shown in Table 7.

Table 7: Efficiencies at 100% load condition

Input voltage (volts)	Input current (Amps)	Output voltage (volts)	Output current (Amps)	Efficiency (η) in %
18	9.4	4.8173	30	86.4
28	5.9	4.8202	30	87.533
36	4.5	4.8224	30	89.303
50	3.36	4.8268	30	86.19

The efficiency of the converter at full load is more than 80% throughout the input range and has met the specified value.

5.4 Hardware Waveforms

The proposed converter topology is tested and hardware waveforms are obtained using digital storage oscilloscope.

Fig 5 shows the primary side main MOSFET secondary side forward MOSFET and freewheeling MOSFETS gate waveforms for nominal input voltage and full load conditions of 28V and 30A. The complementary gate signals are generated for forward and freewheeling MOSFET.

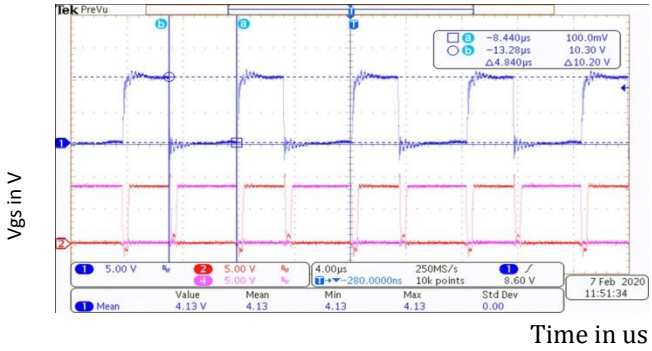

Fig 5 Vgs of the main MOSFET (blue), forward(red) and freewheeling(pink) MOSFETs at nominal voltage and full load

Fig 6 shows primary side main MOSFET, secondary side forward MOSFET, and freewheeling MOSFET drain waveforms for nominal input voltage and full load conditions of 28V, 30A.

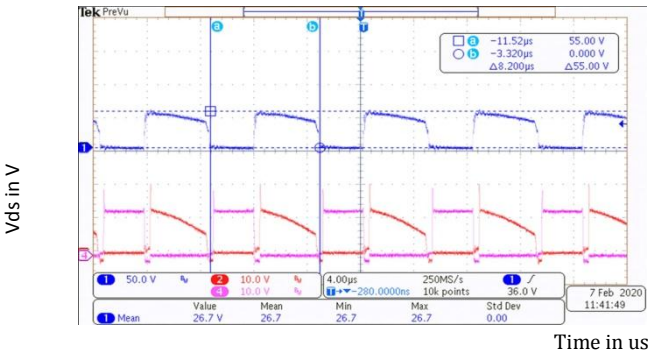

Fig 6 Vds of the main MOSFET (blue), forward(red) and freewheeling (pink) MOSFETs at nominal voltage and full load

Fig 7 shows active clamp MOSFET drain concerning to the primary main MOSFET drain waveform.

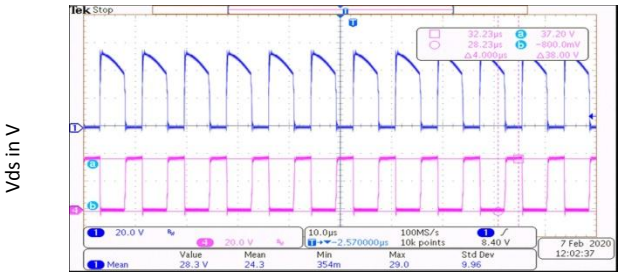

Fig 7 Vds of main MOSFET (blue) and active clamp MOSFET (pink)

The active clamp MOSFET gate waveform concerning the main MOSFET gate waveform is as shown in Fig 8.

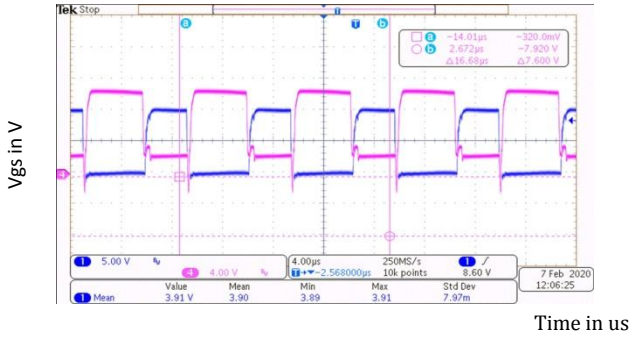

Fig 8 Vgs of main MOSFET (blue) and active clamp MOSFET (pink)

6. CONCLUSION

Active Clamp Synchronous Forward Converter is implemented. High efficiencies at a full load of 30A is achieved by using MOSFETs in place of diodes at the secondary side for rectification. The clamp technique reduces the voltage stress of the primary switch Hardware prototype is implemented and is tested under various input and output conditions. From the analysis of hardware results it is observed that the converter is operating at an efficiency greater than 80%. The line and load regulations are found to be less than ±1% and the output ripple voltage is less than 100mV. The experimental results obtained for various input and load conditions are meeting the values of the design specification.

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