

# Online Ageing Monitoring System for IoT Devices based on Cloud

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**Abstract** - Traditionally, the ageing has been performed in setting where check has been applied to accelerate the ageing process then a model is established to form the futuristic prediction. Reliability of an device, concerning if it can function reliably over its designated lifetime within the field (such as 10 or 15 years), has become more and more important in today's safety-critical applications like automotive electronics. This type of method contains a drawback of not having the ability to require into consideration the factor of the unique operating condition and environment that a tool could have experienced within the Old during this work, we present the cloud-based ageing monitoring system to the simplest of our knowledge, for the Internet-of-Things (IoT) devices. It has many advantages. One can know the ageing status of an IoT device remotely and continuously. Secondly, through data analysis in an exceedingly cloud server, more accurate prediction are often achieved. Thirdly, an ageing hazard are often alarmed before it actually strikes, and thereby pre-caution actions (such as online repair, or perhaps call-for-maintenance request) are often taken before to avoid unnecessary system fatal failure. A system with prototype using test chips with built-in design for ageing monitoring circuitry are demonstrated with measurement data collected through a Cloud server.

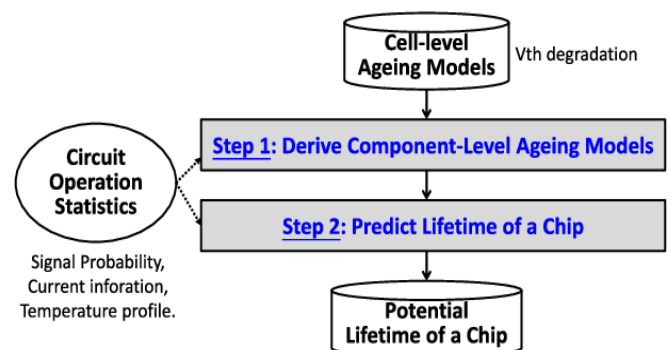
**Key Words:** Ageing monitoring, reliability, Internet of Things, stress test, ring oscillator.

## 1. INTRODUCTION

The scaling of integrated circuit technology brings numerous advantages, such as higher speed, the reduction of the form factor and lower power. However, the concern of reliability over a long lifetime as required by critical applications for safety e.g., automobile electronics, biomedical electronics, and various IoT devices is getting more and more challenging [1], [2]. Such as an automotive IC is required to operate in the field for more than 10 to 15 years under hostile conditions (e.g., -40C to 150C). It is well known that the reliability in terms of the failure rate is a function of time, following a bathtub curve which is divided into three stages i.e. mortality stage, normal lifetime stage and final ageing stage. The high infant mortality stage can be skipped by applying stress tests (with higher temperature and/or higher VDD) to eliminate the weak devices with potential latent defects. It is hopeful that, most shipped devices can operate in a system during its normal lifetime stage with reasonably low failure rate for certain amount of time.

There are several differing kinds of ageing mechanisms [3]-[6], e.g., Bias Temperature Instability (BTI), Electro Migration (EM), Hot Carrier Injection (HCI), and Thin-Oxide Breakdown, etc. When the ageing effect turns serious, sudden functional failure could occur. As a result, a safety-critical device should have a collection of anti ageing solutions during the planning stage, manufacturing test stage, and in the field stage, so on meet the target reliability requirement.

The ageing prediction may be done statically by offline ageing analysis, as depicted in Fig. 1. At the cell level, the ageing phenomenon of a transistor or an interconnect under a specific process technology is first characterized by embedded ageing sensors (e.g., ring-oscillator) to live the  $V_{th}$  and/or performance degradation under certain temperature or VDD stress conditions, (e.g., 195 C for six months) [7]-[10]. This is offline characterization process produces various fundamental cell level ageing models.



**Fig 1:** Traditional static ageing analysis to derive the potential lifetime of an IC based on a given set of cell-level ageing models and circuit operation statistics.

With the cell-level ageing models in place, a designer can then perform the ageing analysis [10], taking into account the Circuit Operation Statistics (COS), such as signal probability, current information at each node, and temperature profile, etc. In some sense, COS information reflects how rigorously each transistor and interconnect has been exercised or stressed. Then, a component-level ageing model can be derived, describing the performance degradation of each circuit block or component over the time. In some previous works, COS might be referred to as *workload*. Throughout this paper, we will use these two terms without distinction. Next, at the chip level, the ageing model for each component can be combined to predict the overall lifetime of a chip, and hopefully revealing the ageing-vulnerable spots at the same time.

The above ageing analysis is becoming more and more inevitable during the design process for a reliability conscious IC product. Even though it may not be very accurate, it does provide first-degree estimation and early feedback to the design process for lifetime enhancement. The inaccuracy of static ageing analysis mainly arises from the hypotheses used in mapping the cell-level ageing models to the component-level models. These hypotheses may not be very consistent with the reality. For example, it is a still issue how a cell-level model derived based on measurement data over a timing window of just 6 months can be extrapolated to an extended lifetime such as 10 years. Also, the assumed COS information is often too simplified and does not fully reflect the true situations in the field. In reality, each chip is likely to have a unique ageing process based on its own Circuit Operation Statistics (COS). To take this practicality into account, a more integrated method is needed. To address this challenge, we propose a highly integrated cloud-based online ageing monitoring and prediction methodology in this work, with the following key features:

- (1) Ageing monitors are inserted in the chip to collect online ageing information, as some previous works [9], [10]. But how these data are utilized afterwards is different.
- (2) An offline ageing characterization process (with some assumed stress test procedure) is performed on a number of fabricated chips to derive the so-called collective "accelerated ageing models".

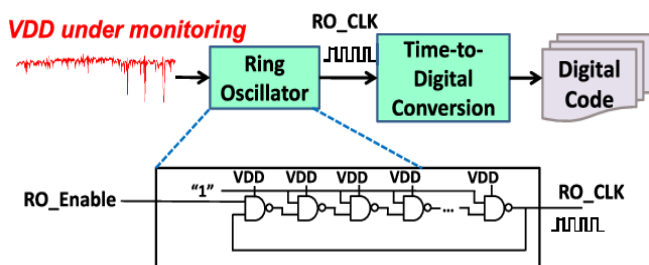


Fig 2: Ring-Oscillator based monitor.

- (3) For the online operation, each individual chip sends its Ageing data periodically to a designated cloud server as "ageing history". Then, over the time, more accurate IC-specific ageing and lifetime prediction is performed in the cloud and warning message is sent to each specific chip with the threat of ageing. During this process, the collective "accelerated ageing models" is converted into an IC-specific ageing model, which takes into account its unique "ageing history".

The proposed cloud-based online ageing monitoring and prediction is particularly effective as compared to the previous works in two aspects. First, the genuine COS information through an IC's life cycle is faithfully reflected in the ageing history, to render accurate lifetime prediction. Second, the ageing threat can be detected quickly and therefore preventive measures can be taken in a timelier

manner to avert the ageing-induced catastrophe. The preventive measures could take multiple forms, such as reconfiguration of the functional units in a chip, immediate replacement by a refreshing unit, or a warning signal calling for maintenance. We believe that our work is the first to use the "ageing history" in conjunction with the "accelerated ageing model" to produce IC-specific ageing model, and thereby making accurate lifetime estimation possible for each individual IC.

The rest of this paper is organized as follows. In Section II, we first provide preliminaries. In Section III, we present the proposed online ageing monitoring and prediction methodology including the ageing monitor, the overall system architecture, and the model translation scheme and system integration. In Section IV, we report the silicon results based on fabricated test chips, and in Section V we conclude.

## 2. PRELIMINARIES

It is quite common that Ring-Oscillators (RO) are used as monitors for the measurement of the results of method, VDD voltage, Temperature, and Ageing (or conjointly referred to as PVT effects). Fig. 2 a pair of shows Associate in nursing example [14]. The ring generator produces a clock signal, with the clock amount, referred to as ROCP, bearing the knowledge of combined PVT effects. When a time-to-digital converter, the time-varying clock amount is reborn to some digital codes for more analysis, some capturing the common ROCP, and a few capturing the worst-case ROCP. Resulting in helpful info concerning the method standing, the common and worst-case VDD voltages, and therefore the temperature, severally, it's doable to more decipher from the ensuing digital codes with the individual result of every conductive issue.

In this work, we have a tendency to use ROs for the aim of ageing watching. In general, it's kind of like the watching of PVT effects, however completely different within the following 2 aspects:

- (1) Ageing result happens rather more slowly than the results of the VDD voltage (changing in nano-seconds), and the temperature (changing in mini-seconds). Usually, it takes Weeks or maybe months for ageing result to be noticeable underneath a typical employment. Therefore, one solely has to take the ageing samples (e.g., one sample per day).
- (2) For monitoring dynamic VDD drop, one needs to capture and analyze not only the average, but also the worst case Ring-Oscillator Clock Period (ROCP) over a monitoring interval. For monitoring ageing effects, we only need to capture the average ROCP values at some specific sampling times. However, these average ROCP values need to be measured at a "proper condition" so the average performance of an RO monitor is only affected by the ageing effect alone, not by any other wanted PVT effects. In our system, we use the following condition:

Whenever we attempt to sample an average ROCP value bearing only the ageing effect, we set the chip to operate in the idle mode for a while (e.g., a few seconds) and so it will cool down to the ambient temperature with only little leakage current. Also, the current drained from the power/ground pads are stable and little, and thus the VDD voltage driving our RO monitor is also stable to remove the unwanted effect of dynamic VDD variation. The resulting average ROCP value is further compared to its time zero reference (recorded when the chip was just installed on the system board), and their difference reflects only the accumulated ageing effect from time zero up to the current sampling time. Certainly, one may need many RO monitors inserted in the chip, one for each selected site of interest. These RO monitors can be arranged into a special architecture, as shown in Fig. 3, so they can share the same clock period measurement circuit. At any given time, only one RO monitor is active and transfers its output clock signal, RO\_CLK, to the Clock Period Measurement (CPM) circuit.

### 3. PROPOSED CLOUD-BASED AGEING MONITORING

In this section, we introduce the proposed cloud-based online ageing monitoring methodology, including its benefits, architecture, operation flow, and test chip design.

#### 3.1 OVERVIEW

For an IC used in an Internet of Things (IoT) system, the data produced during the monitoring process can be sent to the cloud via existing wireless internet connection. Such a cloud-based monitoring methodology can have several benefits.

- (1) The *ageing history* of an IC (consisting of the average ROCP samples recorded over its lifetime) can be checked at anytime and from anywhere in the world.
- (2) In the cloud, the ageing histories of all ICs of the same type can be gathered and compared, and therefore, an IC with abnormal ageing conditions from the population can be easily identified as an outlier in terms of some features. When each IC is only monitored individually inside its own system, this kind of peer based over ageing detection cannot be easily performed.
- (3) As discussed earlier, a monitoring system is composed of not only hardware, but also software. In a cloud-based monitoring system, the software responsible for the “ageing data analysis” can be run in the cloud, rather than on the edge device containing the IC. Such an arrangement is more modular and flexible. A new version of ageing analysis algorithm whenever available, we only need to install it in the cloud. There is no need to

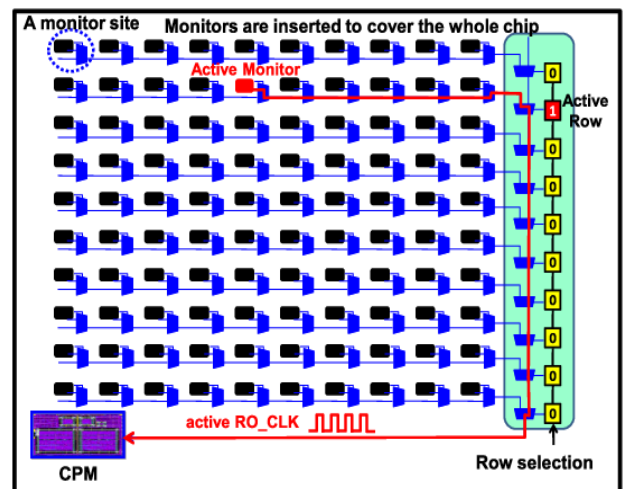


Fig 3: A two-level row-column daisy-chain for transferring a selected RO\_CLK to the CPM circuit [14].

update the software at the numerous edge devices, which can save a lot of efforts and costs. In terms of the architecture, a cloud-based monitoring system can be divided into three different domains as shown in Fig. 4, namely, (1) User domain, (2) Cloud domain, and (3) IoT Edge domain. This framework is not only scalable, but also easy-to-integrate in a way that the IoT edge devices are only responsible for producing the raw data, while the complicated back-end data analysis which creates meaningful ageing information from the raw data is performed at the cloud server. By such a hardware/software collaboration, the system becomes more flexible in its ability to distribute the functions among the edge devices and the server in a cost-effective manner. In more detail, the User part contains a control console which regulates the overall monitoring flow of all IoT devices. The Cloud part is located in a designated server which stores the gathered raw data and also supports the subsequent data analysis to predict ageing and lifetime. The IoT Edge part is associated with each device under monitoring, responsible for producing the ROCP raw data and transmitting the raw data through the internet to the cloud part.

#### 3.2 AGEING MONITORING FLOW

In this section, we explain our monitoring flow for “ageing and remaining lifetime prediction”, as outlined in Fig. 5.

It is divided into four phases. Part 1 and part 2 area unit only once effort created on variety of selected ICs once they're unreal. On the opposite aspect, part three and part four area units performed within the field of predefined observance intervals for every edge device.



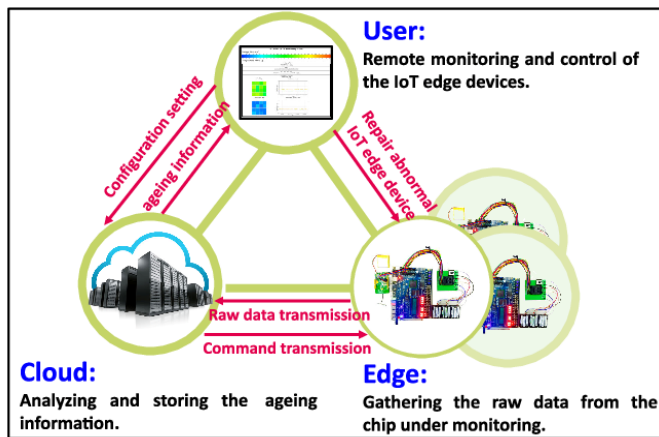


Fig 4: The user, cloud, and IoT edge parts of our cloud-based ageing monitoring system [14].

Model”): Having the results from the higher than ageing acceleration method, AN “accelerated ageing model” is made by setting the accelerated ageing information. we tend to use a polynomial of degree five because the setting operate as shown in Fig. 6. The ensuing “accelerated ageing model” could be a operate of your time, denoted as A(t)

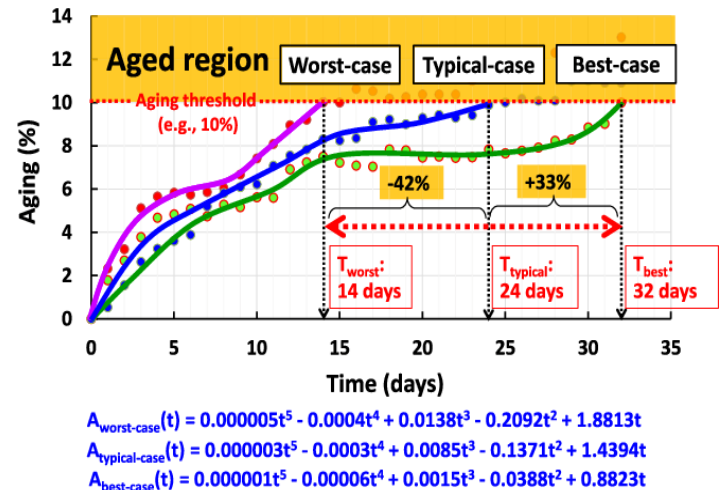


Fig 6: Accelerated ageing models derived by curve-fitting using polynomials of degree 5. Note that the accelerated ageing data in this figure are based on actual data based on the measurement results of fabricated chips.

Just like the temporal order model for a regular cell, our “accelerated ageing model” area unit derive in 3 cases: (1) worst case, (2) typical case, and (3) best-case, wherever the worst-case “accelerated ageing model” is non inheritable by taking the highest cover of these “accelerated ageing data” at every recording time obtained throughout the accelerated ageing method. Similarly, the best-case is non inheritable by taking rock bottom cover, whereas the typical-case is non inheritable by taking the typical “accelerated ageing data”. As shown in Fig. 6, our accelerated ageing method reaches a tenth ageing on these take a look at chips in fourteen days within the worse case, twenty four days within the typical case, and thirty two days within the best case. We have a tendency to use ulterior terms to help our subsequent discussions.

- $T_{worst}$ : The time needed to reach an ageing threshold (e.g., 10% ageing) using the worst-case accelerated ageing model.
- $T_{typical}$ : The time needed to reach an ageing threshold using the typical-case accelerated ageing model.
- $T_{best}$ : The time needed to reach an ageing threshold (e.g., 10% ageing) using the best-case accelerated ageing model.

Then, in our legal action,  $T_{worst}$  D fourteen days,  $T_{typical}$  D twenty four days,  $T_{best}$  D thirty two days. Taking typical as a reference, additional calculated 2 ratios to be used later once we conduct the remaining time period prediction, namely, the Ratio(worst-to-typical) D 14/24 D zero.58 (or -42%), and also the Ratio(best-to-typical) =

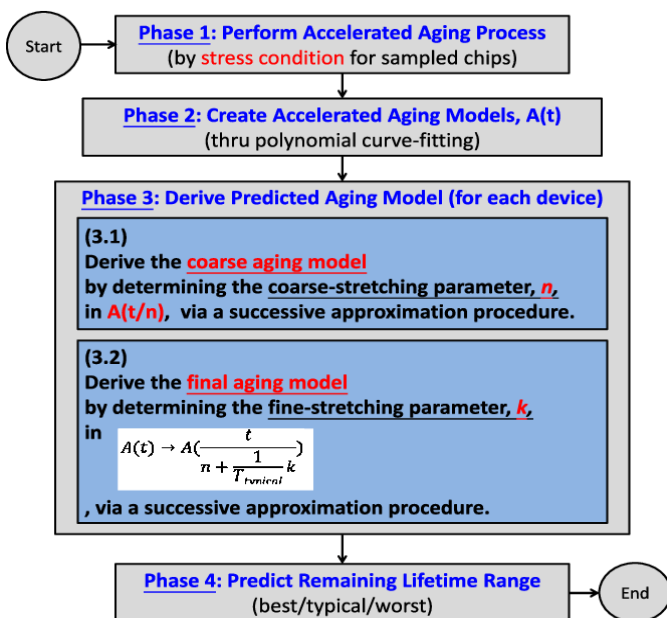


Fig 5: The overall flow for ageing and remaining lifetime prediction.

Phase 1 (Perform Accelerated Ageing Process):

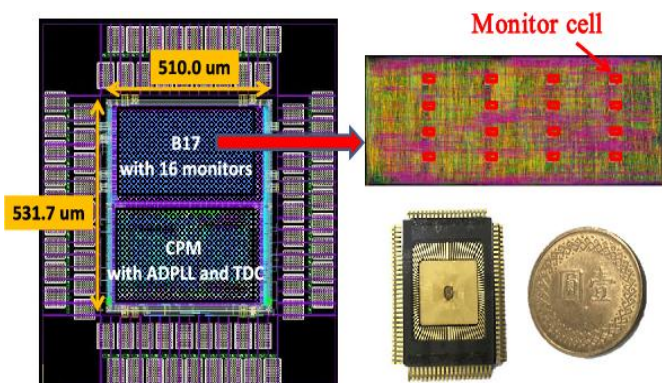
It is acknowledged that assay will be applied to accelerate the ageing method. This part is to watch however some of ICs selected for characterization throughout of the fine testing can age beneath stressed conditions. As an example, we tend to apply a “boosted offer voltage” two times the rated VDD level in our action at law, and then, their aged behaviors (rejected by the common ROCP values) area unit recorded over time. The ageing acceleration method is sustained till the IC beneath assay has aged on the far side a planned threshold (say 10%). as an example, in our action at law, we’ve 3 ICs beneath stress, and that we recorded the common RoCP prices of all sixteen RO monitors inserted within the IC once per day till all 3 ICs have aged by a threshold value of 100 percent (as compared to their time zero references). part two (Derive “Accelerated Ageing

$32/24 = \text{one.33}$  (or C33%). In some sense, the variation of accelerated ageing is during a vary of[-42%, 33%].

#### 4. MEASUREMENT RESULTS

##### 4.1. TEST CHIP DESIGN

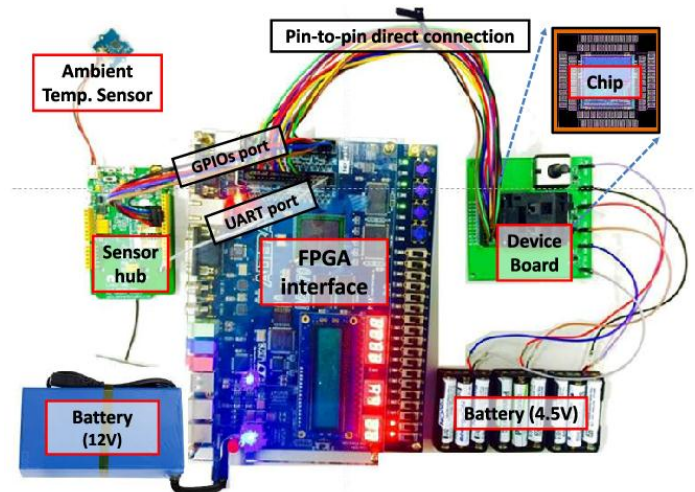
A benchmark circuit (B17) adopting the higher than ageing observation methodology has been designed and made-up as shown in Fig. 7. this is often additionally the chip we've went to conduct the experiments for PVT (Process, Voltage, and Temperature) observation in [14]. However, the methodology utilized in this paper for ageing prediction is extremely completely different from those utilized in [14], that is additional involved regarding capturing the worst-case dynamic VDD drops and therefore the temperature variation. This take a look at chip style is embedded with sixteen monitors and a logic BIST (Built-In Self-Test) circuit. The CPM circuit contains a Time-to-Digital device additionally as a cell-based Phase-Locked Loop made by in-house compilers. supported our take a look at flow, the sixteen monitors inserted would take communicate be ascertained, every of that produces associate RO\_CLK signal reflective the ageing condition at the positioning it monitors.



**Fig 7:** A benchmark circuit "B17" embedded with 16 monitors, a logic Built-In Self-Test circuit, and a CPM circuit. Note that, in addition to supporting ageing monitoring, this test chip also supports PVT monitoring proposed in [14].

##### 4.2. HARDWARE COMPONENTS

Our test chips are fabricated in a 90nmCMOSprocess.Achip Under monitoring is put into the socket on the device board, This is further connected to the FPGA interface board, sensor hub, ambient temperature sensor, and two battery modules as shown in Fig. 8, in our prototype system. We have built three of such prototype systems.



**Fig 8:** An IoT edge device harboring one of our test chips.

##### 4.3. SOFTWARE COMPONENTS

In addition to hardware, there are software components in our prototype system as listed in Table. 1. These software components are implemented in six different kinds of programming languages, including HTML, Javascript, PHPCSQL, Perl, Python, and C.

- (1) In the User part, there are about 500 lines of code using HTML language to build the overall structure of control console interface, with additional 400 lines of Javascript code to communicate with the cloud.
- (2) Within the Cloud half, there are four code components: together with User communication agent, info manager, PVT and ageing prediction, and Edge communication agent. The 2 communication agent provides bridge between Users half and a grip half for transmission commands, ROCP information, and PVT and ageing info, with regarding 850 lines of PHP code. The info manager has 142 lines of PHPCSQL code to support info functions. The ROCP modeling and PVT and Ageing prediction code element is that the major code element of this method, completed by 1360 lines of code in each Perl and Python language. It's chargeable for method activity, temperature-aware VDD-drop prediction, and remaining time period estimation.
- (3) Within the Edge half, there are 336 lines of C code, wont to perform wireless network association (using API functions given LinkIt-ONE) and edge device regulation. Within the following, we have a tendency to gift measuring results of ourcloud-based watching system for ageing prediction.

**TABLE 1:** List of software components in our cloud-based PVTA monitoring system.

Domain	Software	Language	Function	Lines of code
User	Control console	HTML	Website-based user interface	496
			Temperature/VDD-drop map display	105
		Javascript	Temperature/VDD-drop historical curve display	162
			PVTA information update	109
			Command transmission	35
Cloud	User communication agent	PHP	Command buffer management	122
	PVTA information transmission		333	
	Database manager	PHP + SQL	Database management	142
	ROCP modeling and PVTA prediction (MAJOR)	Perl	Process calibration	794
			Temperature-aware VDD-drop prediction	215
			Lifetime estimation	351
	Edge communication agent	PHP	Raw data packet receiver	300
			Command buffer checking window	89
Edge	Wireless network communication	C	Wireless network connection	124
			Command buffer checker	49
			Raw data packet transmission	87
	Device regulation	C	Command decoder	48
Raw data buffering			28	
Total lines of code				3589

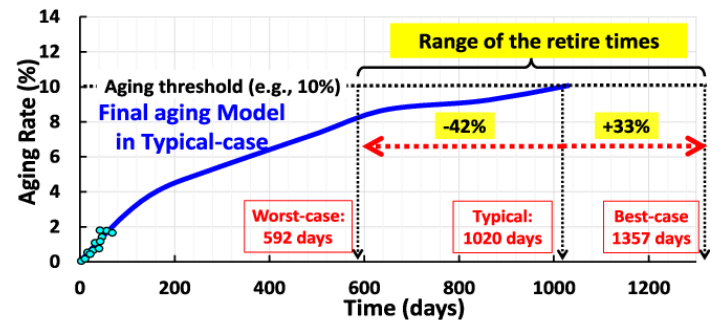
#### 4.4. AGEING AND REMAINING LIFETIME PREDICTION

The projected "accelerated ageing process" on 3 take a look at chips to derive the worst-case, typical-case, and worst-case "accelerated ageing models". Then, we use the three models to predict the "final ageing model" for one chip by the coarse-stretching and fine-stretching operations. The retire times of this chip are indicated in Fig. 9, as days, within the worst case, the standard case, and the best case, severally. With the data of those retire times, the remaining lifespan may be calculated thereby. For example, if the retire time is foretold once the chip has been operated for eighty days, then its remaining lifespan would be D days D years within the worst case, the standard case, and the best case, severally. Note that these lifetimes could appear comparatively short. It's partially as a result of we tend to operate this take a look at give a non-stop manner after we collected its "normal ageing data". If a chip is operated in a very additional relaxed manner (e.g., defrayment most of its time within the OFF-state), then it might age additional slowly.

#### 4.5. APPLICATION NOTES

In reality, associate degree IC might have several practical blocks. Each functional block might expertise its own distinctive work and therefore age at a unique pace. Despite the fact that the projected methodology is barely incontestable on the ring oscillators used because the ageing sensors, it may be integrated with alternative run-time ageing sensors still. every ageing sensor is employed to gather the net ageing history of a special functional block (such as cache memory, SRAM memory, logic blocks, etc.), so supported the prebuilt accelerated ageing model of that special practical block and the workload-aware on-line

ageing history, one will thereby accurately predict the ageing standing and therefore the remaining lifespan of every perform block. At associate degree "ageing observation center", a sign may be maintained to stay track of the ageing condition.



**Fig 9:** Final ageing model and remaining retire times (for one fabricated chip).

### 5. CONCLUSION

For safety-critical applications, a convincing methodology that will demonstrate however long Associate in Nursing IC can operate faithfully under the impudence of ageing is urgently required. Traditional ways in which of victimization strictly software-based prediction might not be adequate, because the results may well is rough. In lightweight of this, we've got projected a lot of correct technique during this paper. Our contributions are summarized in 2 aspects. First, the ageing and lifelong prediction will become a lot of credible since it's derived by not solely the fine "accelerated ageing model", however additionally on-line "ageing history" below traditional workload. Also, one will turn out a novel "lifetime" prediction for every individual IC. Second, Associate in nursing ageing watching system contains each hardware and code, and involves the information analysis for a bigger range of ICs spreading round the globe. By adopting a cloud-based technique, the system integration and maintenance become easier additionally. Activity information of take a look at chips are accustomed demonstrate the effectiveness of the projected methodology.

### REFERENCES

[1] V. Prasanth, D. Foley, and S. Ravi, "Demystifying automotive safety and security for semiconductor developer," in Proc. IEEE Int. Test Conf. (ITC), Oct./Nov. 2017, pp. 1\_10.  
 [2] G. A. Klutke, P. C. Kiessler, and M. A. Wortman, "A critical look at the bathtub curve," IEEE Trans. Rel., vol. 52, no. 1, pp. 125\_129, Mar. 2003.  
 [3] J. H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," Microelectron. Rel., vol. 46, nos. 2\_4, pp. 270\_286, 2006.  
 [4] T. Wang, L.-P. Chiang, N.-K. Zous, C.-F. Hsu, L.-Y. Huang, and T.-S. Chao, "A comprehensive study of hot carrier stress-



induced drain leakage current degradation in thin-oxide n-MOSFETs," IEEE Trans. Electron Devices, vol. 46, no. 9, pp. 1877\_1882, Sep. 1999.

[5] M. Kimura, "Field and temperature acceleration model for time-dependent dielectric breakdown," IEEE Trans. Electron Devices, vol. 46, no. 1, pp. 220\_229, Jan. 1999.

[6] K. N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," J. Appl. Phys., vol. 94, no. 9, pp. 5451\_5473, 2003.

[7] K. K. Kim, W. Wang, and K. Choi, "On-chip aging sensor circuits for reliable nanometer MOSFET digital circuits," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 10, pp. 798\_802, Oct. 2010.

[8] B. Jang, J. K. Lee, M. Choi, and K. K. Kim, "On-chip aging prediction circuit in nanometer digital circuits," in Proc. IEEE SoC Design Conf. (ISOCC), Nov. 2014, pp. 68\_69.

[9] S. Majerus, X. Tang, J. Liang, and S. Mandal, "Embedded silicon odometers for monitoring the aging of high-temperature integrated circuits," in Proc. IEEE Nat. Aerosp. Electron. Conf. (NAECON), Jun. 2017, pp. 98\_103.

[10] D. Sengupta and S. S. Sapatnekar, "Estimating circuit aging due to BTI and HCI using ring-oscillator-based sensors," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 36, no. 10, pp. 1688\_1701, Oct. 2017.

[11] A. Goel and R. J. Graves, "Electronic system reliability: Collating prediction models," IEEE Trans. Device Mater. Rel., vol. 6, no. 2, pp. 258\_265, Jun. 2006.

[12] IEEE Standard Framework for the Reliability Prediction of Hardware IEEE Standard 1413, 2009.

[13] D. Lorenz, G. Georgakos, and U. Schlichtmann, "Aging analysis of circuit timing considering NBTI and HCI," in Proc. IEEE Int.-Line Test. Symp., Jun. 2009, pp. 3\_8.

[14] G.-H. Lian, S.-Y. Huang, and W.-Y. Chen, "Cloud-based PVT monitoring system for IoT devices," in Proc. IEEE Asian Test Symp. (ATS), Nov. 2017, pp. 76\_81.