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AN AREA EFFICIENT SCAN CHAIN ARCHITECTURE FOR MIXED MODE OPERATION

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Abstract - *In recent years, sequential output configuration has gotten the accepted structure for testability system. The simplicity of testing and high test inclusion has made it increase across the board mechanical acknowledgment. In any case, there are punishments related with the sequential check plan. These punishments incorporate execution corruption, test information volume, test application time, and test power dissemination. The presentation overhead of output configuration is because of the sweep multiplexers added to the contributions of each flip-flop. In the present very rapid plans with least conceivable combinational profundity, the presentation debasement brought about by the output multiplexer has gotten amplified. Subsequently, to keep up circuit execution, the planning overhead of sweep configuration must be tended to. In this paper, we propose another output flip-flop structure that disposes of the exhibition overhead of sequential output. The proposed structure expels the sweep multiplexer from the practical way. The proposed configuration can help improve the utilitarian recurrence of execution basic plans. Moreover, the proposed structure can be utilized as a typical output flip-flop in the "blended sweep" test wherein it tends to be utilized as a sequential output cell just as an arbitrary get to check (RAS) cell. The blended sweep test design has been executed utilizing the proposed examine flip-flop. The exploratory results show a promising decrease in interconnect wire length, test time, and test information volume, contrasted with the cutting edge RAS and various sequential output executions.*

***Key Words*: serial scan test, random access , scan test, mixed mode scan test, low power test, test application time, test data volume, scan flip flop.**

1. INTRODUCTION

TESTING of high complex SOC plans is a major challenge looked by VLSI test network these days. Sweep configuration is the main DFT approach that can adequately test a profoundly unpredictable plan with high shortcoming inclusion. The goal of sweep configuration is to accomplish full controllability and recognizability of each flip-flop in the structure. In a full output structure, each flip-flop is supplanted by a sweep flip-flop. An output flip-flop is only a mixed input ace slave based D type flip-flop. The sweep multiplexer has two sources of info: information input (D) and output input (SI). The info choice is performed utilizing a control signal called test empower (TE). In useful mode, information input is chosen and the sweep flip-flop work as a customary flip-flop. In test mode, check input is chosen, and all the check flip-flops associate in a sequential manner to shape at least one sequential move register(s). The sequential move register(s) is prominently known as output chain(s). Every single flip-lemon of the sweep chain are stacked with wanted information by back to back use of the clock signal. A full sweep configuration decreases the consecutive test issue to combinational test issue. The sequential output is clearly not liberated from downsides. There are some inborn punishments related with the sequential output. These punishments include: 1) execution overhead, 2) test information volume, 3) test power utilization, and 4) test application time. The presentation overhead of sequential sweep is expected to the filter multiplexer [1],[2],[4]. The output multiplexer falls into each timed way and includes execution punishment of roughly two entryway delays. A circuit without examine plan and with check configuration is appeared in Figure 1. As it is perceptible in Fig 1a, the basic way of a successive circuit without filter inclusion is chosen by the longest combinational way between two flip-flops. In any case, in an output embedded successive circuit (see Figure 1b) the equivalent basic way is prolonged by an output multiplexer toward the finish of the combinational way. The sweep configuration likewise includes an extra fanout at the yield of a flip-flop. Both of these elements increment the basic way delay, henceforth decreases useful clock speed by 5% to 10% [1]. This makes it important to kill the exhibition overhead of the sweep multiplexer. A few arrangements have been proposed to lighten the presentation punishment of sweep structure.

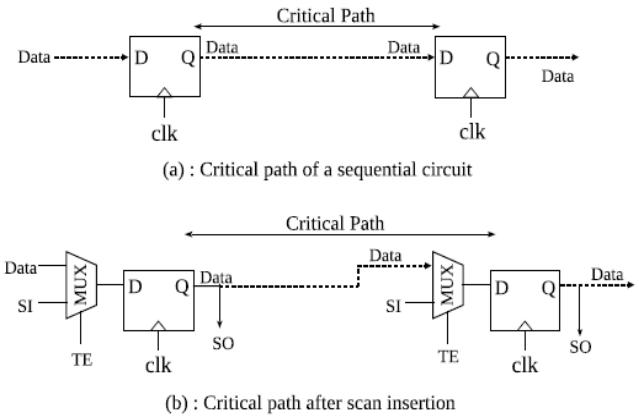

Fig.1 Scan design performance over head .

The vast majority of the fractional output procedures requires computationally requesting successive ATPG [5], and can't be managed with ever expanding circuit multifaceted nature. Moreover, halfway sweep plan procedures don't give high blame inclusion as gave by the full output structure, and it is hard to coordinate them into the current mechanical structure stream. Another methodology for dispensing with execution punishment of output configuration is to utilize examine cell structures which give superior. Galbi and Basto [14] proposed a double edge beat activated searchable flip-flop which is a superior and low force examine cell. In an ongoing work [3], Ahlawat et al. utilize an adjusted output cell wherein the examine multiplexer is killed off the useful way by utilizing separate ace lock for useful and test mode. These high performance filter cell plans can take out the presentation overhead of output plan [6]. Be that as it may, such output cells can't be utilized in a blended output test engineering. Arbitrary access check (RAS) is an option DFT system that can ease the issues related with the sequential sweep [7]. Writing shows that RAS can enormously lessen test application time and test information volume alongside test power decrease up to 99% [15].This paper proposes another sweep flip-flop structure that can be utilized as both a sequential sweep cell just as an arbitrary access examine cell. The significant focal points of the proposed examine flip-flop configuration are as per the following:

1) It disposes of the exhibition punishment of the sequential sweep by expelling check multiplexer from the utilitarian way.
2) It can be utilized both as a sequential sweep cell just as a RAS cell, in the blended mode check test.
3) The proposed structure doesn't present any extra control sign and uses the test control signal as a semi consecutive or low-recurrence filter clock.

The proposed plan completely agrees to the current industry plan and test stream. The rest of the paper is composed as follows: Segment II portrays the regular sweep flip-flop and the proposed examine flip-flop plan. Area III further explains on the subtleties of test application procedure and detainment for test quality. Area IV clarifies the post-design timing results.

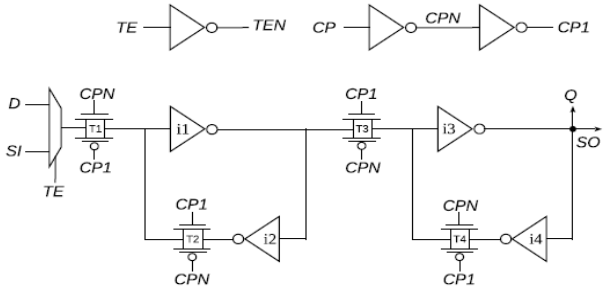

Fig.2 A conventional scan flip-flop design.

A conventional scan flip-flop design is shown in Figure 2. This scan cell is a master-slave latch based positive edge triggered mixed input *D* type flip-flop. The transmission gate *T*1, and the inverter pair connected back to back via transmission gate *T*2 forms the master latch. The slave latch comprises of transmission gate *T*3 and the inverter pair connected back to back via transmission gate *T*4. The multiplexer at the input of master latch selects between functional input (*D*) and scan input (*SI*) depending upon the value of test control signal test enable (*TE*). In test mode, when *TE* is high (1), *SI* is selected and is connected to master latch's input. When the clock signal (*CP*) is low (0), the value of *SI* propagates to the master latch. In the meantime, slave latch retains the value from previous clock cycle. The value latched into the master propagates to slave latch when *CP* turns to high (1), and to the output *Q* of scan flip-flop. Similarly, when the test enable signal (*TE*) is set to 0, functional input *D* is selected, and the circuit operates in functional mode.

2. Proposed Scan Flip-Flop Design

This section discusses the working of the proposed scan flip-flop in different modes of operation. The proposed scan flip-flop's schematic design is shown in Figure 3. Instead of a multiplexer at master latch's input, the proposed design uses a separate path for loading test vector values into the master latch. Furthermore, the proposed scan flip-flop uses a low-cost dynamic slave latch for shifting of test vectors in the test mode. In functional mode, functional slave latch's output *Q* drives the combinational circuit inputs. The master latch of the proposed scan flip-flop is formed by transmission gate *T*1, and inverter pair (*i*1, *i*2) connected back to back via

transmission gate *T*2. Similarly, the slave latch is formed by transmission gate *T*3, and inverter pair (*i*3, *i*4) connected back to back via transmission gate *T*4. The dynamic slave latch comprises transmission gate *T*7 and inverter *i*7. The test mode path is formed by adding transmission gate *T*5, *T*6, buffer *i*5, and inverter *i*6 to the master latch structure. It should be noted that the extra gates added to the master stage to form the test mode input path are not on the functional path. This extra circuitry remains disabled during the functional mode, and the proposed scan flip-flop acts as a regular flip-flop. The master latch and the slave latch are controlled by functional clock signal *CP*. The test mode input path is disabled by the test enable cum scan clock signal *SCK*. Note that, the *SCK* signal in the proposed scan cell is functionally equivalent to the test enable signal *TE*, however, in contrast to the conventional scan design in which *TE* is a purely combinational signal, *SCK* is a low frequency or quasi-sequential signal. The SCK signal is utilized both as test control just as a low frequency examine check signal in the proposed filter plan. Since the sweep activity is performed at a much lower recurrence, ordinarily at 10MHz to 50MHz, contrasted with the framework or utilitarian clock recurrence [8], the steering of SCK as a moderate recurrence examine clock sign won't present a lot of overhead as far as zone and force. The directing region and force overhead of SCK is investigated in result and examination segment [9]. The subtleties of the working of the proposed plan in various methods of activity are clarified in the accompanying subsections.

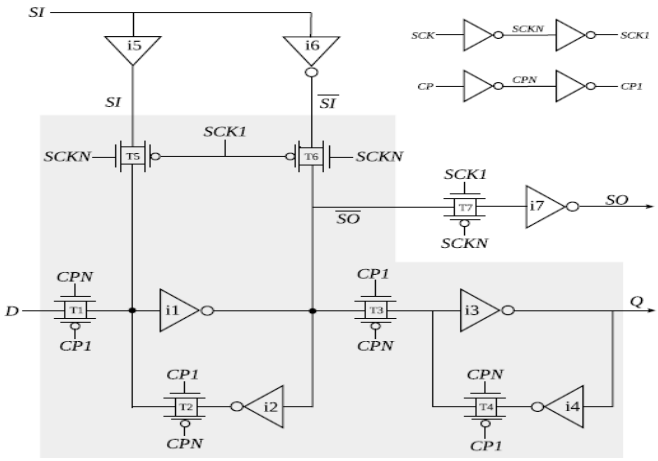

Fig.3.proposed scan flip-flop design.

2.1. Functional Mode

The proposed examine flip-flop fills in as an ordinary flip-flop in practical mode. In practical mode, check clock signal SCK is kept at consistent rationale high (1) level. As long as SCK is at consistent high (1) level the transmission door T5, and T6 stay handicapped. This separates the test mode input way from the ace structure and the proposed filter flip-flop works as an ordinary flip-flop. The sweep clock signal (SCK) held at consistent high (1) level shows utilitarian mode activity. During the practical mode activity, the transmission entryway T7 consistently remains empowered. This keeps the dynamic slave lock constantly straightforward during the practical mode and makes the sweep yield (SO) flip each time at whatever point there is an adjustment in ace lock's state. In any case, that isn't of any worry most definitely since the sweep yield (SO) drives just the output way which takes care of the sweep input (SI) of the progressive output flip-flop.

The output input way stays detached from the ace structure during the practical method of activity. The flipping of sweep yield SO will make exchanging action in the filter way which additionally occurs in the customary output plan. Since if there should be an occurrence of regular output cell the combinational load, just as the sweep way, is driven by the Q yield of the sweep cell. In this way, if there should be an occurrence of ordinary output cell during useful mode, at whatever point there will be a flipping on the Q yield, it will spread in both the combinational rationale as well in the output way [10] [11]. Likewise, in regular sweep cell, the output multiplexer which falls in the output way would disseminate excess power in both the modes. In practical mode, the ace hook of proposed filter cell gets it's contribution from the practical information input D. At the point when clock CP is low, the estimation of practical input D engenders into the useful ace hook. When CP goes to high, the worth locked into the ace proliferates to useful slave lock, and to yield Q of the output cell. We check the said usefulness utilizing post-design recreation.

2.2. Test Mode

While keeping the useful clock CP held at steady high (1) level, back to back use of check clock SCK makes the proposed examine flip-failure to work in test mode. As the practical clock CP is kept high (1), the transmission entryway T1 consistently stays debilitated in test mode. This detaches the useful info D from the ace hook. During test mode, the ace lock gets its info from scan input SI. The back to back use of output clock SCK loads the test esteems into the sweep flip-flops. As it very well may be seen in Figure 3, when SCK gets to rationale low (0), T5 and T6 get empowered, and the estimation of SI is composed into the ace hook along these lines to memory compose activity. It ought to be noticed that in test mode since CP is in every case high (1), the input way transmission entryway T2 consistently remains empowered. This makes the ace hook continually attempting to hold its past worth. Be that as it may, it very well may be seen from Figure 3, the test mode input way circuit power composes the SI esteem all the while at both info and yield hubs of inverter i1 by means of support i5 and inverter i6 separately. This makes the compose activity quicker undoubtedly.

When the output clock SCK gets high (1), the dynamic slave hook transmission door T7 gets empowered, and the ace hook begins driving both powerful slave hook inverter i7, and useful slave hook inverter i3. This engenders the test esteem hooked into the ace during the negative clock cycle, to dynamic slave lock, and to scan output SO of the output cell. At the point when sweep clock SCK gets to rationale low (0), T7 gets incapacitated, furthermore, the information parasitic capacitance of inverter i7 drives the progressive sweep cell's scan input SI. Because of the high impedance of the inverter, the parasitic capacitance doesn't release promptly and takes quite a while. The parasitic capacitance release time chooses the base output clock recurrence at which output moving should be possible. The parasitic capacitance release time essentially relies on two variables: all out info capacitance of inverter i7, and the charge spillage rate. Subsequently, for a specific manufacture process innovation with very much described spillage rate, the release time can be improved by controlling the complete info capacitance which thusly relies on the size of inverter i7. The size of inverter i7 can be scaled according to the necessary least output recurrence. Be that as it may, a low move recurrence is bothersome as it expands the test time, which thusly builds the test cost [12]. It ought to be noticed that in test mode the transmission door T3 consistently remains empowered. This keeps the practical slave hook constantly straightforward during test mode and makes the yield (Q) flip each time at whatever point there is an adjustment in ace lock's state. Each ace hook in check chain gets its sweep contribution from going before filter flip-lemon's SO yield, with the exception of the absolute first ace hook in the sweep chain which gets its test contribution from an essential info pin. The sweep yield SO of the last flip-lemon of the sweep anchor is associated with an essential yield pin. The moving of test vectors into the sweep chain is finished utilizing the dynamic slave lock. When the sweep chain is stacked, the test vector is propelled by means of the utilitarian slave lock.

3. Mixed Mode Scan design

This section describes the use of the proposed scan flip-flop to simulate mixed mode scan architecture. In mixed scan architecture, some of the FFs are used to form serial scan and rest of the flip-flops form RAS architecture. Both serial scan test architecture and RAS test architecture are operated parallel. In the rudimentary implementation of the mixed scan, the flip-flops that are included in serial scan architecture are replaced by a serial scan flip-flop and the flip-flops that are included in RAS architecture are replaced by RAS cell. In mixed mode scan design the clock needs to be kept high throughout the test mode to perform RAS cell read/write operation[13][14]. So, the serial scan part cannot be operated in concurrent to RAS using the conventional serial scan cell. The proposed scan cell overcomes this problem by using test control signal as a slow frequency scan clock and allows functioning both serial and RAS design in parallel.

3.1 Proposed scan Flip Flop as RAS Cell

The proposed scan design eliminates the need for two separate scan cell libraries for implementing serial scan part and RAS part. It provides a common scan cell as well as a RAS cell. Schematic design of area and performance efficient, progressive random access scan cell is shown in fig 4.

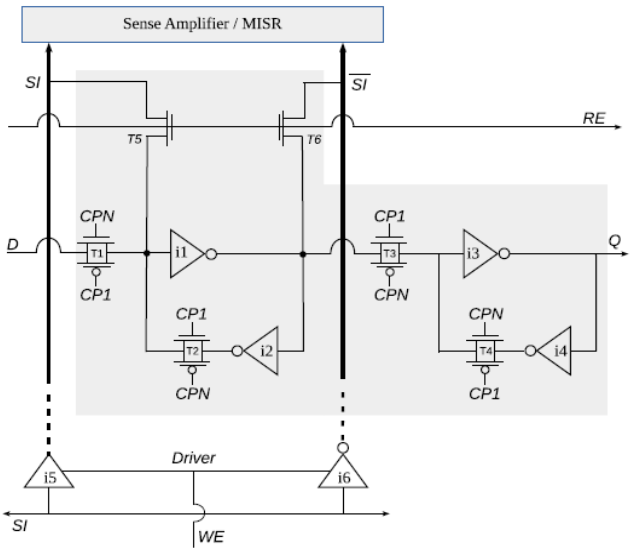

Fig.4.Progressive Random Access Scan (PRAS) cell

This *PRAS* cell is a modified design of a regular master-slave based positive edge triggered *D* type flip-flop. The grey part in Figure 4 depicts the *PRAS* cell, and the remaining circuit is part of *RAS* test architecture. The grey part of the proposed scan flip-flop shown in Figure 3 can be used as a base scan cell. The grey box of the proposed flip flop maps to the basic *PRAS* cell design except the access pass transistors are replaced by transmission gates (*T*5, *T*6). Both of these basic cells are functionally equivalent. Therefore, the same basic cell of the proposed design can be used as a *PRAS* cell without modification. Note that the proposed scan cell has one extra output node *SO* which remains unconnected in *RAS*. The base scan cell can be synthesized as a *PRAS* cell by mapping the base scan cell in/out signals with corresponding *PRAS* in/out signals to use in *RAS* test architecture. Similarly, the base scan cell can be synthesized as serial scan cell with the full logic shown in Figure 3. It is worth to note that with a minor change in synthesis process the proposed scan flip-flop can be synthesized as both serial scan cell and *PRAS* cell.

Furthermore, another major advantage of the proposed scan cell is that both serial scan design and *RAS* design can be

synthesized with a common clock tree. As discussed in the previous sections the clock is kept at a constant high level to operate the proposed scan cell in test mode, and test enable signal is used as scan clock. This can make the mixed mode scan architecture implementation very efficient and smooth.

3.2Mixed Mode scan Architecture

The architecture of mixed mode scan is shown fig 5.

The mixed mode scan architecture has three main components: Multiple Serial Scan (MSS) part, *RAS* part, and the test controller. The multiple serial scan part is denoted by p-serial, and *RAS* part is denoted by p-random. The p-serial part consists multiple serial scan chains with inputs *SI*0, *SI*1, and *SI*2, and a *MISR* at the outputs to compact the test responses. The number of scan chains can vary depending upon the available number of test pins. The shift operation in p-serial is performed by using the scan enable cum scan clock signal *SCK*. The *RAS* part is denoted by p-random and implemented as *PRAS* architecture . The row address shift register and column driver are used for writing test data. Based on the column address the test controller generates control signals to drive the *bit* and bit-bar lines using the column driver. The Sense Amplifier and MISR block are used to read and compact the test response data. The *MISR* for p-serial and p-random are connected serially with the controller to shift out the test response signature via the scan *I/O* port. The two input signals test-mode0 and test-mode1 connected to the test controller are used to operate the circuit between functional mode and the test mode and exercising the test.

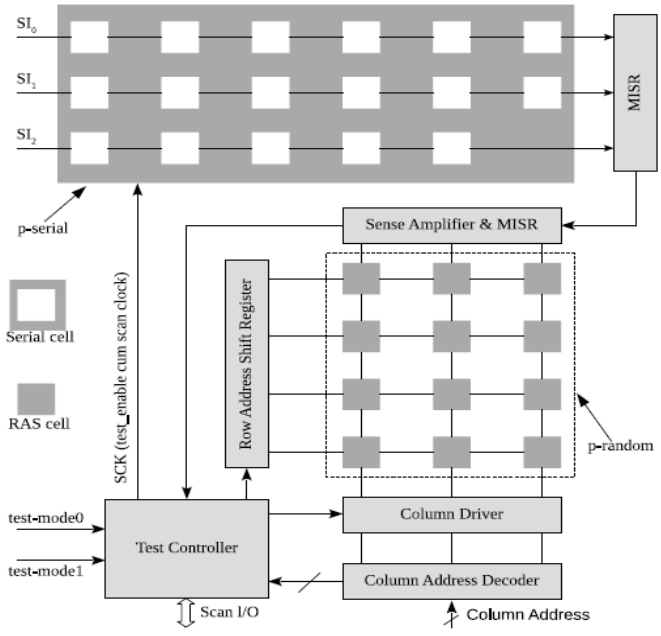

Fig.5. Mixed Mode scan design Architecture

Test Application*:* The functionality of the circuit is controlled by the two test mode control signals test-mode0 and test-mode1. Depending upon the states of the test control signals the circuit can operate in four modes. When both signals are 0, the circuit operates in normal functional mode. The remaining three states are mixed-mode (01), p-random-mode (10), and p-serial-mode (11). The test process starts with mixed-mode with p-serial and p-random loading/unloading the test stimuli/response concurrently. The shift operation in p-serial which is synthesized using the proposed scan flip-flop is done as explained in table 1.

The read/write operation in p-random is carried out in two steps. Note that the read/write operation in *RAS* corresponds to loading/unloading of test stimuli/response. First, the row enable signal is asserted to read the existing state of the *RAS* cells. The read operation is performed row by row using the sense amplifier. In the second step, only those *RAS* cells are written which corresponds to the care bits in present test vector, and for which the previous response bits differs from the present test vector's care bits. The *RAS* cells are written one after another in the column by column fashion using the column address pins. In case the loading /unloading of both p-serial and p-random finish in equal time the circuit is switched to functional mode to launch/capture of test stimuli/ response. In case, loading in p-serial completes before p-random, the circuit switches to p-random-mode. In this mode, the p-serial shift operation is stopped by holding the *SCK* signal at a constant high level. The write operation in the p-random is continued until all the test vectors care bits are written in the corresponding *RAS* cells. Once the write operation is complete, the circuit is switched to functional mode to apply the test vector and capture the response. In case, the p-random write operation finishes earlier that p serial loading the circuit enters in p-serial-mode. The p-random part is held in an inactive state, and the p-serial continues with the loading of test patterns. Once loading in p-serial is done, the circuit is switched to functional mode, and the test is applied. As explained in the preceding sections, the proposed scan cell is fully compatible with all the modes.

4. Experimental Results and Discussion

To approve the viability of the proposed check flip-flop in blended mode check structure condition, scaled ISCAS 89 benchmark circuits have been utilized. The benchmark circuits are up-scaled as far as size by duplicating a similar circuit module on numerous occasions. The circuits are blended utilizing Synopsys Structure Compiler for all the three DFT designs, i.e., different sequential sweep (MSS)

plan, PRAS structure, and Mixed mode check plan. The complete directing wire length (WL) figured by the device for all the three test plans is accounted for in Table I. As it very well may be seen from Table I, the full numerous sequential sweep design sets the least bound on the aggregate and normal wire length. Then again, the RAS design has the most elevated wire length as a result of which it has directing clog issue. The blended mode examine test engineering utilizes the best of both various sequential sweep and RAS design. The blended mode filter engineering gives a method for exchange off between equipment overhead and test time, test information volume, and test power. The steering wire length has been determined with two extraordinary number of test pins. The principal push results relate to the S38417 and S5378 benchmark circuits actualized with eleven outputs in pins. Then again, the subsequent column results compare to circuit execution with ten output in pins. It tends to be seen from Table I that the inter connect directing wire length additionally improves with the higher number of test pins. With a higher number of test pins accessible at the chip level the quantity of inward sweep chain increment which in turn lessens the sweep chain length or at the end of the day the number of sweep cell in an output chain. The decline in filter chain length diminishes the sweep way length. Thus, the generally speaking wire length lessens as the quantity of test pins increments. The most extreme rate decrease in complete wire length is roughly 21% for S38417 benchmark circuit.

Table.1 Routing Wire Length in Mixed, PRAS and MSS

Ckts	Layout Area(μm²)	Arch.	Total WL(mm)	AvgWL/net (μm)	%red
S38417	65149.30	PRAS	279.54	45.02	0.00
		Mixed	221.28	35.29	20.84
		MSS	167.63	28.37	40.03
	75929.06	PRAS	281.59	45.32	0.00
		Mixed	232.11	36.96	17.57
		MSS	179.17	30.71	46.37
S5378	7400.92	PRAS	29.52	28.72	0.00
		Mixed	26.74	26.60	9.42
		MSS	24.00	25.87	18.69
	8616.95	PRAS	29.43	28.69	0.00
		Mixed	27.30	27.87	7.40
		MSS	22.86	25.6	22.48

As clarified in Section II, in mixed mode scanned architecture, the SCK signal is utilized both as test control just as a low-recurrence check clock. Consequently, steering of SCK as a worldwide semi successive sign will present some region and force overhead. So as to examine the impact of output recurrence over the steering zone and force overhead SCK directing, complete spot and course on a couple of benchmark circuits with SCK recurrence changing from 10MHz to 100MHz. additionally, the recurrence of useful clock CP for directing was kept steady at 1GHz. It ought to be noticed that these numbers don't give the absolute steering region and force dissemination. The all out directing region and force rely on different factors, for example, sorts of steering metal layers utilized, the all out number of VIA's, the absolute length of metal wire utilized, and metal wire length utilized for a specific steering metal layer. It can be seen, that the territory and force overhead because of the directing of SCK as a low frequencies signal is marginally higher than the directing of SCK as an unadulterated combinational signal. In any case, it is a lot of lower than the steering overhead of the utilitarian clock signal CP. In this way, orchestrating what's more, directing the SCK as a low-recurrence clock signal is financially savvy. Additionally from the table, we see that there is a slight variety in cradles/inverters mean CP signal due to the stochastic idea of directing and arrangement.

5. Conclusion

We have proposed an output flip-flop structure which dispenses with the presentation punishment of the sequential sweep by evacuating check multiplexer from the useful way. The new output flip-flop is equipped for applying every single regular test and completely goes along with the ordinary business plan and test stream. Moreover, the proposed filter flip-lemon can be utilized both as a sequential output cell just as a RAS cell, in the blended mode check test. The blended mode filter configuration executed with proposed examine flip-flop shows a promising decrease in interconnect wire length, test information volume, and test application time.

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