Design of Wideband Low Noise Amplifier for Communication Applications

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Abstract – *The wireless standards are rapidly growing in recent years. Accordingly, user want low power dissipation, wideband, less cost, compact size wireless standards for future. Low noise amplifier (LNA) is one in all the foremost important block within the wireless transceiver RFIC design. The performance parameters of the LNA which incorporates Input/output impedance matching, noise figure, gain and linearity have tradeoff among them. The proposed design aim to balance the tradeoff among different performance parameters and improve performance of the LNA to form it suitable for future RF receiver. This paper presents a wideband low noise amplifier (LNA) operating in subthreshold region. The proposed CMOS low noise amplifier (LNA) can pander to different wireless channels appeared at the antenna simultaneously, because it is not only low-power energy-efficient but also wideband that can support multiple wireless standards (Bluetooth, Zigbee, ultra-wideband (UWB), etc). Wideband matching is obtained by employing a gate inductor-assisted impedance matching and low noise figure is obtained by current reuse feed-forward noise cancellation technique, respectively. As this paper uses 0.18-µm UMC CMOS fabrication technology, the proposed LNA draws 1 mA from 1.8-V supply and provides a voltage gain of 11-13 dB (taking into consideration a 6-8 dB loss in buffer) and minimum noise figure (NFmin) of 5 dB, with 3 dB bandwidth from 1.8 to 5.5 GHz.*

***Key Words*: LNA, subthreshold, current reuse feed-forward noise cancellation, gate inductor assisted impedance, complementary metal oxide semiconductor(CMOS), low noise**

1.INTRODUCTION

The demand of wireless communication applications push VLSI designer to continuous research in wireless transceiver RFICs design. Application of wireless communication is increasing exponentially. Different wireless standards like GSM, CDMA, UMTS, GPS, Wireless LAN (IEEE 802.11a/b/g), Bluetooth, ZigBee, LTE and WiMax are operate in numerous frequencies and having different modulation schemes. As per wireless communication users demand future smart phone should support all wireless standards with low power dissipation, less cost and compact size. So as to cut back power dissipation, complex interfacing, cost and area requirement of smart phone, future wireless receiver should have single wideband high performance RF frontend to support all wireless communication standards. The planning of LNA for future universal receiver remains a difficult task. The implementation of multi-mode multi standard receiver using multi transceiver which not only requires larger silicon area but also consumes more power and it's not suitable for battery operated device. Universal wireless architecture has wideband transceiver, which support multi standards wireless communication applications and reduce silicon area and power consumption. This paper aim to style wideband LNAs for next generation universal and Ultra wideband(UWB) system receiver.

2. LITERATURE SURVEY

At present, many low power consuming CMOS LNAs which use current-reuse technique [1], self-body bias [2], capacitive cross-coupling [3], etc., are reported. Each technique has its own pros and cons. This paper presents a wideband CMOS low noise amplifier(LNA) operating in subthreshold region, which is not only consume low power but also energy-efficient.

3. SUBTHRESHOLD UWB LNA

Fig-1 incorporates common gate stage followed by cascode CG-CS stage which is considered as a current reuse configuration. Buffer provides output matching. As the circuit operates in subthreshold region, biasing voltages are 550mV, 1.5V, 611m, 800m. In this circuit, gain boosting and feed-forward noise cancellation is obtained. L_{g1} provides wideband matching by reducing the dependency of transconductance g_m. Resistance R_{d1} is resistive. L_{d3} by resonating with the total drain capacitance of M_3, provides shunt peaking which inturn provide bandwidth extension. The resistance R_{d3} is in series with

L_{d3} which not only reduce the quality factor of the inductor, but also improve the low frequency gain.

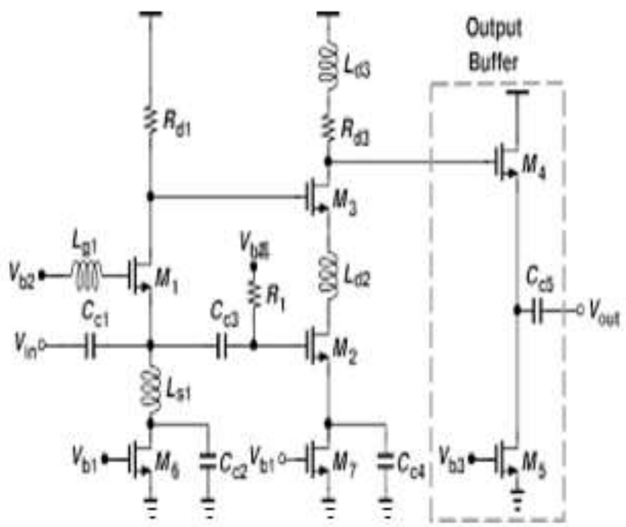

Fig-1: UWB LNA

Table-1: Component Values

$\left(\frac{W}{L}\right)_1$	$\left(\frac{W}{L}\right)_2$	$\left(\frac{W}{L}\right)_3$	$\left(\frac{W}{L}\right)_4$	$\left(\frac{W}{L}\right)_5$	$\left(\frac{W}{L}\right)_6$	$\left(\frac{W}{L}\right)_7$
$\frac{150\mu m}{0.18\mu m}$	$\frac{170\mu m}{0.18\mu m}$	$\frac{25\mu m}{0.18\mu m}$	$\frac{40\mu m}{0.18\mu m}$	$\frac{40\mu m}{0.18\mu m}$	$\frac{95\mu m}{0.18\mu m}$	$\frac{105\mu m}{0.18\mu m}$

L_{g1}	L_{s1}	L_{d2}	L_{d3}	R_{d1}	R_{d3}	R_1
2.5nH	9nH	3nH	8nH	700ohm	200ohm	1.2kohm
$C_{c1} = C_{c2} = C_{c3} = C_{c4} = C_{c5} = 5pF$						

3.1 Impedance Matching

LNA is the first stage in receiver to receive weak signals incoming from antenna and amplify it. Input impedance matching is very important parameter in LNA design for maximum power transfer from the antenna to LNA. S11 of two port network S parameter indicate ratio between reflected signal powers to the input signal power at port 1. S11 below -10 dB is desired. -10dB of S11 mean 10% of total input power reflected back. The proposed circuit provides S11 below -10dB within a 3dB bandwidth ranging between 1.8–5.5 GHz. Similarly, Output impedance matching is measured by S22 of S parameter.

3.2 Power gain

Performance parameter power gain is measured by S21 of S parameter. To improve strength of the weak received signals, S21 should be as high as possible. S21 of the proposed circuit float between 11-13 dB corresponding to the ratio of W/L.

3.3 Stability

In the high power gain MOSFET based amplifier design care have to be taken that the design remain stable in all input and output loading condition. A widely used metric for study of the stability characteristics based in the S parameters involves the use of the stability factor K, given by the expression,

$$K = \frac{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|}$$

where, $\Delta = S_{11}S_{22} - S_{21}S_{12}$,determinant of S parameter matrix. Value of K greater than unity and Δ less than the unity make system unconditionally stable.

From the expression for K, amplifiers with high power gain (S_{21}) require the feedback parameter S_{12} to be small. By reducing the gain at the output of the driver transistor, the cascode amplifier circuit enhances the stability, which makes the device more unilateral.

3.4 Noise Analysis

The noise in any amplifier or RF receiver circuit is characterized as thermal noise, flicker noise, shot noise, generation recombination noise, etc., Fig-1. Cancels the thermal noise and suppress the other noise sources.

Noise is measured by noise figure(NF), which determines the amount of noise added to the received RF signal. Noise figure is usually expressed in decibel(dB). For a good LNA design, noise figure must be as low as possible. The proposed LNA provides a NF of 5 dB.

Table-2: Comparison with other techniques

Techniques	3dB range	Gain	Noise Figure(NFmin)
Subthreshold	1.8-5.5 GHz	11-13 dB	5dB
Current reuse[1]	0.1-7 GHz	5.5dB	9dB
Self-body bias[2]	7-10 GHz	3dB	1.9-2.6dB
Capacitive cross coupling[3]	0.1-1.45 GHz		2.5dB

4.CONCLUSION

The proposed LNA draws 1 mA from 1.8-V supply and achieves a voltage gain of 11-13 dB (taking into account a 6-8 dB loss in buffer), minimum noise figure (NFmin) of 5dB, and 3 dB bandwidth from 1.8 to 5.5 GHz. Comparison of results with other techniques is tabulated. The proposed design can balance tradeoff among different performance parameters and can enhance the performance of the LNA to make it suitable for future RF receiver.

REFERENCES

[1] Mahdi Parvizi, Student Member, IEEE, Karim Allidina, Student Member, IEEE, and Mourad N. El-Gamal, Member, IEEE, "A Sub-mW, Ultra-Low-Voltage, Wideband Low-Noise Amplifier Design Technique," IEEE June 2015

[2] Rong-Fu Ye, Student Member, IEEE, Tzyy -Sheng Horng, Senior Member, IEEE, and Jian-Ming Wu,Member,IEEE, "Two CMOS Dual-Feedback Common-Gate Low-Noise Amplifiers With Wideband Input and Noise Matching," IEEE October 2013

[3] Li Ma, Zhi-Gong Wang, Senior Member, IEEE, Jian Xu, and N. M. Amin, "High-Linearity Wideband Common-Gate LNA with a Differential Active Inductor," IEEE April 2017