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HIGH SPEED APPROXIMATION ERROR TOLERANCE ADDERS FOR IMAGE PROCESSING APPLICATIONS

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Abstract: *Addition is the one of the basic arithmetic operations, which are used in many VLSI systems like microprocessors and application specific DSP architectures .The approximation error tolerance adders are efficient in terms of area, power and accuracy while considering the basic structure of adders. In this paper, proposes a design of adder, which improves the overall performance based on static segmentation and accuracy adjustment logic (AAL) methods. During this implementation SAET adder is meant using full adder and approximation full adder cells with reduced complexity at gate level. In this paper, the performance of 8 bit conventional and proposed adders are explained. Area, power and delay analysis are compared for various adders using approximation adder technique.*

KEYWORDS: Significance approximation(SA), Error tolerance(ET), Digital signal processing (DSP), Image blending, static segment adder(SSA), Accuracy adjustment logic (AAL) , VLSI .

1. INTRODUCTION

The functional unit of VLSI systems and application specific DSP architectures performance is totally depends upon adders. The filters are widely used in DSP for removing unwanted features from a signal in order to improve the quality of the signal and it is used in communication system applications such as echo cancellation, noise reduction, speech and waveform synthesis etc.. Adders are widely used in the different types of the digital filter applications. The design performance will be degraded, when adders are consumes large energy (or) processed as too slow. Approximation addition has been carried out for achieving area, power and speed improvements at the accuracy in the field. This paper proposes a design of approximation adder, which improves the overall performance based on static segmentation and (AAL) method to improve the accuracy derived from negating lower bytes of input operands. The content of the paper is organized as follows, Section 2 discuss about the conventional and error tolerant adder theory. Section 3 explains about the proposed significance approximation error tolerant carry select adder. Sections 4 presents comparison of simulation results and chapter 5 deals with image processing application using proposed SAET-CSLA. Finally conclusion.

2. CONVENTIONAL AND ERROR TOLERANT ADDERS THEORY

2.1 CONVENTIONAL 8 BIT CSLA

Ripple carry adder is that each adder has to wait for the arrival of its carry input signal before the actual addition starts. In carry select adder is to use blocks of two ripple carry adder, one of which is fed with a constant '0' carry in, while the other is fed with constant '1' carry in. Both blocks can calculate in parallel. Multiplexers are used to select the correct one of both partial sums of the carry in signal. The resulting carryout is selected and propagated to the next carry select block .for addition full adder is beneficial that have multiple bits in each of its operands. Three inputs are taken and produce a sum and a carryout as outputs[6,8,11,14]. Full adder logic has 13 basic logic gates (AND, OR and NOT gates), which are wont to implement the primarily gate level structure (2 Exor gates (2*5) +3) and 6 logic delays. The inputs have an equivalent weight 2i, the sum output features a weight of 2i, and therefore the carryout output features a weight of 2(i+1) . The truth table and k map minimization of full adder is shown Table 1 and Fig. 1 respectively. From k map, the minimized expression is obtained. The sum and carry expression of the logical gate implementation is shown in Fig. 2. Using Full adder truth table (Table 1), the approximation logic comparisons are done.

TABLE 1 TRUTH TABLE FOR FULL ADDER

Inputs			Conventional FA	
A	*B*	*C*	*SUM*	*CARRY*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig .1 KMAP MINIMIZATION OF FULL ADDER

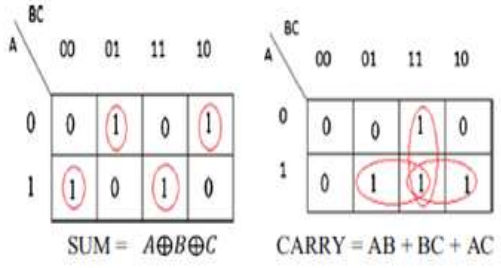
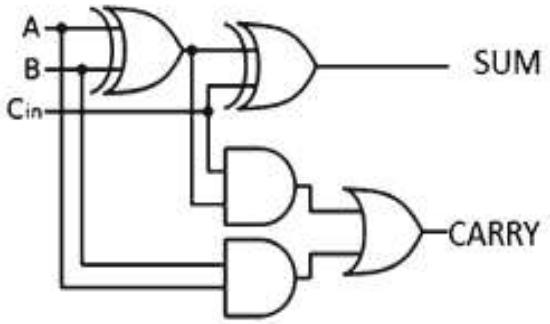


Fig .2 LOGIC IMPLEMENTATION OF FULL ADDER



2.2 8 BIT ERROR TOLERANT CSLA

Approximation adders are derived from accurate adders based on various approximation which have incorrect outputs for sum and carryout for more input combinations. The input is considered only with the uniform distribution for simplicity[5]. Approximation addition is used for low power and high speed circuit design. This technique specially developed for the DSP for increase the throughput (or)to reduce the power consumption in image processing systems .a lot of the design methods of the low power approximation adders were proposed in the literatures[5,16].some applications need an approximation adder to operate at high frequencies such as video processing .in this approximation full adder are constructed by modifying the conventional full adder in the gate level of carry signal is independent of carry input. Within the approximation logic, approximation is chosen since it gives minimum errors in comparison to other approximations. In Sum it shows only 2 errors and for carry, there is no error as shown in Table.2. K map minimization for approximation Full adder gate level implementation is completed and represented in Fig.3. Approximation Full adder logic has 2 errors in sum output and no error in carry output, where all the input bits are either '0's or '1's. Whereas for all other sum and carry values, there's no change in outputs

TABLE: 2 TRUTH TABLE FOR APPROXIMATION FULL ADDER

Inputs			Approximation FA	
A	*B*	*C*	*SUM*	*CARRY*
0	0	0	1 (Error)	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0 (Error)	1

Fig .3 K MAP OF APPROXIMATION FULL ADDER

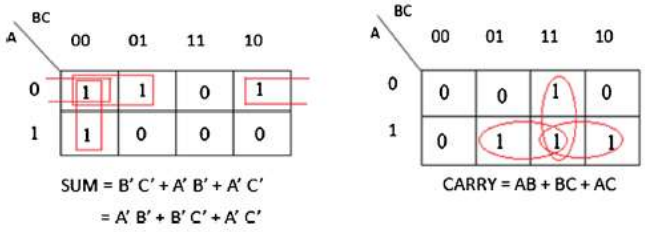
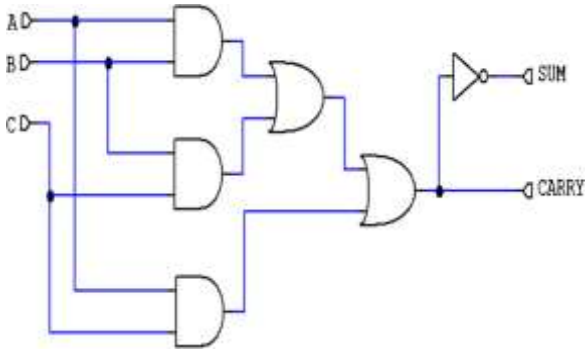


Fig.4 LOGIC IMPLEMENTATION OF APPROXIMATION FULL ADDER



Logic implementation of Approximation full adder shown in Fig.1.4, has 6 basic logic gates and 4 delays rather than 13 basic logic gates and 6 delays of conventional full adder. . When the approximation is applied, only the 2 combinations (000 or 111) of inputs end in error, all the remaining combinations are correct. When all the inputs are 1 then sum is an error (i.e., rather than 1 sum is 0) and when all the inputs are 0 then sum is a mistake (i.e., rather than 0 sum is 1).

3. PROPOSED SIGNIFICANCE APPROXIMATION ERROR TOLERANT ADDER

Error-tolerance (ET) deals with the use of defective circuitry that occasionally produces an errors. This proposed significance approximation error concept is an integration of conventional CSLA and ET-CSLA for the system which improve accuracy of the output results. Error can be tolerated at some threshold for approximation result in approximation adder [7, 11].

3.1 SEGMENTATION AND AAL

Segmentation based ETA the input operands are divided into accurate part and inaccurate parts. The 8 bit adder is divided by 4bit accurate part and 4 bit inaccurate part. Normal addition is used for higher order bits of the input operands .ripple carry adder is choose as accurate part. In accurate part divided into carry free addition block and control block. If input values are '1', control signal is high. If both values are different (or) '0', normal XOR is performed and proceeding the operation. AAL is enable for higher order segment selection of input operands and lower order segment is selected for SSA. Accuracy increased by static segment method with AAL.

Addition techniques for SSA,

Two 8-bit input operands are:

Augend (A) = 1000 0101

Addend (B) = 0000 0001

Addition (conventional sum) = 134

The addition technique used in SSA method is given in steps as follows:

Step 1: Segmentation

A = 1000 01011111 1111 100001012 (4 bit)

B = 0000 0001 1111 1111 000000012 (4 bit)

Step 2: 4-bit Addition

Now we have; Aseg ½ 1012

Bseg ½ 0012

Let Z = Aseg + Bseg =0101 + 0001 +1(Accuracy adjustment logic) Thus,

Z ({C,Sum}) = 00111 (5 bit)

Step 3: With AAL output ,the addition is expanded and ones are padded.

Thus, SSA Out =001111111 (9 bit) = 135

OE= |134-135|=1

OE Tolerance (%) = (1/134) *100% = 0.01%

Accuracy = (1 - (1/134)) *100%= 99.9%

3.2 ACCURATE PART

In this part, the traditional 8 bit conventional Carry select adder is applied to preserve its correctness since the upper order bits play a crucial role than lower order bits for better accuracy.

3.3 INACCURATE PART

In this part, 8 bit ET-Carry select adder is chosen for inaccurate a part of circuit since it's simplest one for many power saving and requires less hardware circuitry. The proposed SAET-CSLA adder has gates which are considerably fewer than conventional CSLA and slightly quite ET-CSLA. In 8 Bit dual ripple carry accurate part, adder requires (2 RCA* 4FA in each RCA) 2*4*13 = 104 gates, inaccurate a part of adder requires (1 RCA* 4 AFA in each RCA) 1*4*6 = 24 and for multiplexer it requires gates. Hence a neighborhood reduction of 19.81 what's obtained for proposed SAET-CSLA adder in comparison with conventional CSLA.

3.4 ACCURACY CALCULATION

The addition should actually yield from two operands, if normal arithmetic has been applied. The various terminologies utilized in this work are as Follows:

1. **Overall error (OE)** is the difference between the outputs of conventional adder (Rc) and approximation adder (RE).
2. **Percentage of error Tolerance** = [OE/R c]*100% (the results are represented in decimal numbers).
3. **Accuracy (ACC)** of an adder indicates the correctness of the adder output for a particular input.

ACC = (1-(OE/ Rc))*100%.

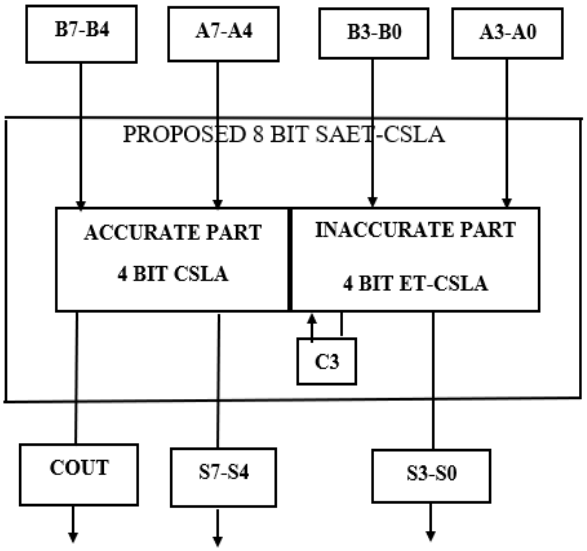
4. **Minimum Acceptable Accuracy (MAA**) is defined as some errors lower than a threshold value are allowed to exist at the output of adder to meet the requirement of whole system.
5. **Acceptance Probability (AP):** The probability that the adder accuracy is above the minimum acceptable accuracy.
6. **Minimum Accuracy** of an adder is higher than the minimum acceptable accuracy.

The total error generated are often computed by the subsequent equation [1]:

Overall Error (OE) = | Rc– Re | ----------[1]

Where, Re is that the result obtain from SAET-CSLA adder and Rc denotes the right result. OE, OE Tolerance, Accuracy = 99:927% (Accuracy of an adder with reference to the 2 input operands) are derived.

Fig.5 8BIT PROPOSED SAET-CSLA



4. SIMULATION RESULT COMPARISION

4.1 SIMULATION RESULT

Xilinx ISE design suite 14.7 software is used to design the conventional and proposed adders for analyze the performance. The proposed SSA adder accuracy is greatly increased by using AAL and static segment method. The worst case accuracy range can varies from 50% to 94%. SSA achieves 13.84%, 50.06%, and 13.13% computational speed improvement when compared to existing conventional CSLA, conventional RCA. It consumes more area (8 LUTs) than existing ETA. Whereas, the proposed SSA consumes less energy using multiplexer switching. In this proposed adder design, from 0 to 255 range of input operands are playing a important role in the contrast digital signal(high, low and medium) are represented. But for improved ET-CSLA is kind of 50% accurate for upper input operands. In SSA design, it considered all the input operands to achieve high performance and this design can be better solution to get high accuracy for all the error tolerant applications like image blending, defect detection machine in vision applications, contrast stretching in image processing applications , audio and video processing, etc. One of the applications is implemented and presented in the following section. That the error tolerance performance of the adder for all input operands are greatly improved using SAET-CSLA.

Fig.6 8 BIT CARRY LOOK AHEAD ADDER SIMULATION OUTPUT

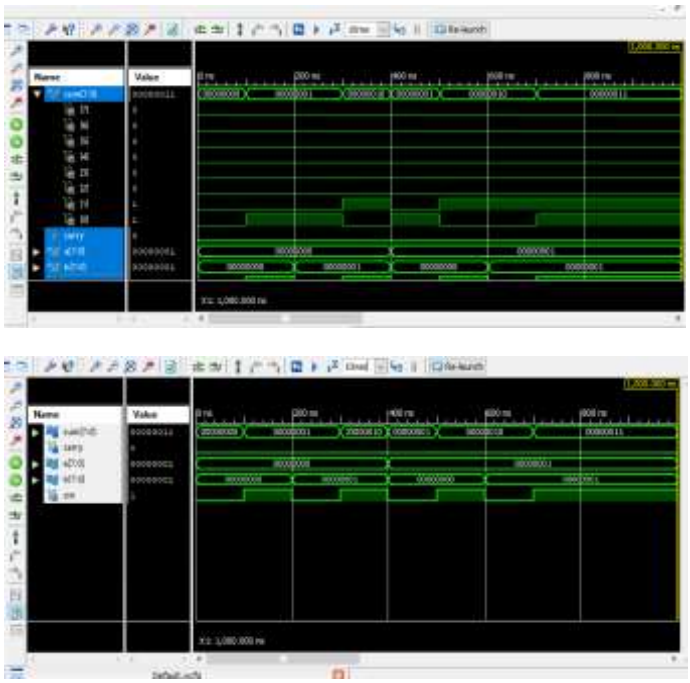


Fig .7 8 BIT APPROXIMATION CARRY LOOK AHEAD ADDER

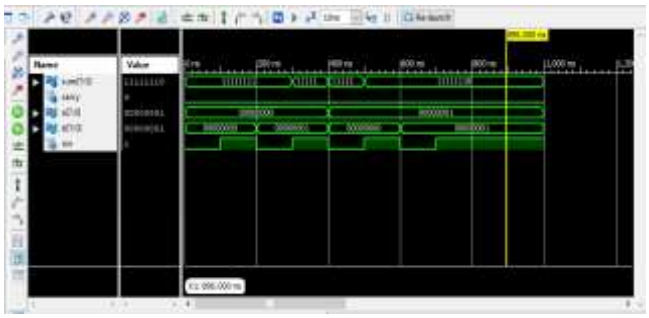


Fig .8 8 BIT RIPPLE CARRY ADDER SIMULATION OUTPUT

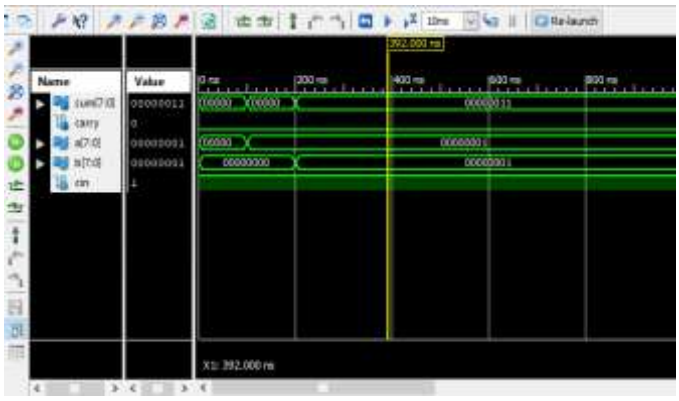


Fig .9 APPROXIMATION RCA SIMULATIONS

OUTPUT

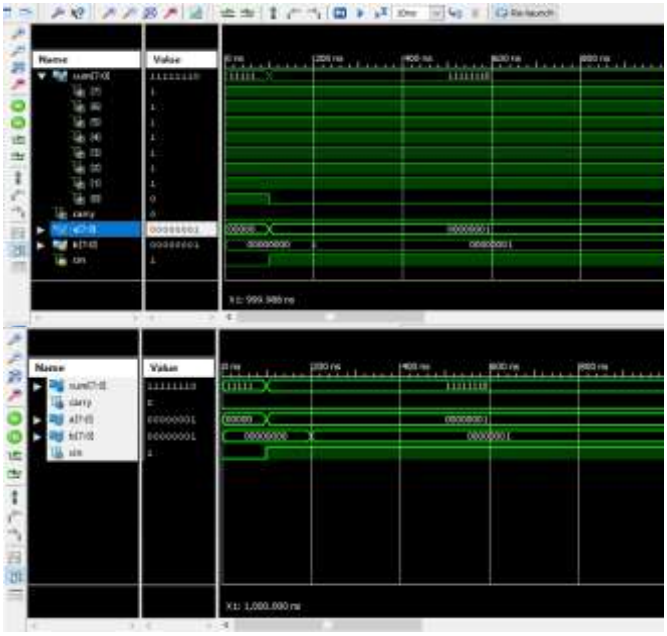
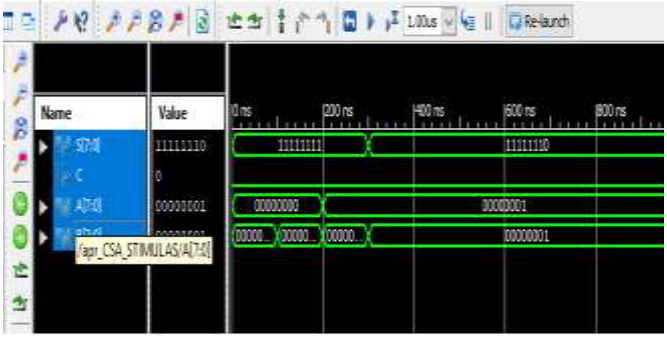


Fig .10 8 BIT CSA SIMULATION OUTPUT

Fig 11 8BIT APPROXIMATION CSA OUTPUT



From the simulation result the report analysis are tabulated for conventional and error tolerant approximation adder of RCA, CLA and CSLA adders .This technique reduces the propagation delay and power consumption .And also improves the overall performance accuracy of the circuit.

TABLE . 3 COMPARISON OF ADDERS FOR CSLA

Adder	Area (gate count)	Delay (ns)	Power (mw)
Conventional CSLA	424	24.686	87
ET-CSLA	228	18.851	79
Proposed SAET-CSLA	340	22.187	84

TABLE .4 COMPARISION OF ADDERS

8 BIT ADDERS	NO OF 4 LUTS	NO OF OCCUPIED SLICES	NO OF IOBS	TOTAL CPU COMPLETION TIME	MAXIMUM COMBINATIONAL PATH DELAY	AREA MAP COMPLETION	RESOURSE USAGE
CLA	16	12	26	0.23secs 12.78secs	13.203ns	10 to 2secs	890ms
ACLA	12	7	26	0.00secs 0.27secs	10.245ns	14to 14.16 secs	756ms
RCA	16	9	26	0.00secs 0.22secs	13.203ns	12to 12.16 secs	796ms
ARCA	17	12	26	0.00secs 0.30secs	11.040ns	13.00 to 12.77 secs	650ms
CSA	18	10	25	2.00 secs 2.20secs	10.061ns	18.00 to 17.64 secs	820ms
ACSA	18	11	25	3.00secs 3.16 secs	10.530ns	20 to 20.25 secs	796ms

5. FUTURE APPLICATION OF PROPOSED SAET-CSLA IN IMAGE PROCESSING

In image processing image blending operation is performed supported image addition principle, but different weights are to tend for images in order that it gives a sense of blending or transparency. As per the equation in below the images were added

$$G(X,Y)=(1-\alpha)F1(X,Y)+\alpha\, F2(X,Y)$$

where, α is that the blending ratio which determines the influence of every input image within the output. By varying the values of α from 0 to 1, a cool transition between one image to a different is performed. This operator forms a mix of two input images of an equivalent size. Almost like pixel addition, the worth of every pixel within the output image may be a linear combination of the corresponding pixel values within the input images. The coefficients are user-specified and before combining them, the ratio is defined by scaling each image. These proportions are applied such the output pixel values don't exceed the utmost pixel value. Image blending using 8 bit proposed SAET -CSLA f1 and f2 are the 2 input images. In some applications f2 also can be a continuing, thus allowing a continuing offset

value to be added to one image. A can either be a continuing factor for all pixels within the image or are often determined for every pixel separately employing a mask. The dimensions of the mask must then be identical with the dimensions of the pictures. Architecture of image blending is shown in fig.12. F1 and f2 are the 2 input images (255 × 255) are separately given to 2 different partition blocks. By a multiplication factor the partitioned images are multiplied. One among the pictures is multiplied by the factor α and other by the factor(1-α). The multiplied images are then added with the proposed 8 bit SAET-CSLA. A is that the variable which determines the measure of blending of output resolution. Image blending application is performed using proposed SAET-CSLA and therefore the input and outputs are shown in fig.13. Verilog code is employed to construct the adders and therefore the image blending operation is performed in mat lab using proposed SAET-CSLA by varying the intensity factor to urge the high accuracy images. Variation in α alters the foreground and background pixels of blended image parameters like sharpness, brightness and contrast. From the fig.5.2. It's noted that increasing the worth of α enhances the standard of the blended image.

Fig. 12 ARCHITECTURE OF IMAGE BLENDING USING PROPOSED 8 BIT SAET-CSLA

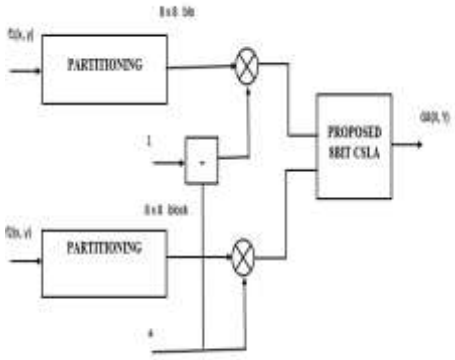
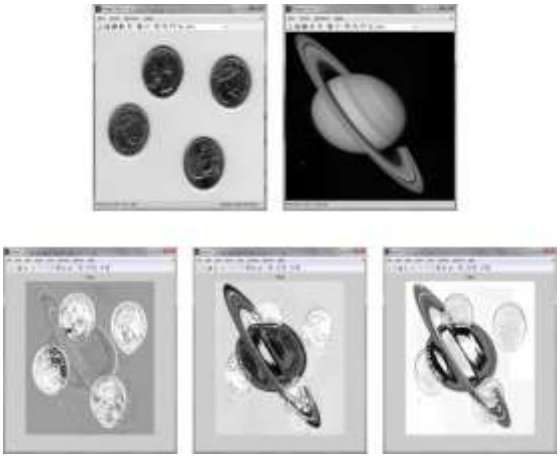


Fig. 13 F1 AND F2 IMAGES BLENDING AND FOR $\alpha = 0.2, 0.6$ AND 0.8



6. CONCLUSION

SAET-CSLA adder structure is applicable to general purpose design, with a couple of exceptions. The necessary for the quick response for increasingly the large data sets, the adder should be high accuracy and fast. During this proposed adder, minimum error tolerance is obtained by conventional full adder logic within the accurate part so as to extend the accuracy at the foremost significance level. The error tolerant adder is meant using approximate full adder cells with reduced complexity at the gate level within the inaccurate part. 8 bit conventional, ET and proposed 8 bit adders are implemented. For all possible 216 input combinations, performance analysis is completed and the average error computed smaller amount than I chronicles. The error of the proposed adder are often reduced by analyzing the relation between the input bit patterns and approximation logic. The SAET for CSA design has possible solution to attain high accuracy image outputs for all the range of input operands in image processing applications. The ET-CSLA can attain an improvement in both the facility in consumption also as well as speed and area efficient performance. By accuracy adjustment logic and static segment method the accuracy and speed are increased in the proposed adder. Performance analysis is carried out and the worst case error is computed for all the possible input combinations. When compared with conventional ETA, proposed method of adders consumes less energy and notable high speed with computational accuracy error 0.64%.so thus proposed method of approximate adders will result in higher quality for all the kinds of error tolerant applications.

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