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REALIZATION OF POWER OPTIMISED CARRY SKIP ADDER USING AOI LOGIC

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Abstract:- The binary adder is the critical element in most digital circuit designs. The more important parameters in VLSI design are power consumption, area and speed. And since the binary adder is exist in most digital circuit designs. In this paper a carry skip adder (CSKA)based AND-OR INVERTER (AOI)logic is proposed in order to reduce area and power consumption. The proposed adder is simulated by Xilinx and compared with the conventional CSKA based multiplexer logic

Key words-Carry skip adder (CSKA), AND-OR-INVERTER, Xilinx Simulation.

1-INTRODUCTION

While designing an adder, lot of constraints comes into picture. The tradeoff between speed and size being the most important one. The most basic adder has a very small area and is very easy to implement. But the delay involved in obtaining the output is very huge. Hence the new designs came to picture. But in current age the power consumed by the device is also a very important constraint.

Hence designing an adder which is very close in meeting all these requirements is a very important. Apart from the design, the technology we use to design the adder also plays a huge role in the speed and size of the adder. **A**dders are a key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been low-power/energy consumptions, which is a challenge for the designers of general purpose processors.

One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect. Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions.

2- Full adder using MUX.

The Full adder using multiplexer is shown below in fig 1.

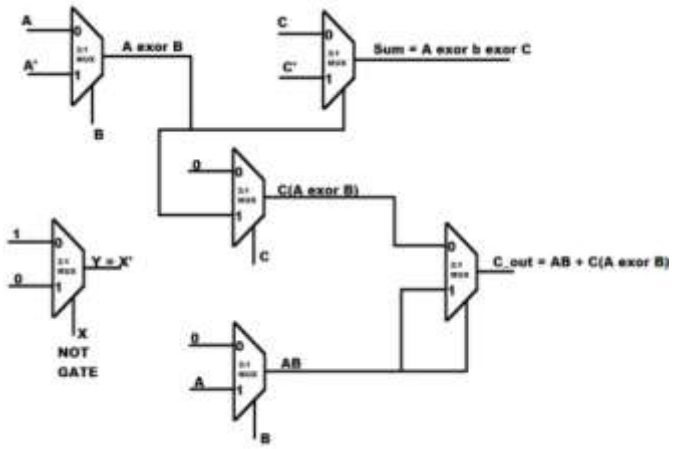

Fig1: full adder using Mux

The sum and carry of a full adder is given by:

$$Sum=A\oplus B\oplus C$$

$$C_{out}=C_{in}(A \oplus B)+AB$$

$$Y=A\bar{S}+BS$$

3- **Carry Skip Adder Using Mux**

The carry skip adder using mux is shown in Fig 2 .

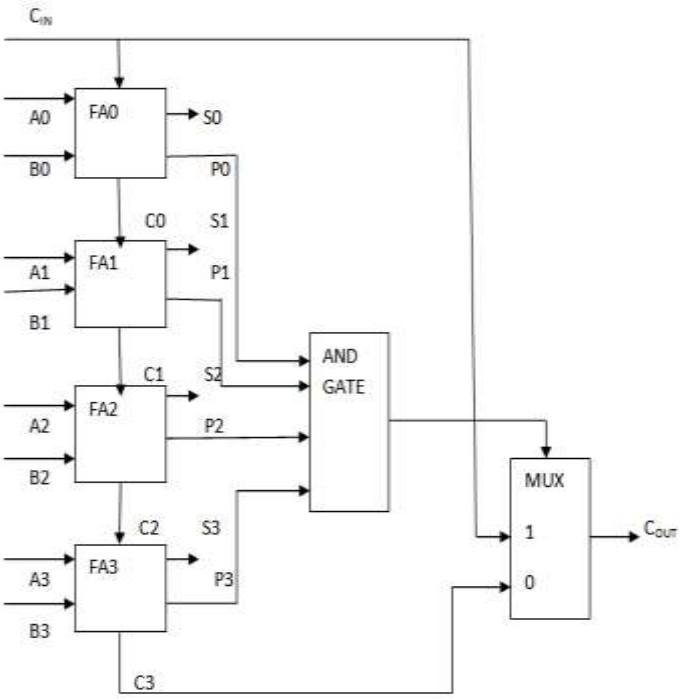

Fig2: Carry skip adder using Mux

In carry skip adder four full adders are cascaded, the calculations of sum and propagation are :

Sum s=a xor b xor cin.

Propagation p=a xor b.

And also done the same process done in the ripple carry adder for generating carry(c3) of final full adder.Propagation outputs of the four adders are p0,p1,p2 and p3 .And all the propagated outputs are given to the one AND gate. The output of AND gate acts as a selection line to the multiplexer, cin and c 3 are inputs to mux circuit ,this is nothing but skip logic.

In carry skip adder four full adders are cascaded, same as the ripple carry adder and every full adder calculating sum and propagation.

Sum s=a xor b xor cin.

Propagation p=a xor b.

And also done the same process done in the ripple carry adder for generating carry(c3) of final full adder.Propagation outputs of the four adders are p0,p1,p2 and p3 .And all the propagated outputs are given to the one AND gate. The output of AND gate acts as a selection line to the multiplexer, cin and c 3 are inputs to mux circuit ,this is nothing but skip logic.

4- The CSKA based and-or-inverter

The proposed 4bit carry skip adder using and-or-inverter is shown in fig 3

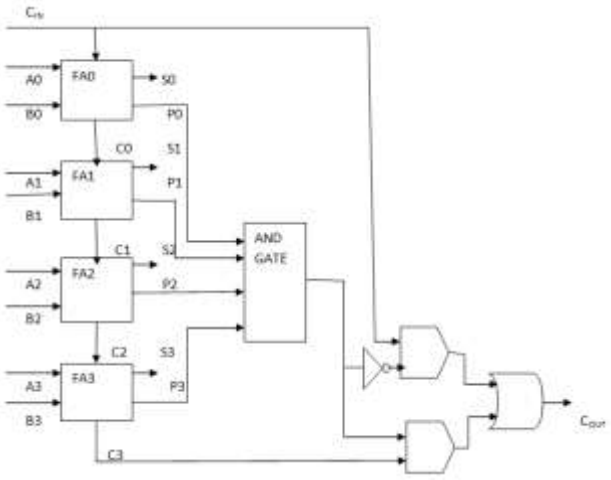

Fig :3 Four full adders using and-or-inverter

For example let us take 4 bit carry skip adder The inputs of carry skip adder is 'a' and 'b'. In carry skip adder four full adders are cascaded, same as the ripple carry adder and every full adder calculating sum and propagation.

Sum s=a xor b xor c_{in}.

Propagation p=a xor b.

for generating carry(c_3) of final full adder. Propagation outputs of the four adders are p0,p1,p2 and p3 .And all the propagated outputs are given to the one AND gate. The output of AND gate is connected toAOI logic circuit this is nothing but skip logic.

Initially c_{in} =0,what the carry given to the next stage of either c_{in} or c_3. We are having two cases of carry production, those are best case and worst case.

In case of best case let us assume a=1010 and b=0110

P0= 0 xor 0= 0.

P1= 1 xor 1= 0.

P2= 0 xor 1 =1.

P3 =1 xor 0 =1.

P0,p1,p2 and ,p3 are given to the and gate , the output of and gate is p= (0&0&1&1)=0.

A1=Cin and p=1&&0=0.

A2=C3 and p=1&&1=1.

4-Simulation and Results

The simulations are done by Xilinx version 12.3 using 32bit CSKA based Mux fig 4,and 32bit CSKA based and-or-inverter fig 5 and the simulation results are shown below.

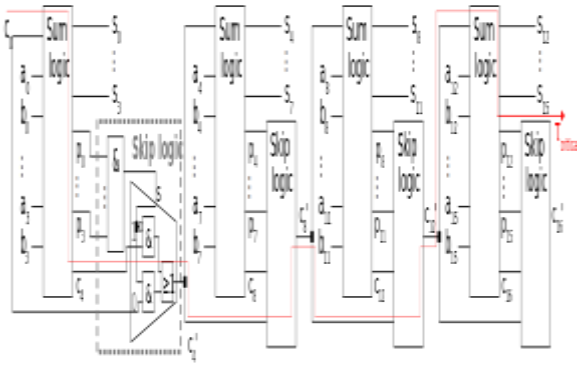

Fig 4: 32bit CSKA USING Mux

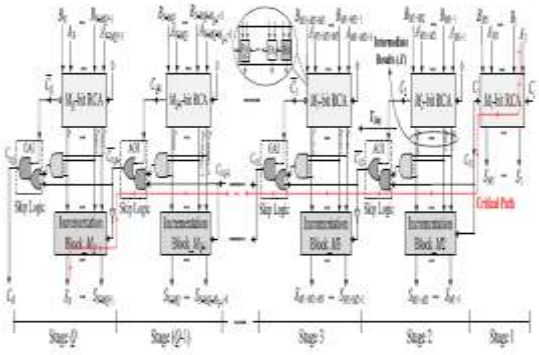

Fig5 : 32bit CSKA using and-or-inverter

4.1- CSKA based Mux simulation:

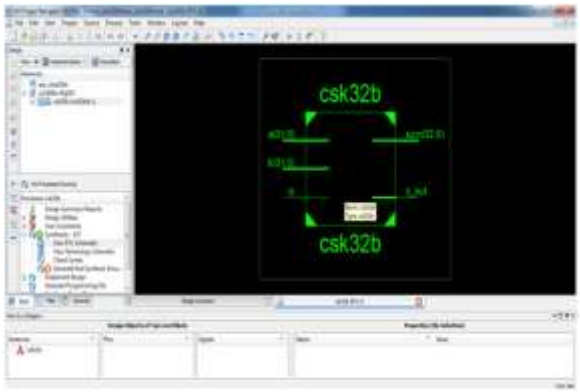

Fig6.1: RTL schematic view

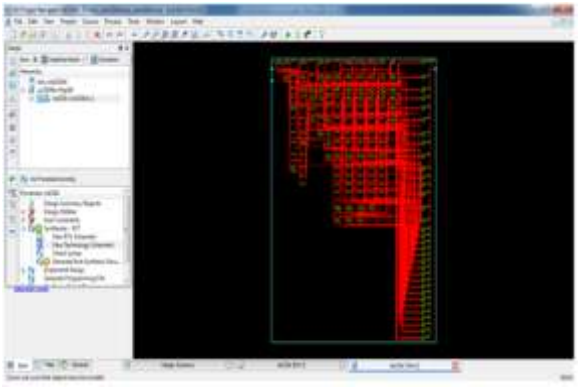

Fig6.2: view technology schematic

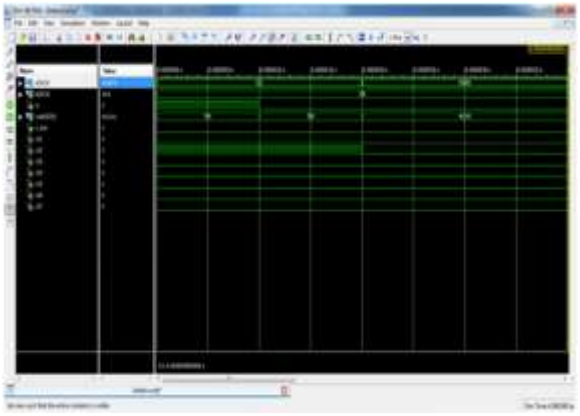

Fig6.3: simulation results using Mux

4.2 CSKAbasedand-or-inverter simulation

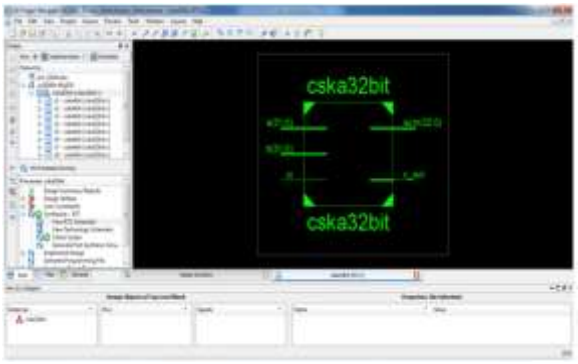

Fig6.4: RTL Schematic View

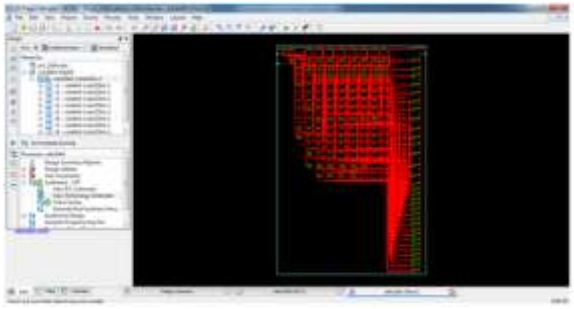

Fig6.5: View Technology Schematic

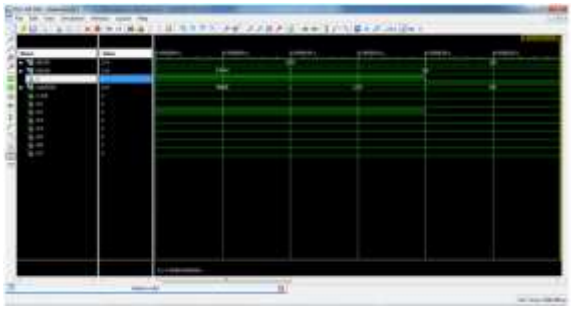

Fig6.6: simulation results using and-or-inverter

5. Conclusion

In this paper, The carry skip adder based and-or-inverter (AOI) is proposed and simulated using Xilinx.The simulated results showed that it has less area and low power consumption compared with traditional one and it can be used in digital circuit design where the area and power consumption are critical.

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