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COMPARISON OF VEDIC, WALLAC TREE AND ARRAY MULTIPLIERS.

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Abstract - *Multiplications are the most important and crucial operation in any system. They are done through the process of repetitive addition. Since speed is necessary in any factor therefore multiplication must also be done in a faster way so that they are utilized properly for a faster result. This paper gives a detailed explanation on all three multipliers and compares them accordingly-In this paper, three various multiplication methods are considered and simulated. Three structural multipliers such as Vedic, Wallace tree and array multipliers are compared and their output is shown through the FGPA. For comparison, the results of multipliers are synthesized and simulated using XILINX.IS E.14.5 tool .Later the comparison is concluded by evaluating their utilization of the device.*

Key Words: Vedic multiplier, Wallace tree multiplier, Array, multipliers, XILINX, adder, VerilogHDL

1. INTRODUCTION

Multiplication operation play a very important role in micro processing, DSP and other communication applications. They produce partial product by adding them .For a high speed processing, a high speed multiplier is required. Therefore an ideal multiplier must be designed in terms of high speed, low power consumption, low delay and area. Multiplier is a device which is capable multiplying two given numbers. They are known as the binary adders. In this process each of the bits are multiplied with their respective multiplicand and the corresponding products are obtained. These products obtained are *added to get final result. In this paper two numbers are multiplied using three different multiplier techniques.*

In this paper, three multipliers are used .They are :

- *VEDIC MULTIPLIER*
- *WALLACE TREE MULTIPLIER*
- *ARRAY MULTIPLIER*

Consider two 8-bit number,

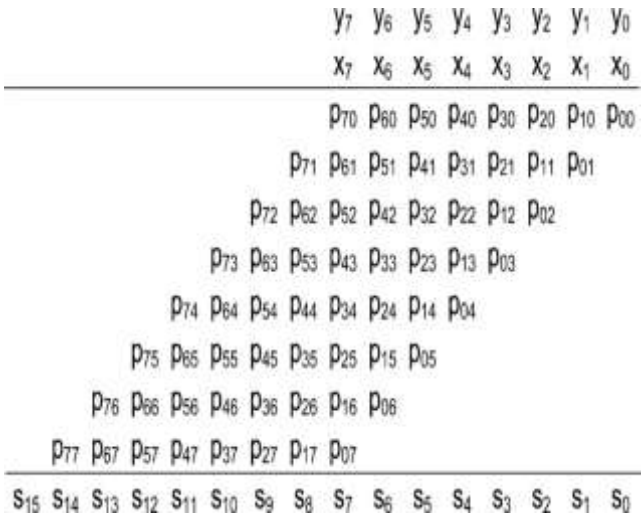

Fig-1: Multiplying *two numbers.*

from the fig. 1.it can be observed that multiplication is just a lot of addition involved. Hence these multipliers are designed using full adders and half adders.

2. VEDIC MULTIPLIER

Vedic multiplier is based on 16 Vedic sutras which describes natural way of solving whole range of mathematical problems. Out of 16 Vedic sutras the Urtdhva-Trayakbhyam is the general multiplication formula applicable to all mathematical cases which means vertically and crosswise. Vedic is the oldest mathematic system which is very well known for their fastest technique in calculations. It explains various mathematical element such as the trigonometry, geometry, quadratic factors and calculus. It produces product and sum in a single step. Their calculations are

done parallel which makes Vedic the fastest multiplier. As the number of bits increases in a Vedic multiplier the timing delay decreases greatly when compared to other multiplier.

2.1. Algorithm

- Divided the Multiplicands A and B, where first bit indicates the MSB and other LSB.
- Now represent A and B as Am, Al and Bm, Bl respectively.
- These inputs are multiplied likeAm x Bm, Am x Bl, Al x Bl Al x Bm

- *Products* can be obtained by the partitioning method and applying the basic building blocks.

2.2. Advantage

- It increases the speed of the system
- It provides better efficiency
- They reduce time delay as well as path delay in the multiplier
- It requires smaller area when compared to other multipli*er.*

2.3Disadvantage:

- The system becomes complex when the multiplication is complex
- For reduction of delay it needs additional circuitry which means increasing the chip *area.*

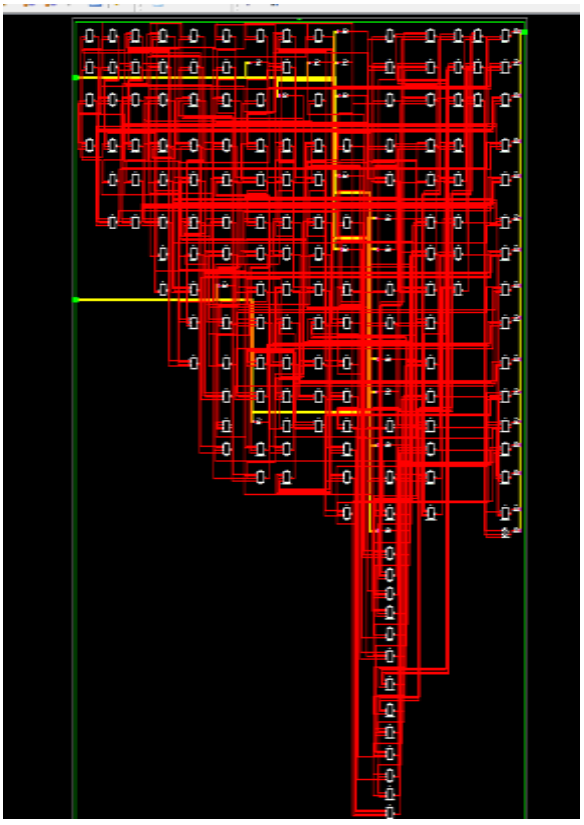

Fig-2:*RTL SIMULATION*

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	72	3584	2%
Number of 4 input LUTs	126	7168	1%
Number of bonded IOBs	32	141	22%

Fig-3: *UTILIZATION TABLE*

3. WALLAC TREE

Wallace tree multiplier is an efficient implementation of digital circuit. It multiplies two integers and the given numbers are multiplied in structural format . Chris Wallace, an Australian scientist in 1964 introduced parallel multiplier architecture. Wallace tree multipliers are considered to perform efficiently but they are hard to implement. Although they are considered to be the fastermultiplier than simple array multiplier.

They include:

1. Partial Product Generation

2.. Partial Product Reduction

3. Partial Product Addition

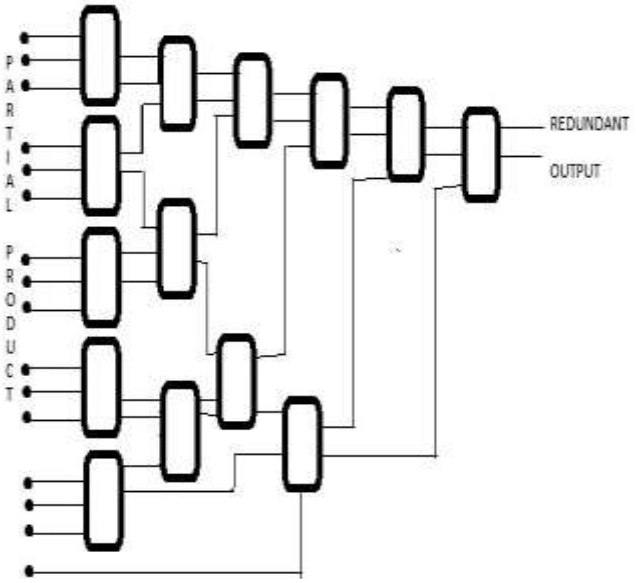

Fig-4: *BLOCK DIAGRAM*

3.1. Advantage

- *The multiplier provides the system with minimum complexity .*

- *They are easily scalable.*
- *Pipeline is done very easily.*
- *They are multipliers with regular shape.*
- *They are easy to place and route.*

3.2. Disadvantage

- *They have more delay*
- *The system consumes high power.*

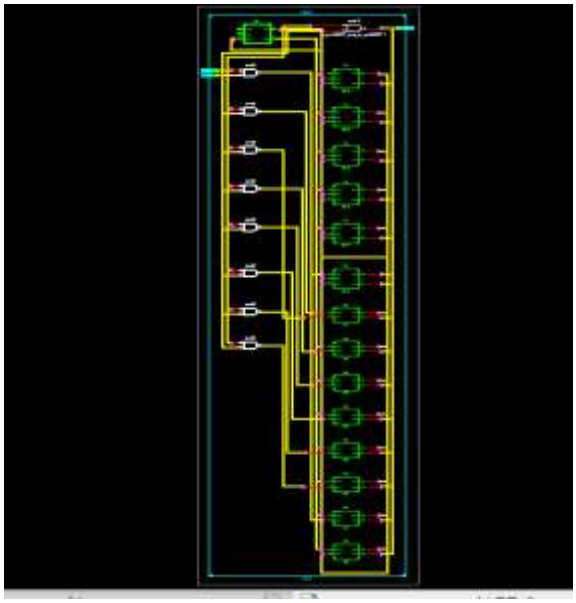

Fig-5: *RTL SIMULATION*

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	72	3584	2%
Number of 4 input LUTs	126	7168	1%
Number of bonded IOBs	32	141	22%

Fig-6: *UTILIZATION TABLE*

4. ARRAY MULTIPLIER

The array multipliers are the layout of combinational multipliers. More digital gates resulting in large chip area. Although it utilizes more gates the performance be easily increased using pipeline technique. The add and shift algorithm is followed in array multipliers. The partial products are generated and shifted according to bit orders and addition operation take place. The result for multiplying two numbers is obtained by using AND logic gate that gives bit of the product .Consider 8X8 bit multiplication with A= X0 X1 X2 X3 X4 X5 X6 X7 and B= Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 and the result is given by S

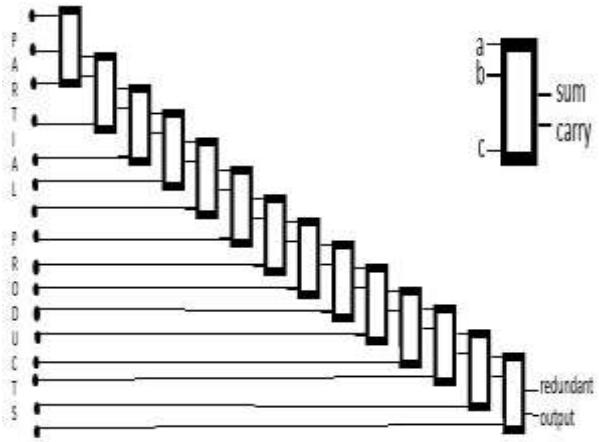

Fig-7: *BLOCK DIAGRAM*

4.1. Advantage

- *The multiplier provides the system with minimum complexity.*
- *They are easily scalable.*
- *Pipeline is done very easily.*
- *They are multipliers with regular shape.*
- *They are easy to place and route*

4.2. Disadvantage

- *They have more delay.*
- *The system consumes high power.*

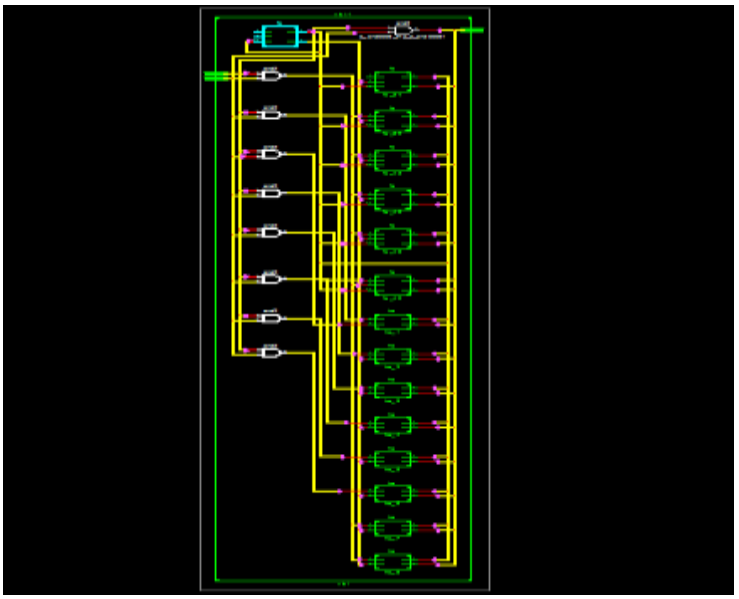

Fig-8: *RTL SIMULATION*

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	89	3584	2%
Number of 4 input LUTs	155	7168	2%
Number of bonded IOBs	32	141	22%

Fig-9: *UTILIZATION TABLE*

5. FPGA IMPLEMENTATION

The final procedure is to implement them in a hardware kit. With the help of XILINX tool the code is burnt into the FPGA it and the output can be verified using them. Hence the result is done in both hardware and software using XILINX . Here Initially a0 is in on state (a0=1) and b1 is in on state (b1 =1) and other values set as „0" that will be displayed in data input switches. The output is displayed in LED Indicators. There are 8 LED Indicators.X0 (1) is in on state(X0(1) =1) and others will be in offstate. The Outputs are X0(0), X0(1), Sum2 (0), Sum2 (1), Sum2 (2), Sum2 (3), Cout 1, Cout 2.

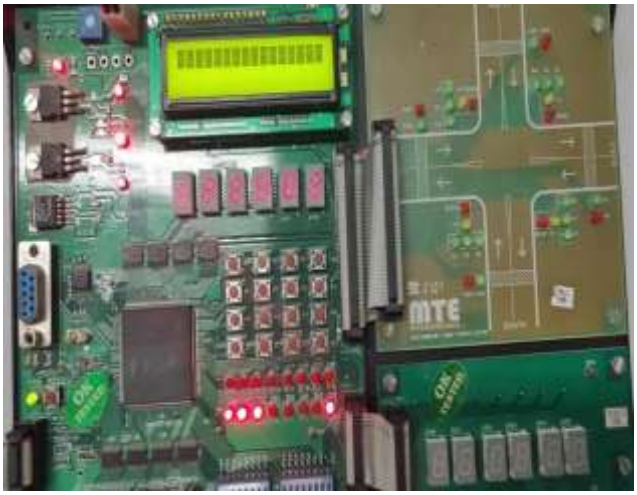

Fig-10: *FPGA OUTPUT*

6. SIMULATIONS RESULT:

To generate output two inputs are given to a multiplier:

A="157"(in decimal number system) B="129"(in decimal number system)

Output ="20253"(in decimal number system)

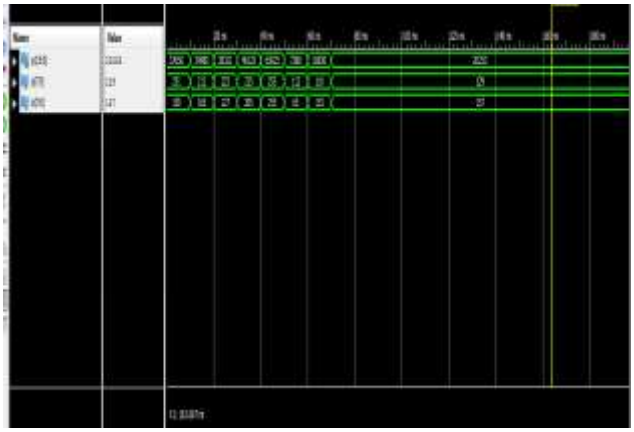

Fig-11: *SIMULATION RESULT*

7. EXTENSIVE APPROACH

Finite Impulse Response (FIR) filters are widely utilized in Digital Signal process (DSP) applications because of their stability and linear-phase property. In nowadays state of affairs, low power consumption and fewer space area are the foremost necessary. Several finite impulse response(FIR) filter styles aimed toward either low space or high speed reduced power consumption area are developed. This results in style where FIR filter with the advantage of high efficiency and high speed performance. The implementation of an FIR filter wants three basic building blocks. They're Multiplication, Addition and Signal delay. Multipliers consume the foremost quantity of house in a FIR filter style within the system thus it'll have an effect on the performance of the FIR filter. Here, typical multipliers unit is replaced by lesser variety of adders and lesser steps. As a results of that, they become a more efficient system and thus used in digital processes, image processes and so on.

8. CONCLUSION

The implementation of 8x8 multipliers such as Vedic multiplier, Wallace tree multiplier and array multipliers are done. It is observed that delay in each multiplier vary respective to their design and hence it is found that Vedic multiplier uses less delay than any other multipliers and considered to be the fastest in its performance. Also the utilization by Vedic multiplier is less than other multipliers. Therefore in this paper it is verified that Vedic multiplier is the most suitable technique to implement complex mathematical problem.

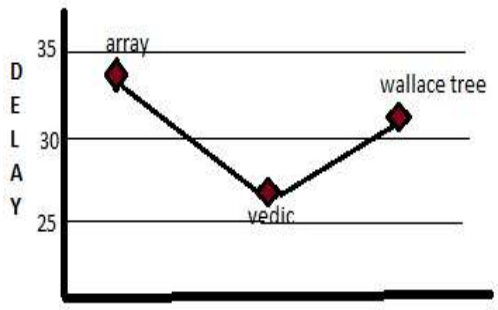

Fig-12: *COMPARISON GRAPH*

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