DESIGN AND ANALYSIS OF KOGGE STONE ADDER USING APPROXIMATE COMPRESSOR

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ABSTRACT: *The major role of electronics device is to provide low power dissipation and compact area with high speed performance. Among the major modules in digital building blocks system, multiplier is the most complex one and main source of power dissipation. Approximate Computing to multiplier design plays major role in electronic applications, like multimedia by providing fastest result even though it possesses low reliability. In this paper, a design approach of 16bit Wallace Tree approximate multiplier with 15-4 compressor is considered to provide more reliability. The 16*□*16 Wallace tree multiplier is synthesized and simulated using Xilinx ISE 14.5 software.*

Index Terms—5-3 compressor, Approximate 15-4 compressor,Kogge stone adder

1. INTRODUCTION

MICROPROCESSORS and Digital Signal Processors (DSP) are playing a big role to handle the complexity of digital signal. About 95% of the processors within the market are supported digital signal. Digital signal processors lookout of convolution, correlation and filtering of digital signal. Multipliers, shifters and adders are mainly wont to accomplish these tasks. Among the three modules, multiplier is that the most complex one. Multipliers take longer and consume higher power than other two modules. Multipliers have three phases

• Generation of partial products

• Reduction of partial products

• Final stage addition.

Reduction of partial products takes much time and power within the multiplier. Many techniques were proposed to scale back the critical path within the multiplier. Among them, the utilization of compressors in partial product reduction stage is that the hottest . Compressors are basic circuits which are made from full adders or half adders to count the amount of "ones" within the input. Several compressors are required within the partial product reduction stage. Various compressors like 3-2, 4-2, 5-2 and 5-3 were proposed by researchers within the last 20 years.These are useful only the dimensions of multiplier is little . 16 □ 16, 32 □ 32 bit multipliers require large size of compressors. High order compressors provide better leads to terms of power and speed. But it consumes more area than low order compressors. of these techniques perform the precise computation and modules produce the right result. Accuracy of the module/device is usually 100% in exact computing. But exact computing has one major drawback. it's impossible to optimize all the parameters of the circuit in exact computing. However, exact computing isn't essential for each application. There are some applications like image processing and multimedia can tolerate errors and supply meaningful results. Inexact (approximate) computing techniques became popular due to its low complexity and fewer power consumption.

Inexact computing produces reasonable result, even it's low accuracy. In approximate computing, the worth of error rate (ER), error distance (ED) and normalized error distance (NED) play a crucial role to calculate the ultimate output. Error rate is given by variety of erroneous outputs over the entire number of outputs. Error Distance is that the arithmetic distance between an erroneous output and therefore the correct one. Normalized Error Distance is that the ratio of mean error distance over all inputs by maximum input of the circuit. Several approximation techniques were proposed for adders and multipliers. From central point to the foremost significant bit (MSB) is named accurate and to the smallest amount significant bit (LSB) is named inaccurate a part of adders. Inaccurate computing in MSB side causes large error. the traditional addition rule is applied in accurate part whereas a special method of addition takes place in inaccurate part.

Output "sum" value is calculated normally when anybody of the operand value of adder is "0". When both operands are "1", "sum" value are often fixed as "1" from that bit position to least significant bit. this system is employed to attenuate the error distance of the adder.

2. EXISTING SYSTEM

2.1 DESIGNS OF APPROXIMATE 5-3 COMPRESSORS

In this section, four designs of a 5-3 approximate compressor are presented. 5-3 compressor has five primary inputs (X0, X1, X2, X3, and X4) and three outputs (O0, O1, and O2). This compressor uses the counter property. Output of the compressor depends on number of ones present at input. This proposed compressor also called as 5-3 counter. In this paper, we have called this module as a compressor because this module compresses five bits into three bits. We have chosen 5-3 compressor because it is a basic module for 15-4

compressor. Error rate and error distance of each design are considered.

Design 1

In this design, initially output O2 of 5-3 compressor is approximated. Logical AND between inputs X3 and X2 matches with accurate output O2 of the conventional 5-3 compressor with an error rate of 18.75%. The following expressions show design 1 of 5-3 approximate compressor.

$$O_2' = X_3 \bullet X_2$$

$$O_2 = (X_0 \bullet (\sim (X_0 \oplus X_1)) + X_2 \bullet (X_0 \oplus X_1) \bullet (X_3 \bullet (\sim (X_0 \oplus X_1 \oplus X_2 \oplus X_3)) + X_4 \bullet (X_0 \oplus X_1 \oplus X_2 \oplus X_3)$$

$$O_1 = (X_0 \bullet (\sim (X_0 \oplus X_1)) + (X_2 \bullet (X_0 \oplus X_1)) \oplus (X_3 \bullet (\sim (X_0 \oplus X_1 \oplus X_2 \oplus X_3))) + (X_4 \bullet (X_0 \oplus X_1 \oplus X_2 \oplus X_3 \oplus X_4)))$$

$$O_0 = X_0 \oplus X_1 \oplus X_2 \oplus X_3 \oplus X_4$$

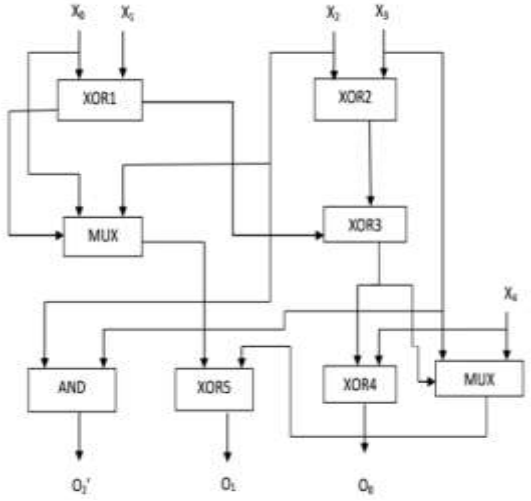


Fig1: Initially output O2 of 5-3 compressor is approximated

Design 2

In this design, O2, O1 are approximated and O0 is kept as the same as original expression. Error distance of all the error cases is either -2 or +2. From the truth table, it can be noted that pass rate of O2 is 87.5% when O2 alone is replaced with O2 in a 5-3 compressor. Similarly, pass rate of O1 is 75% when compared with the O1 output of the 5-3 compressor. Expression for O2 and O1 are modified to get the minimum error distance. The overall pass rate of this design is 75%. The output of the compressor differs only in eight input cases. In this design, the critical path is between input X0 and output O0. Four XOR gates are involved in the critical path. This design has least critical path than other proposed designs.

$$O_2' = X_4 \bullet [X_0 \bullet (\sim (X_0 \oplus X_1)) + (X_2 \bullet (X_0 \oplus X_1))]$$

$$O_1' = X_4 \oplus [X_0 \bullet (\sim (X_0 \oplus X_1)) + (X_2 \bullet (X_0 \oplus X_1))]$$

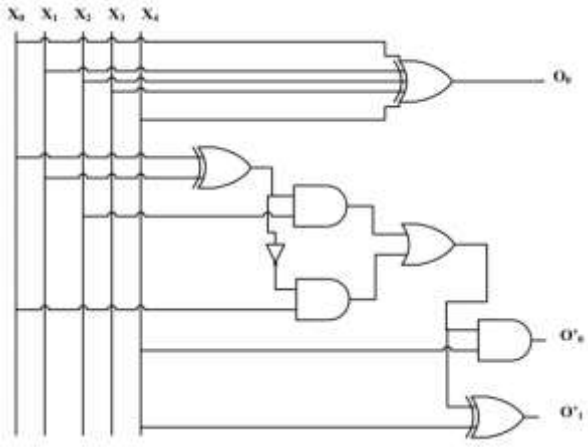


Fig 2: Logic diagram of design 2 approximate 5-3 compressor.

2.2 MULTIPLIER DESIGN

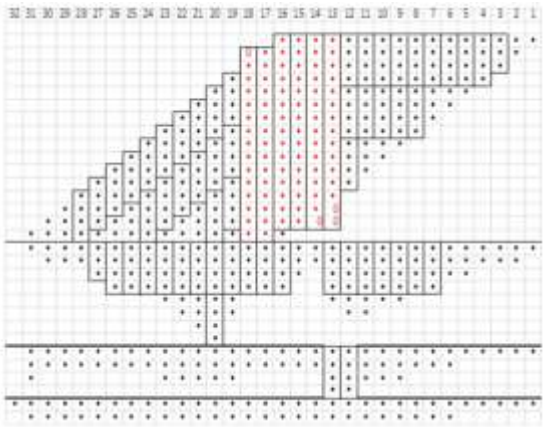


Fig3: Design of 16 × 16 multiplier

In this section, design of 16 × 16 multiplier is presented. Four approximate multipliers are designed using the proposed four 15-4 compressors. In addition to this, one accurate multiplier and four other approximate multipliers are considered. Approximate multipliers using the proposed approximate 15-4 compressors are compared with the accurate 16 × 16 multipliers with accurate 15-4 compressors and also with other multipliers designed using various other approximate compressors. Figure shows the design of 16 × 16 bit multiplier using 15-4 compressor where, each dot represents one partial product. Six 15-4 compressors are used to design one multiplier in the partial product

reduction and finally four multipliers are designed. In figure, rectangular boxes indicate the use of 15-4 and 4-2 compressor in the multiplier. 15-4 compressors are used in the multiplier from 13th column onwards. Column number 13 of the multiplier has only thirteen partial products. Two zeros are added in that column to make use of the 15-4 compressor. Similarly, one "0" is added in 14th column. Along with 15-4 compressors in the multiplier other accurate compressor like 4-2 and half, full adders are used for partial product reduction. Approximate compressors are used in 13th, 14th and 15th column of multipliers. Use of approximate compressors in most significant part would produce a larger error rate. Design 1 of 15-4 approximate compressor is used in multiplier 1. Similarly, design 2, 3 and 4 of 15-4 approximate compressors are used in multiplier 2, 3 and 4 respectively. In accurate multiplier, all accurate 15-4 compressors are used along with accurate 3-2 and 4-2 compressors. Accurate 4-2 compressors, half and full adders are used in second and third stage of partial product reduction tree. In final stage, parallel adders are used to compute the final result.

3. PROPOSED SYSTEM

3.1 WALLACE TREE MULTIPLIER

3.1.1 15-4 COMPRESSOR

A compressor is simply an adder circuit. It takes a number of equally-weighted bits, adds them, and produces some sum signals. Compressors are commonly used with the aim of reducing and accumulating a large number of inputs to a smaller number in a parallel manner. They are the important parts of the multiplier design as they highly influence the speed of the multiplier. Their main application is within a multiplier, where a huge number of partial products have to be summed up concurrently. For high speed applications like DSP, image processing needs several compressors to perform arithmetic operation. A compressor adder provides reduced delay over conventional adders using both half adders and full adders. Here the representation as 'N-r', in which 'N' denotes as the number of bits and 'r' denotes as the total number of 1's present in 'N' inputs. The compressor reduces the number of gates and the delay with reference to other adder circuits. The inner structure of compressors avoids carry propagation. Either there are not any carry signals or they do arrive at the same time of the internal values. Compressors are widely used in the reduction stage of a multiplier to accumulate partial products in a concurrent manner. In this part it is considered the design of 15-4 compressor by using with approximate 5-3 compressors. This compressor compresses 15 inputs (C0-C14) into 4 outputs (B0-B3). The 15-4 compressor consists of three phases. The first phase has five full adders, the second phase uses two 5-3 compressors and finally the 4-bit kogge stone adder. In this compressor design, approximate 5-3 compressor is preferred over accurate 5-3 compressors.

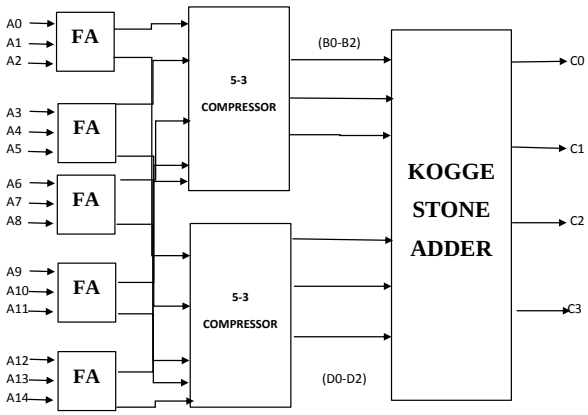


Fig4: 15-4 COMPRESSOR

3.1.2 5-3 Compressor

The 15-4 compressor consists of 5-3 compressor as a basic design. The 5-3 compressor utilizes five primary inputs namely X0, X1, X2, X3, X4 and produces three outputs namely O0, O1, O2. In this compressor, the presence of number of 1's at the input decides the output of compressor and also uses counter property.

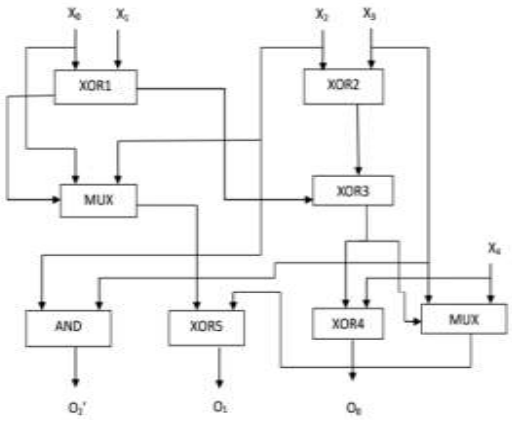


Fig5: 5-3 Compressor

3.2 Kogge Stone Adder

It is basically a parallel prefix adder. This type of adder has the specialty of fastest addition based on design time. It is known for its special and fastest addition based on design time. By using the ith bit of given input, the propagate signals 'Pi' and generate signals 'Gi' are calculated.

Similarly, these generated signals produce output carry signals. Therefore by minimizing the computation delay, Prefix Adders are mainly classified into 3 categories. A. Pre- processing B. Generation of Carry C. Final processing.

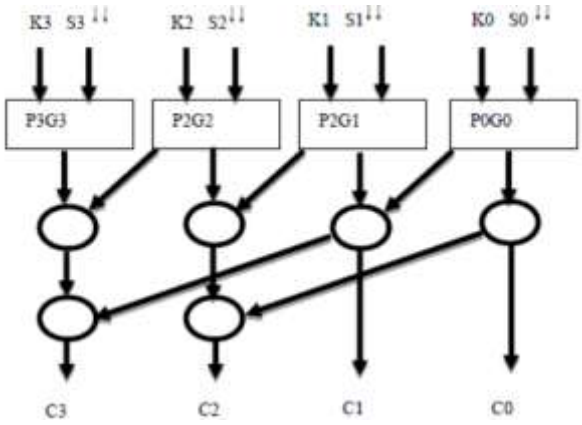


Fig6: Kogge Stone Adder

KSA is a parallel prefix form carry look ahead adder, it is widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits The complete functioning of KSA are often easily comprehended by analyzing it in terms of three distinct parts.

There are three stages of the computation in PPA.

- ✓ Pre processing.
- ✓ Prefix.
- ✓ Final computation. **PRE-PROCESSING**

In this stage, generate and propagate signals are given by the equations.

- ✓ Pi = Ai XOR Bi
- ✓ Gi = Ai AND Bi

3.2.1 GENERATION OF CARRY

- In this stage, carries are calculated with their corresponding bits and this operation is executed in parallel manner.
- Carry propagation and generation are used as intermediate signals. The logic equations for carry propagate and generate are shown below

- ✓ G = Gi OR (Pi AND Pj)
- ✓ P = Pi AND Pj

3.2.2 FINAL PROCESSING

- In final processing, the sum and carry outputs bits are computed for the given input bits and the logic equation for the final processing stage is given by

- ✓ Si = Pi XOR Ci-1

  Ci = Gi

3.3 SOFTWARE REQUIREMENTS

3.3.1 XILINX ISE Design Tools:

Xilinx ISE is that the planning tool provided by Xilinx. Xilinx would be virtually identical for our purposes.

3.3.2 VERILOG -LANGUAGE:

VERILOG -LANGUAGE is used as programming language.

4. OUTPUT:

4.1 DEVICE UTILIZATION SUMMARY:

multiplier16x16 Project Status (02/14/2020 - 13:15:03)			
Project File:	KSA.ise	Parser Errors:	
Module Name:	multiplier16x16	Implementation State:	Synthesized
Target Device:	xc6slx9-3tqg144	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	1 Warning (1 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	507	5720	8%
Number of fully used LUT-FF pairs	0	507	0%
Number of bonded IOBs	65	102	63%

Fig7: Area utilization summary

4.2 RTL SCHEMATIC:

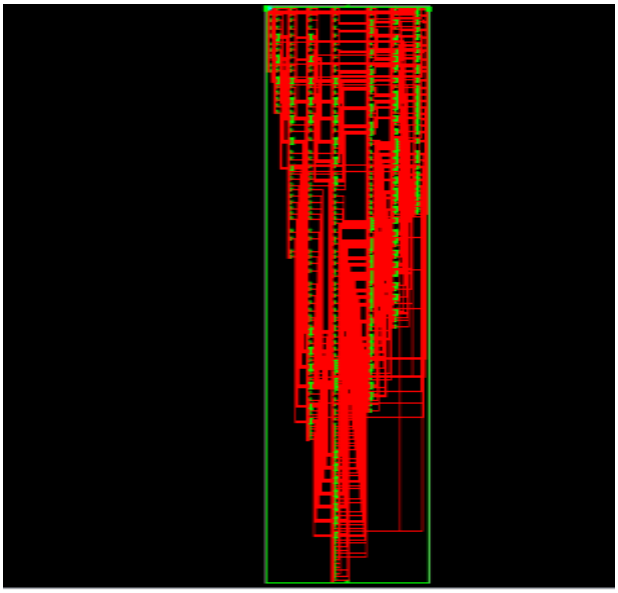


Fig8: RTL SCHEMATIC DIAGRAM

4.3 OUTPUT WAVEFORM:

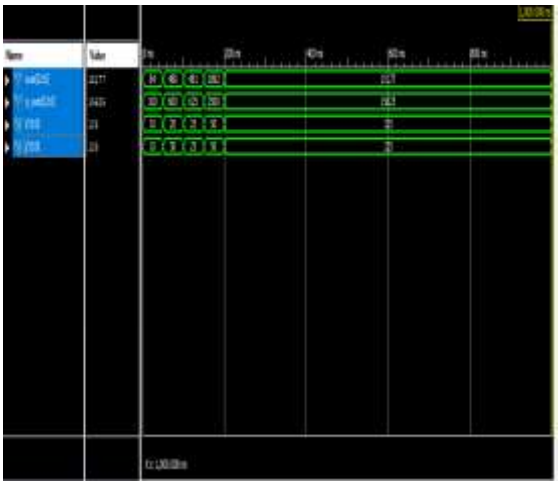
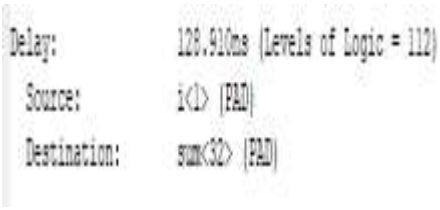


Fig9: OUTPUT WAVEFORM

4.4 TIMING ANALYSIS:



5. CONCLUSION

The approximate 16×16bit Wallace tree multiplier using 15- 4 compressor architecture has been designed and synthesized using on Spartan 6 XC3S100E board and simulated in Xilinx ISE 14.7. The performance of proposed Multiplier with kogge stone adder is compared with the same architecture of multiplier using parallel adder. It can be inferred that 16×16 multiplier architecture using 15-4 compressor with kogge stone adder is faster compared to multiplier with parallel adder. In future the performance of the proposed multiplier can be improved and applied in applications like video and image processing.

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