ANALYSIS OF POWER CONSUMPTION IN GLITCH FREE DUAL EDGE TRIGGERED FLIPFLOP

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Abstract - *In the field of VLSI designing, in order to achieve high performance and low power consumption, Dual edge triggered methodology is the most preferable methodology by the research workers. In comparison with the Single edge triggered (SET), the Dual edge triggered (DET) provides the same throughput at half of the clock frequency. This helps to reduce half of the power consumption and thereby reducing the Total system power consumption. In this paper, the proposed design is, a low power glitch free advanced Dual Edge Triggered Flip Flop (DETFF). The proposed design, DETFF is constructed by using the combination of C-element circuit and 2P-1N structure. If any error affects one of the structures, then it is nullified by the other one structure. To limit the input loading, the two circuits are combined to contribute the transistors connected to the input. This DETFF has used an internal dual feedback structure. The presented DETFF reduces the area and average power consumption and gain the higher speed of the system. Analysis of the temperature impact on power and delay at different supply voltages has also been done.*

***Key Words*: Clock distribution network; Dual edge triggered; Glitches; Power consumption; Power Delay Product.**

1. INTRODUCTION

In VLSI designing, the flip-flops are widely used for information storage. Device's performance and fault tolerance capability are affected by the flip flop's speed, power consumption and reliability. Consequently, it is necessary to design the flip-flops for minimum power consumption, propagation delay, area and maximum reliability with highest fault tolerance capability. Device scaling minimizes the supply voltage and device capacitances and circuit becomes more sensitive to the glitches. The electron hole combinations take place when particles touch the drain side of a MOSFET. The opposite biased electric field induces a drift transient current.

Transient fault is the voltage transient as a result of the collected charge. This fault may be formed by the prior combinational circuit glitches. By supply voltage scaling, low power consumption may be achieved efficiently. Power consumption because of the glitches cannot be neglected as the portion of total power consumption varies from 9% to 38%.The designing of energy efficient circuits is one of the hard challenges for the research workers. Previous research papers presented latch configurations which have reduced the average power consumption and also reduced power delay product (PDP).

The clock distribution network may accounts 45% of the total system power. Clock network consumes excess power; so, it is required to minimize the total number of clocks. To minimize the number of clocks, the true single phase clock (TSPC) approach has been recommended with the basic registers. To minimize the clock power consumption, the frequency of the clock can be scaled down, without modify the system throughput by sampling the input data on both of the rising and falling edges of the clock. The DET approach minimizes the half power consumed due to the clock network system. Although DET circuits have more complexity in comparison with the SET circuits however this can be more energy efficient.

In this paper, the existing designs are discussed in part II. The proposed DET-FF design is given in part III. Result and Analysis are given in part IV and the conclusion is given in part V.

2. EXISTING DET-FF DESIGNS

Dual edge triggered flip flop provides the equivalent data rate like single edge triggered flip flop at the 50% of the clock frequency, which minimizes the power consumption. Fig.1 shows a dual edge triggered flip flop to overcome the built in clock overlap challenge, by using TSPC circuits instead of an inverted clock and make clear the point of clock overlapping by using the TSPC circuits and an internal two-fold feedback design. The Dual Data Rate Flip Flop (DDR-FF) has a reduced clock load because of its easy structure, reduced activity factor and its hard edge quality factor. A robust LM_C DET-FF by using C-elements, where the straight clock pulses used to latch the data for the minimize of clock dynamic power consumption without any other pulse generator structure. This flip flop configuration gives the additional robust solution for dual data rate (DDR) flip flops due to absence of complications in it with less transistor count.

Fig. 2 shows the LG_C configuration which is upgraded with common latch MUX dual edge triggered flip flops, because of this fact, flip flops internal node data never changes with the changes in the input. The LG_C configuration presented improvement in the energy dissipation. The LG_C dual edge

triggered flip flop is glitch resistant, designed by three C-element circuits, which are two internal latches and one output latch, with the inverting topology because of the transistor level implementations.

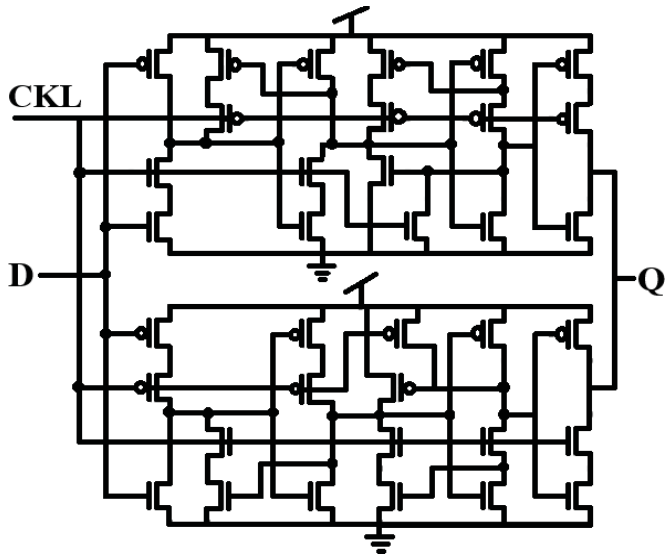

Fig- 1: TSPC-DET-FF

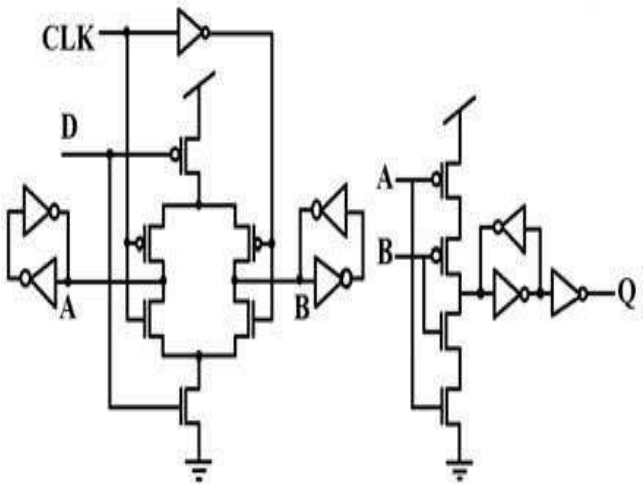

Fig- 2: LG_C-DET-FF

Fig. 3 shows the low power glitch resistant dual edge triggered flip flop design (D1-DET-FF) that minimizes the power consumption and delay and expands the efficiency and speed of the system. The design is constructed by using the combination of C-element structure and 2P-1N circuit. In D1-DET-FF configuration, if any glitch changes the data of one structure then it is nullified by the other one structure. To limit the input burdening, the two structures are combined to share the transistors connected to the input. In this design an internal two-fold feedback circuit is used.

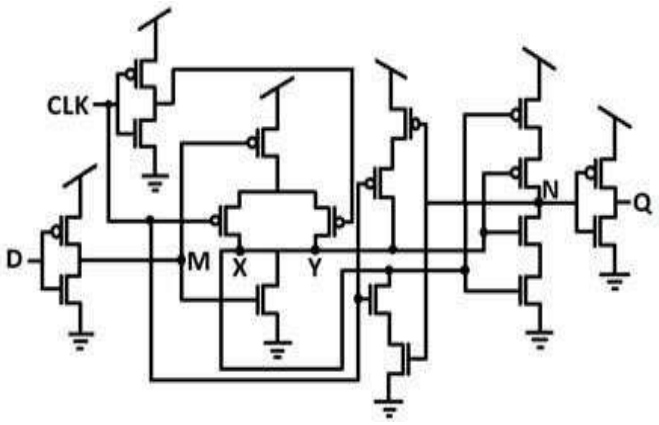

Fig- 3: D1-DET-FF

To reduce the switching activity, in most cases, the C-element circuits are used. The C-element design has the different aspect that when it's both inputs are equivalent, thereupon output switches to its input values; when the inputs are not equivalent, thereupon its output goes to the high impedance situation it means output will be in its past situation.

The 1P-2N circuit is different from the C- element structure:

1) When the inputs are not equivalent then the output may not go to the high impedance situation.

2) The C-element circuit has four transistors, but 1P-2N structure has three transistors only.

3. PROPOSED DESIGN

The main motive of the research workers is to get small area, low power and high speed in VLSI designing. So many techniques have been considered by the research workers in VLSI applications. We have designed a glitch free advanced DET-FF design, shown in Fig. 4.

Existing DET-FF designs are constructed by using the C-element circuits only. The presented glitch free DET-FF is a robust low power glitch free design and designed by the mixed combination of 1P-2N and C-element circuits that can work accurately at low voltage supply. It provides the totally glitch free output that can improve the system efficiency. The presented model consumes less power and provides glitch free output. The working procedure of this design is as follows: I, the glitch either filter out or propagate to the output Q. II, if glitch propagates to the output Q, then it is filtered out through the feedback path. Here, we just clarify how this design can avoid the glitches that can occur at the input node D from the prior combinational designs.

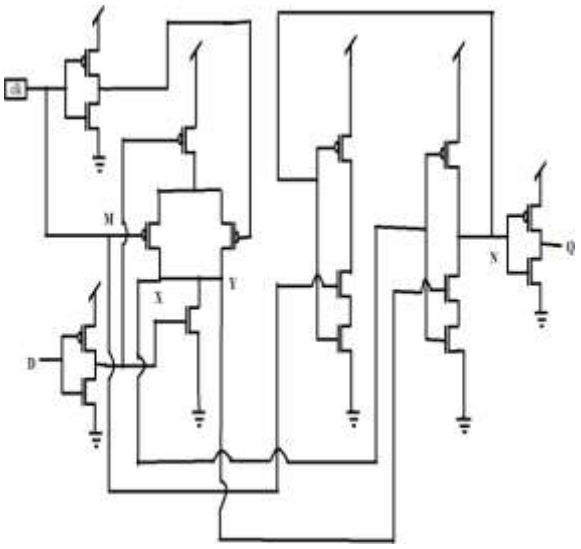

Fig -4: PROPOSED DESIGN WITH 1P-2N STRUCTURE AND C-ELEMENT CIRCUIT

Now we can assume that the initial state of nodes M and N to be M=0, N=0, X=1, Y=1, the output Q=1 and clock **clk=0**. At the node M, if any error or glitch exists from the prior combinational design, then the value of the node M will be changed from 0 to 1. For the first 1P-2N structure, the input combination becomes M=1 and clk=0. For this input combination, first 1P-2N structure's output goes to the high impedance condition, consequently, its output remains in its prior condition that is X=1. For the second 1P-2N structure, the inputs are M=1 and clk=1, so for this input combination, second 1P-2N structures output Y=0. Now for the C-element circuit, the inputs are X=1 and Y=0, therefore, its output goes to the high impedance condition meaning that its output remains in its past condition that is N=0, so the output becomes Q=1. Therefore, we can look that there is no difference in the output state.

Now considering nodes M and N to be M=1, N=1, X=0, Y=0, the output Q=0 and **clk=0**. If any fault occurs at the node M, then the node value will be altered from 1 to 0. For the first 1P-2N structure, the inputs are M=0 and clk=0, consequently, the first 1P-2N structures output is X=1. For the second 1P-2N structure, the inputs are M=0 and clk=1, therefore, second 1P- 2N structures output is Y=1. Like now for the C-element structure, the inputs are X=1 and Y=1, then the C-element structures output switch to its input values that is N=1, therefore the output becomes Q=0, repeatedly we can look that there is no difference in the output state.

Now considering nodes M and N to be M=0, N=0, X=1, Y=1, the output Q=1 and clock **clk=1**. At the node M, if any error or glitch occurs from the prior combinational circuit, then the node value will be altered from 0 to 1. For the first 1P-2N structure, the inputs are M=1 and clk=1. For this input combination, first 1P-2N structures output is X=0. For the second 1P-2N structure, the input combination becomes M=1 and clk=0, for this input combination, second 1P-2N structures output go to the high impedance condition, so, its output is in its prior state that is Y=1. Now for the C-element circuit, the inputs are X=0 and Y=1, so, its output go to the high impedance condition it means output is in its prior condition that is N=0, so the output becomes Q=1. So, we can look that there is no difference in the output condition.

Now considering nodes M and N to be M=1, N=1, X=0, Y=0, the output Q=0 and **clk=1**. If any fault occurs at the node M, then the node value will be altered from 1 to 0. For the first 1P-2N structure, the inputs are M=0 and clk=1, for this input combination, first 1P-2N structures output is X=1. For the second 1P-2N structure, the inputs are M=0 and clk=0, therefore, second 1P-2N structures output is Y=1. Like now for the C-element structure, the input combination becomes X=1 and Y=1, then the C-element structures output switch to its input values that is N=1, therefore the output becomes Q=0, again we can look that there is no difference in the output condition. Thus, the incorrect input data is left out without any changes in area, power and time. Thus, the proposed design is completely glitch-resistant and has high-speed and high-efficiency.

4. RESULT AND ANALYSIS

The proposed DET-FF design is performed through the Microwind simulator.

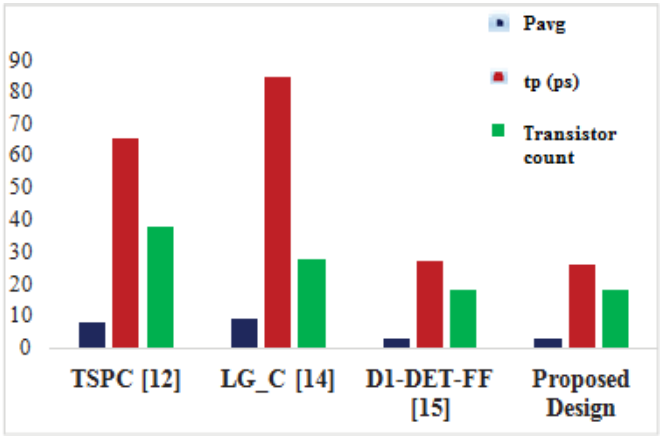

Chart -1: POWER, DELAY AND AREA COMPARISON OF DIFFERENT DET-FFs

Consequently, the proposed design has high efficiency as compared to existing dual edge triggered flip flop designs. The power delay product analysis is shown in Chart-2, which shows the channel lengths for the transistors are taken to 22 nm. In the latest technologies, the operating voltage decreases and the frequency increases. Therefore, we have taken 1V operating voltage and frequency fixed to 500 MHz's. Although the operating frequency is large enough, then the output will not reduce. Table 1 shows the performance evaluation results. The average power consumption, power delay product and propagation delay comparisons are indicated in table and calculated and verified for existing DET-FF designs. We note that the proposed DET-FF design has a small number that the resented design has the lowest power delay product to the lower delay and lower average power consumption, the proposed designs have lower PDP. The propagation delay analysis of proposed DET-FF with temperature variations at different supply voltages is presented in Table 2. The delay rises with the temperature rises but decreases with the supply voltage increment. Temperature affects the carrier mobility and the threshold voltage (V_t). When the temperature increases, both the carrier mobility and the threshold voltage decrease, consequently, the timing performance of a circuit design depends on the supply voltage. Due to the temperature increment, obviously decrement in threshold voltage results in an increment of both the propagation delay and the output transition time, although decrement in the carrier mobility produces completely different variation of the timing performance. Therefore, Increase in temperature decreases the mobility of the ions.

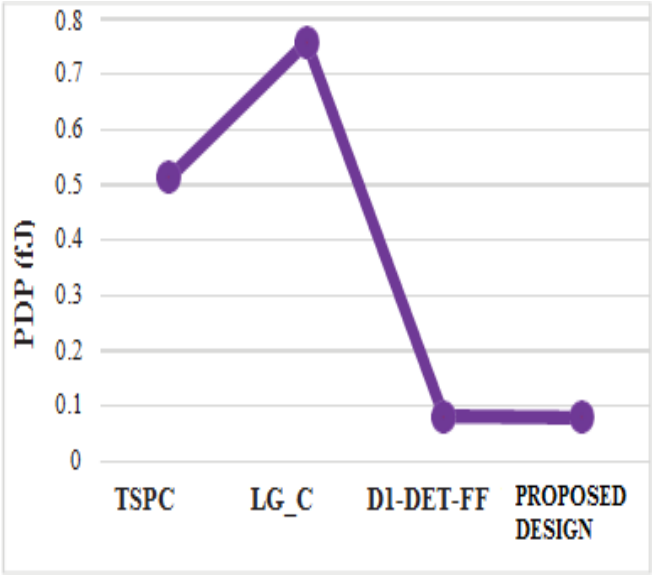

Chart -2: PDP COMPARISON OF DIFFERENT DET-FFs

Due to the technology scaling, the leakage current increases and also increase the total power consumption. To reduce the total power consumption, one possible solution is to use higher threshold voltage. Average power consumption analysis of proposed DET-FF with temperature variations at higher Vt at different supply voltages is presented in Table 4. The Average power consumption reduced by using the higher threshold voltage. Chart-3 shows the delay analysis of proposed DET-FF with frequency. The propagation delay raises with the frequency variations (from 25MHz - 1000MHz). Due to the supply voltage minimization, power consumption reduces but propagation delay rises. Due to the delay rises, the average power consumption also rises with the frequency increment, as indicated in Chart-4.

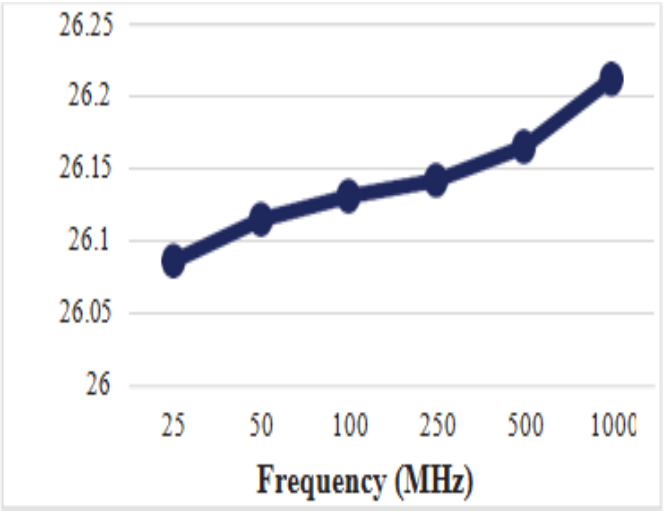

Chart -3: ANALYSIS OF PROPOGATION DELAY OF PROPOSED DESIGN WITH DIFFERENT FREQUENCIES

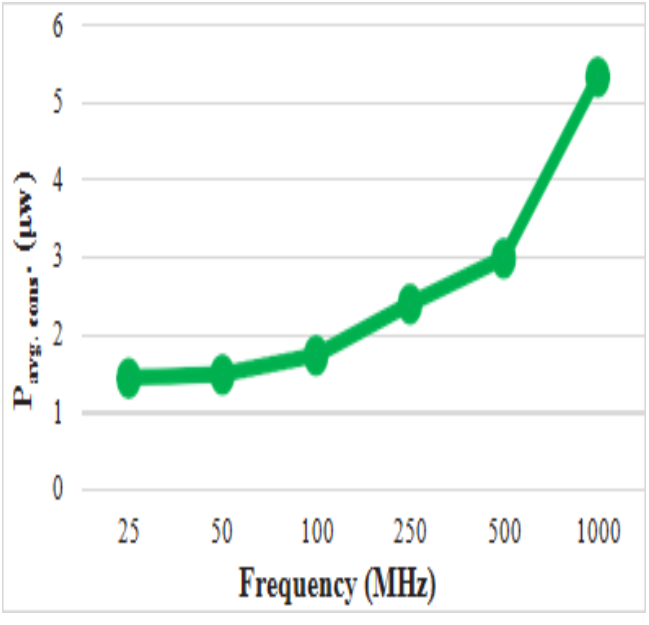

Chart -4: ANALYSIS OF POWER CONSUMPTION OF PROPOSED DESIGN WITH DIFFERENT FREQUENCIES

TABLE I. RESULT ANALYSIS OF DIFFERENT DET-FFs

DET-FFs	TSPC[12]	LG C[14]	D1-DET-FF[15]	Proposed Design
$P_{avg.\ con.}$ (µw)	7.825	8.988	3.049	3.011
$t_{p(D-Q)}$ (ps)	65.536	84.297	26.995	26.165
$t_{p(CLK-Q)}$ (ps)	43.213	63.281	25.896	25.013
PDP (fJ)	0.513	0.758	0.082	0.079
No. of transistors	38	28	18	18

TABLE II. PROPAGATION DELAY ANALYSIS OF PROPOSED DET-FF

Temperature (°C)\Power supply	0.7V	0.8V	0.9V	1V	1.1V	1.2V
-60	47.712	42.347	31.275	21.916	16.961	14.056
-40	52.458	45.389	32.984	22.181	17.489	15.922
-20	57.649	50.264	35.697	22.998	18.071	16.018
0	70.076	58.206	40.927	23.986	19.918	17.028
20	89.185	68.541	45.622	25.365	22.695	19.998
40	105.93	79.95	67.025	41.475	38.085	33.505
60	120.89	97.95	79.986	67.675	61.298	50.245
80	149.02	129.23	109.04	89.902	75.304	61.042

TABLE III. AVERAGE POWER CONSUMPTION ANALYSIS OF PROPOSED DET-FF

Temperature (°C)\Power supply	0.7V	0.8V	0.9V	1V	1.1V	1.2V
-60	1.568	2.133	2.372	2.537	2.885	3.205
-40	2.027	2.228	2.553	2.751	2.994	3.533
-20	2.203	2.456	2.876	2.998	3.316	3.912
0	2.388	2.631	2.989	3.001	3.687	4.198
20	2.422	2.795	3.001	3.003	4.003	4.538
40	3.698	3.958	5.001	5.479	6.502	7.415
60	4.695	5.546	7.011	7.524	8.855	9.705
80	6.054	7.987	9.047	9.978	11.387	12.223

TABLE IV. AVERAGE POWER CONSUMPTION ANALYSIS OF PROPOSED DET-FF AT HIGHER V_T.

Temperature (°C)\Power supply	0.7V	0.8V	0.9V	1V	1.1V	1.2V
-60	1.001	1.233	1.781	2.037	2.335	2.685
-40	1.127	1.388	2.001	2.251	2.594	3.023
-20	1.308	1.686	2.188	2.381	3.002	3.465
0	1.658	2.031	2.534	2.698	3.117	3.798
20	1.981	2.392	2.739	2.898	3.497	4.128
40	2.308	3.058	3.692	3.976	4.582	5.415
60	3.197	4.016	5.001	5.524	6.125	6.895
80	4.154	5.089	5.987	6.564	7.468	8.213

5. CONCLUSION

A glitch free DET-FF with the mixed combination of 1P- 2N structure and C-element circuit has been proposed. The proposed design is constructed by using two fault resistant structures. If any error or glitch affects one of the structures, then it is nullified by another structure. This design provides the totally glitch resistant output and can improve the system efficiency. The proposed design can decrease the half power consumption and commit to the total system power savings. Due to the implementation of this design with fault resistant structures and an internal dual-feedback structure, obtain robust and static operation. The proposed design has the lowest average power consumption and lowest PDP in comparison with the existing DET-FF designs. The proposed DET-FF has the less transistor count, consequently, occupies less area and has the small delay, therefore, provides the high speed and high efficiency. We also analyzed the temperature impact on power and delay. The power consumption and delay increase with the temperature increment. Higher threshold voltage has been used to reduce the power consumption.

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