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Design of 1 Bit ALU using Various Full Adder Circuits

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Abstract - *This paper explores design of 1-bit ALU using various full adder techniques such as Transmission Gate(TG), Complementary Metal Oxide Semiconductor(CMOS), Gate Diffusion Input(GDI), Modified GDI logic. The main design objective is to implement 1-bit ALU using different full adders providing low powered and high speed with voltage swing. GDI is one of the area effective, high speed and low power technique. It needs smallest amount of transistors compared to CMOS technology. 1-bit ALU is designed in 180nm, 130nm technologies.*

***Key Words*: Full adder, ALU, GDI, CMOS**

1. INTRODUCTION

In the current scenario of VLSI circuit design, a tremendous need for low power circuits is seen with an enormous increase in portable devices. Major research works has been focusing on power optimization and minimization in order to increase the battery life of portable devices. This enhances functionality of digital circuits and leakage power expenditure becomes an important design parameter. Adders are heart of computational circuits. It is used in many combinational and application based integrated circuits. An Arithmetic Logic Unit (ALU) is a digital circuit which performs arithmetical and logical operations. It is essential building block of the central processing unit (CPU) in a computer. Modern CPU's contain mind boggling and ground-breaking ALU's.

Full adder is a digital combinational logic circuit that performs addition operation, in which it contains three inputs and two one bit outputs which are sum and carry. A full adder can also be implemented with the help of two half adder cells. Full adders are generally connected in a cascade manner to build various logical circuits.

This paper discusses about overview on one bit ALU designed using various full adders, their power consumption and delay. Section II represents basic full adder cell. Section III represents implementation of various full adder technologies. Section IV represents design of 1bit ALU using full adder techniques. Section V represents their performance comparison.

2. FULL ADDER CELL

A full adder circuit is a combinational circuit that performs addition or subtraction. It is so called because it adds two binary digits together and generates sum and carry as outputs. It consists of three inputs and two one bit outputs as shown in the Figure 1.

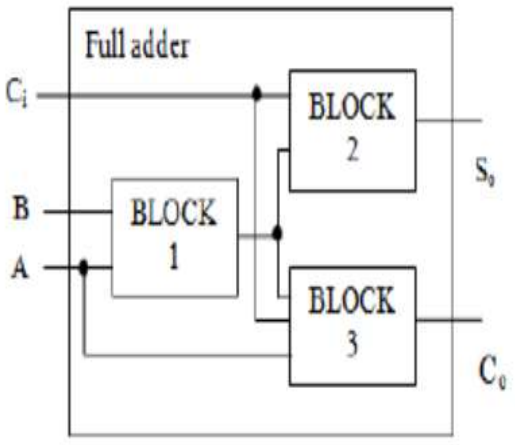

Fig -1: Full Adder cell formed by three logical blocks

3. VARIOUS FULL ADDER TECHNOLOGIES

3.1 Conventional CMOS circuit

The traditional CMOS full adder implemented with 28 transistors which comprises of 14 PMOS and 14 NMOS transistors respectively. It has the ability to produce full swing voltages. The drawback of this circuit is that it has more power dissipation and uses more transistors in count which occupies large area. The conventional design of CMOS full adder is shown in figure 2.

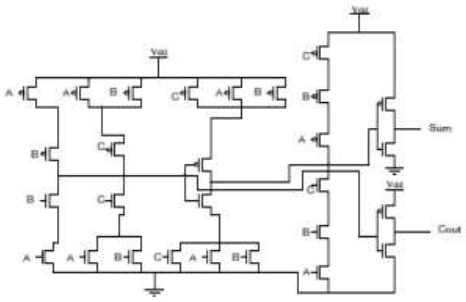

Fig -2: Conventional 28T CMOS full adder

3.2 Transmission Gate full adder

A Transmission Gate (TG) is a Switch kind of technique that can conduct in both the directions or blocked by using a control signal which applies to the gate terminal. It is a CMOS-based switch, where PMOS passes a strong logic '1' but weak logic '0', and NMOS passes strong logic '0' but poor logic '1'. It comprises of 20 transistors comprising PMOS and NMOS. The transmission gate full adder structure is shown in figure 3.

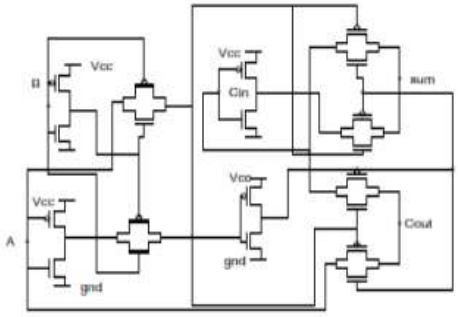

Fig -3: 20T transmission gate full adder

3.3 CPL full adder

Complimentary Pass Transistor Logic (CPL) adder contains complimentary inputs and outputs. It comprises of two stage pass transistor network. The design structure of CPL full adder is shown in the below fig.4.

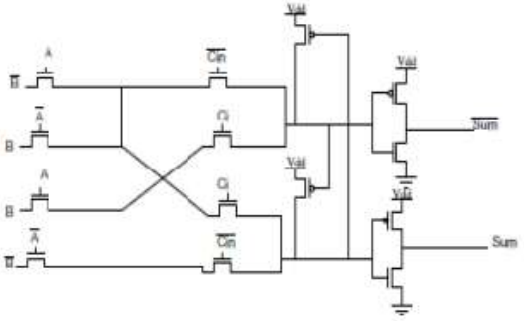

Fig -4: CPL Full adder

3.4 GDI full adder

Gate Diffusion Input (GDI) allows a low power and high speed design technique and compatible for digital combinational circuits design. The GDI technique is better in power efficient, less power consumption and delay. The numbers of transistors required are less. The GDI logic based Full adder circuit is shown below in fig.5.

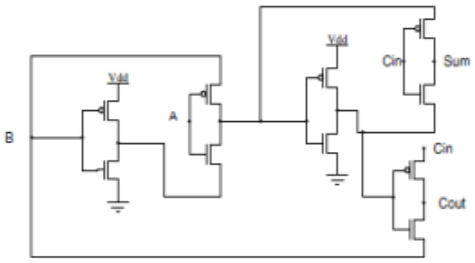

Fig -5: GDI Full Adder

3.5 8T Modified GDI based Full adder

The modified GDI technique is an updated version of GDI . It is built up using 8T where the circuit performance is increased and numbers of transistors are reduced, gives less propagation delay and low cost. It has three input terminals and both the substrates are connected to the ground and VDD.

8T Modified GDI full adder is shown in fig.6. It is constructed using XOR gate and Multiplexer. The power consumption as well as delay is less compared to other technologies.

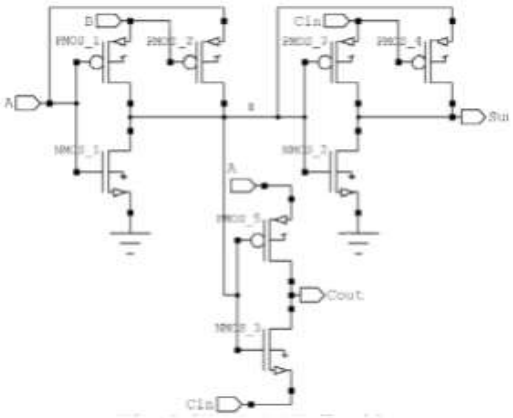

Fig -6: 8T modified GDI full adder

4. 1-BIT ALU

An ALU is a important building block of Central Processing Unit (CPU) of any computer, as every microprocessor contain one. It performs arithmetic operations like addition, subtraction, increment, decrement and also performs logical operations such as AND, OR, XOR and XNOR. The circuit comprises of two 4x1 multiplexers, 2x1 multiplexer, full adder. The fig.7 shows design circuit of 1-BIT ALU.

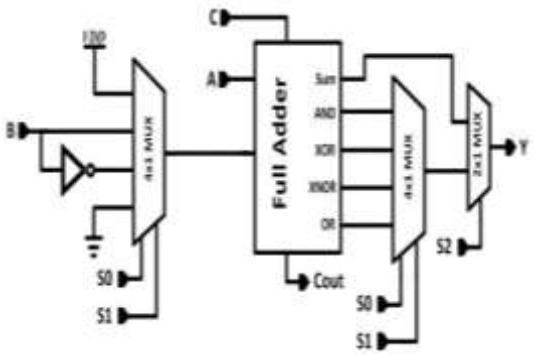

Fig -7: 1-BIT ALU

Here the one- bit ALU is designed using various full adders and their performance is compared with 180nm, 130nm technology.

5. COMPARATIVE ANALYSIS

Table -1: Comparison of various full adder techniques

Parameters	Power Dissipation	Delay
Conventional CMOS circuit	99.65uwatts	99.63nseconds
Transmission gate full adder circuit	39.94uwatts	68.14nseconds
CPL full adder	28.64uwatts	51.14nseconds
GDI based full adder	60.23nwatts	41.17nseconds
Modified GDI based full adder	20.09nwatts	68.78pseconds

Table -2: Comparison between transmission gate based ALU and modified GDI based ALU using 180nm technology.

Parameters	Power Dissipation	Delay
Transmission gate based ALU	1.9uwatts	99.99nseconds
Modified GDI basedALU	1.9uwatts	99.95nseconds

Table -3: Comparison between transmission gate based ALU and modified GDI based ALU using 130nm technology.

Parameters	Power Dissipation	Delay
Transmission gate based ALU	135.83nwatts	50.24nseconds
Modified GDI basedALU	4.4nwatts	49.80nseconds

6. CONCLUSION

Here various full adder designs are compared. 1-BIT ALU using various full adders are designed and also power consumption as well as delay are compared using 180nm, 130nm technologies. On comparing various full adder techniques, it is observed that modified GDI has a smaller number of transistors, less propagation delay, less power consumption. On implementing 1-bit ALU using modified GDI gives better performance than other full adders. This comparison shows that 8T modified GDI full adder is perfect suited for low power applications. So, as the next step to this 1-bit ALU it can be used to design and implement power efficient high speed 4-bit ALU using 90nm, 60nm,45nm technologies which can further reduce power, delay and area.

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