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# A Zero Voltage Switching Pulse Width Modulated Multilevel Buck Converter

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**Abstract -** *Multilevel dc-dc converter design is to produce a dc-dc converter that achieves soft switching for all main switches, reduces the voltage stresses across each main switch. The trend in switching power conversion is to increase the switching frequency. This provides improved transient response, smaller magnetic components and filtering capacitors and thus higher power density. To operate at higher switching frequency, a number of soft-switching technologies are present. This project proposes a new ZVS-PWM Buck converter, which is based on the multilevel technique. Five Level ZVS PWM Buck converter is proposed using the multilevel topology. This project presents ZVS for all the switches without additional voltage stress and a significant increase in the circulating reactive energy throughout the converters. The simulations were carried out to verify the performance of the proposed converter using MATLAB software package.*

***Key Words***: **Multilevel converter, Zero voltage switching (ZVS), Five level Diode clamped, Active clamping , Pulse width Modulation (PWM), Multi-carrier-PWM (MCPWM)**

## 1. INTRODUCTION

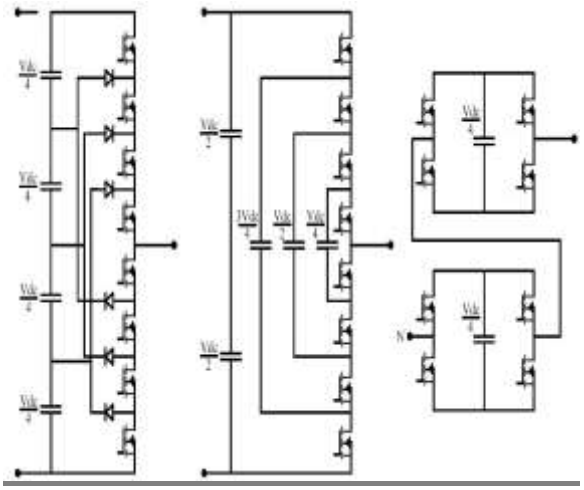
Power electronics is the technology associated with the efficient conversion, control and conditioning of electric power by static means from its available input form in to the desired electrical output form. Nowadays, the conversion is performed with semiconductor switching devices such as diodes, thyristors and transistors. In contrast to electronic systems concerned with transmission and processing of signals and data, in power electronics substantial amounts of electrical energy are processed. In electrical engineering, a DC-DC converter is a circuit which converts DC power from one voltage to another. It is a special class of power converters. DC to DC converters are important in mobile devices such as cellular phones and laptop computers, which are supplied with power from batteries. Often space limitations in a device do not allow multiple batteries to supply different parts of the device. One simple method of DC to DC conversion is a circuit known as a voltage divider, which should be familiar to electrical engineers. This technique involves inserting a resistor in series with the voltage supply to lower the voltage.

The DC-DC buck converter was chosen due to the possibility of using it in applications where the input voltage is relatively high and it is necessary to spread the voltage stresses among the active witches. When low switching losses and low emissions of electromagnetic noise are requirements, it is desirable to operate the converter with ZVS. However, resonant converters increase the voltage of the auxiliary DC bus in relation to the input voltage. Switching devices with high voltage blocking capability, such as thyristor and gate turn off thyristor (GTO's) are used since they are more compatible with voltage levels seen in utility applications. The main disadvantage of these devices is that they switch very slowly, and in the case of thyristors an external circuit is required for turn off. Faster switching devices such as a MOSFET (low voltage) and insulate gate bipolar transistors (IGBT's) bring many advantages in terms of system size and dynamic response but are unable to withstand large voltages. In order to take advantage of these smaller faster devices, several multilevel topologies have been proposed in order to reduce the voltage stress by an individual switches. The main multi level topologies- Diode clamping, flying capacitor and cascade provide for reliable division of voltage across the switching devices. Losses in switching converter are occur during the time of switching instants and the losses increase with increasing switching frequency. Many soft switching topologies have been proposed to reduce this time of switching losses. Diode clamping multi level converter are of interested since this type of multilevel topology have fewer capacitors than the flying capacitor and for the cascade topology they do not require multiple independent voltage sources.

This paper present eh simple connection with the multilevel topology, device voltage stress and achieve the soft switching for all main switches for the five level diode clamping topology with active clamping ZVS PWM technique, converter gets reduce order of circulating current and use with wide range of load application.

## 2. Converter Topology

During the last few years, there has been steady growth multilevel converter topology as they can suit for the high voltage and high power applications. Multilevel topologies are the attractive technology for the medium voltage application, which includes power quality and power conditioning applications in the distribution system. The most well-known multilevel topologies developed so far are shown in Fig. 1. These are diode clamped multilevel voltage source converter (DC-VSC), flying capacitor multilevel voltage source converter (FC-VSC) and cascaded H-bridge multilevel voltage source converter (CHVSC). These multilevel topologies can generate multilevel output voltages with low harmonics.



(a) (b) (c)

**Fig.1 Five level- Multilevel topology**

Fig.1 (a). Shows that the one leg circuit diagram of a five-level DC source converter. This topology uses clamping diodes to limit dynamic and static overvoltage for switching devices. The clamping diodes are connected to taps of dc bus capacitor. In medium voltage applications, dc bus voltage is so high therefore capacitors are connected in series. The DC-VSC generates different voltage levels for output voltage in the ranging between positive and negative of Vdc /2. The rated voltage of a clamping diode equals rate voltage of the main switching devices, a N level- level inverter leg needs the following number of clamping diodes

$$N_{D\ clamp} = (N\ l_{evel}\text{-}1)\ (N_{level}\ \text{-}2) \qquad (1)$$

In practice, more diodes are needed due to the voltage de rating of the series connection of up to (Nlevel-2) diodes.

Fig.1 (b) shows that the five level flying capacitor topology. This topology also allows multilevel output voltages. Instead of diode clamping, voltage sharing is realized by floating additional capacitors. Capacitors voltages are chosen in such a way that the difference between two capacitors corresponds to the nominal voltage of the devices. For a Nlevel-level inverter, the number of cell (Ncell) in one leg is:

$$N_{cell} = N\ l_{evel}\text{-}1 \qquad (2)$$

The size of the capacitors depends not on the number of cells, but on the power characteristics of the converter.
The flying capacitor topology is better for higher voltage and lower currents applications. In medium-voltage converters, the maximum voltage of a capacitor typically has the same voltage rating as semiconductor devices. This means that capacitors with higher voltage rating have to be unit by series connection of multiple single capacitors. The number of capacitor (NC) needed for the clamping capacitors are

$$Nc = 1+2^2+....+N^2_{cell} = N_{cell}(N_{cell}+1)(2\ N_{cell}+1) \qquad (3)$$

Fig.1 (c) shows that the cascaded H bridge Dc source topology. The circuit topology is a cascaded structure consisting of full bridge inverter units connected in series. Each unit is fed by a separate dc capacitor, loaded with the dc voltage (Vdc). No additional circuits to balance the voltage matching of the switching devices are necessary. The simplicity and modularity of this structure brings many practical effects. However, the fact that the dc link voltage must be isolated is the major drawback for the application of these structures. Several independent dc power supplies are required, which can be provided either by a transformer with multiple isolated secondary or by several transformers. For electrical vehicles, batteries or fuel cells can also be used. In order to balance the power provided by the dc voltage sources, each cell can be used in a cyclic way throughout each semi-cycle of a line period. Another benefit of this circulating method is that it achieves the same switching frequencies for all of the devices.

When the use of the multilevel voltage source converters, the first notion is that need for a large number of switches that may lead to complex pulse-width modulation (PWM) switching scheme. However, early developments in this area demonstrated the relatively straightforward nature of multilevel PWM. The most popular and simple switching scheme for multilevel voltage source converter is Multi-carrier-PWM (MCPWM). For an N-level converter, N-1 carrier signals with the same frequency *fc* and peak-to-peak amplitude *Ac* are placed in such a way, that they occupy continuous bands between the positive and negative dc rail of the inverter. The voltage reference, or modulation, waveform has a peak-to-peak amplitude *Am* and frequency *fm*, and it is centered in the middle of the carrier set. The voltage reference is continuously compared with each of the carrier signals. In the voltage source converter, the influence of frequency ratio and the number of converter level for the generated harmonics were considered.

There are several polynomial low-pass filter configurations with different shapes of amplitude-versus frequency responses. The lower order filter is desirable from the power of view of the total number of components, filter size, cost, and weight.

## 3. Five Level ZVS Buck converter

The proposal and analysis of a Five-level buck-type Converter with soft switching is presented. Where a family of distinct five-level ZVS active clamping techniques applied to the dc–dc buck converter is presented. The advantage of employing the Five-level ZVS clamping proposed in this paper is the reduction of the maximum voltage across the active switches by 25% compared to other two and three-level ZVS topologies.

Buck-type clamping features a maximum voltage across the active switches that is independent of any design parameter. The voltage across the switches is theoretically clamped to

half of the input voltage. The characteristics of this topology are very beneficial, and, consequently, the buck–buck converter will be the focus of analysis in the converter.

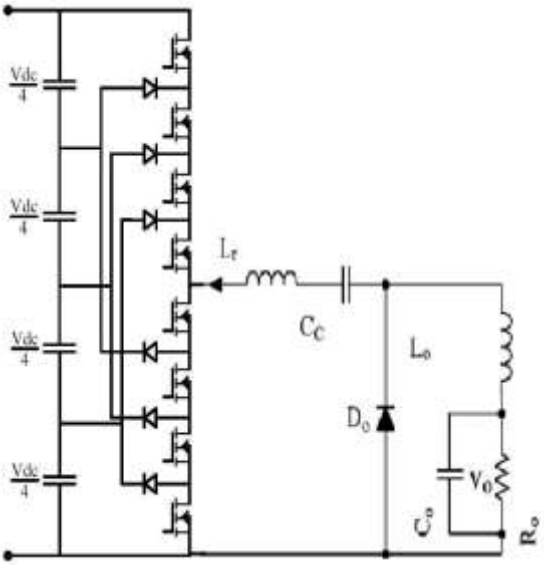


Fig.2. Five level topology for dc-dc buck converter

Fig 2. Shows the elementary topology for five level dc-dc conversions with buck operation. The circuit having the five level conversion with diode and the switches for the required level and for the buck operation diode is placed the active clamping circuit connection consist of the resonant inductance and the resonant capacitor Lr and Cr the resonant capacitor also known as a Cc. Output having the load inductance Lo and the load resistance Ro. In order to ease the understanding of the converter's operation, the following assumptions are considered.

1) Switches are ideal.
2) The converter operates in steady state.
3) The output inductance Lo is such that, in conjunction with output voltage Vo, it can be represented as an ideal current source (Io).
4) The resonant inductor Lr stores sufficient energy to complete the charging and discharging of the resonant capacitors C1 , C2 ,C3 , and C4 (cf., Fig. 5), with value Cr , during the switching transitions and to polarize the intrinsic diodes of the switches.
5) The passive components are considered free from parasitic effects.
6) The auxiliary bus capacitance CC is much larger than Cr and is capable of keeping the voltage unchanged during a switching cycle. Thus, the auxiliary bus capacitors can be represented by voltage sources.

*A. Converter Operation & Design*

Depending on the intervals between the turn-off of the switches and the value of the resonant capacitors (*C*r ), the converter can operate in nine different operation modes. However, for all cases, the converter operates under ZVS, maintaining its static-gain characteristic. The differences are noted only in a few operation stages for very short durations.

In order to simplify the stages, the voltages across capacitors are considered balanced and equal to *V*i/2. The resonant capacitor is chosen so that *C*r > *C*r limit. The necessary condition for ZVS to occur is that the switch is turned on only when its parallel capacitor is discharged. In other words, to achieve zero losses in the switching intervals, the duty cycle is defined in this manner since the drive signals of the switches are not necessarily complementary.

The average current through capacitor *C*C, *i*Cc, is computed Using

$$i_{\mathrm{Ce}}(t) = i_{\mathrm{Lr}}(t) = \int_0^{\Delta 1}\left[\frac{(V_{\mathrm{i}} - V_{\mathrm{Ce}})}{L_{\mathrm{r}}}t + I_{\mathrm{M}}\right]dt + \int_0^{DT_{\mathrm{s}}-\Delta 1}(I_{\mathrm{o}})dt + \int_0^{(1-D)T_{\mathrm{s}}}\left[\frac{-V_{\mathrm{Ce}}}{L_{\mathrm{r}}}t + I_{\mathrm{o}}\right]dt = 0$$

Where

$$I_{\mathrm{M}} = I_{\mathrm{o}} - \frac{V_{\mathrm{Ce}}}{L_{\mathrm{r}}}(1-D)T_{\mathrm{s}} \quad (4)$$

and

$$\Delta 1 = \frac{(I_{\mathrm{M}} + I_{\mathrm{o}})L_{\mathrm{r}}}{(V_{\mathrm{i}} - V_{\mathrm{Ce}})}. \quad (5)$$

The normalized load current or normalized resonant inductance "*L*n" is defined by

$$L_{\mathrm{n}} = L_{\mathrm{r}}\frac{I_{\mathrm{o}}}{V_{\mathrm{i}}T_{\mathrm{s}}}. \quad (6)$$

The average value of the average current across *C*C is zero because the system is under steady-state operation. the expression for the relationship between voltages *V*Cc and *V*i is obtained

$$V_{\mathrm{Ce}} = \frac{2L_{\mathrm{n}}V_{\mathrm{i}}}{2L_{\mathrm{n}} + (1-D)^2}. \quad (7)$$

The static gain is given by

$$V_{\mathrm{o}} = DV_{\mathrm{i}} - V_{\mathrm{Ce}}. \quad (8)$$

Defining the relationship between input and output voltage as

$$q = \frac{V_{\mathrm{o}}}{V_{\mathrm{i}}} \quad (9)$$

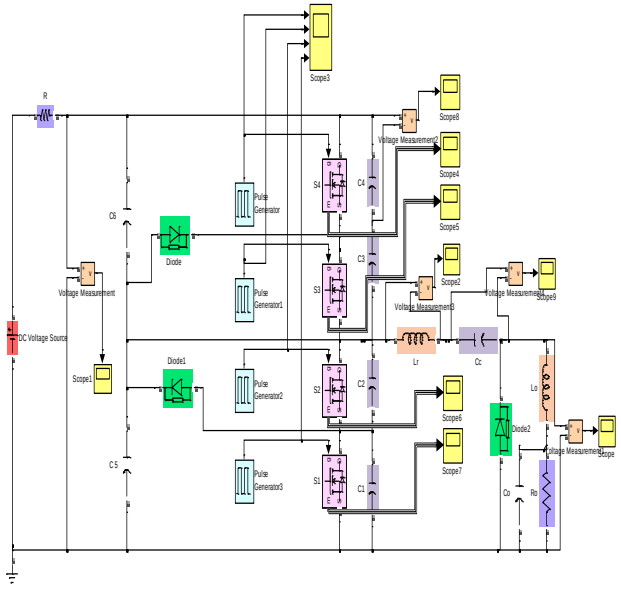
The output capacitor was sized as for a conventional buck converter

$$C_o = \frac{V_i}{f_s^2 \Delta V_o V_o \pi^3 L_o} \Rightarrow C_o : \quad (10)$$

The output inductor current ripple was

$$\Delta I_{L_o} = \frac{V_o}{L_o} \frac{(1-D)}{f_s} \Rightarrow \Delta I_{L_o} \quad (11)$$

*B Simulation Details*



3. Simulation block diagram for three level Buck converter

Using the Sine PWM to generate the gate signal for the three level buck converter. Simulation diagram is used to design the diode clamped topology with the sine and triangular reference and carrier wave from using the simulation we get the output voltage for the desired load. The simulation block having the subsystem the subsystem having the one as a pulse generation systems and other is the diode clamped topology system with the buck converter.

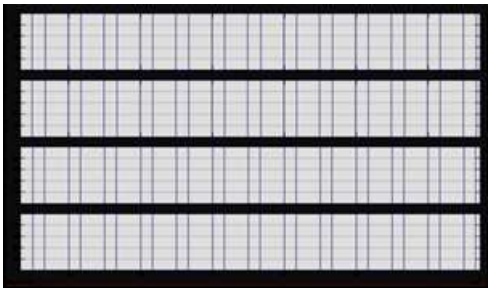


Fig. 4. PWM Signal for three level converter

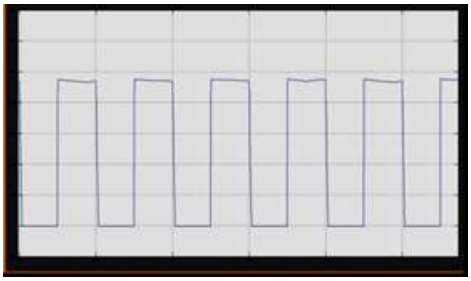


Fig.5. Output voltage for three level Buck converter

There are two type simulation block is designed for the three level converter one as a conventional PWM signal process and the other one is a multi carrier signal process.

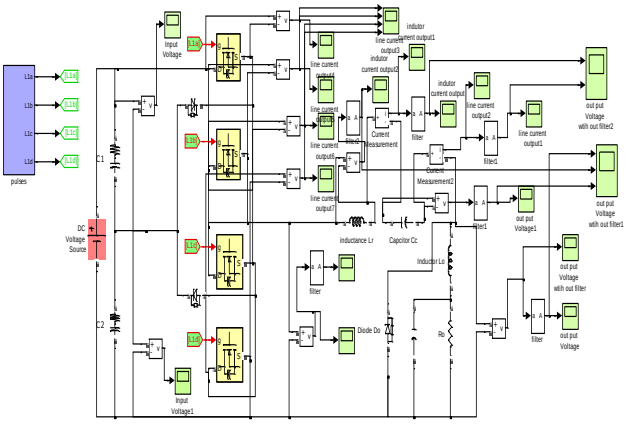


Fig.6. Simulation block for Multi carrier PWM

The both simulation block and their output are shown in the figures and the voltage stress in the three level converter is achieve in their switches only for 50 % of the voltage.

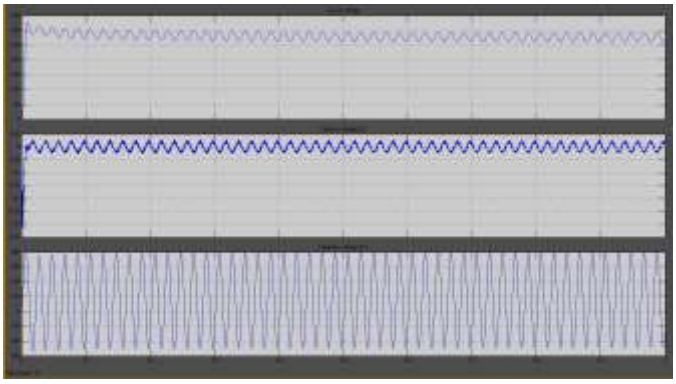


Fig.7. Output voltage for Multi carrier PWM three level Buck converter

Figure 8 shows that the voltage taking in each switch as the fifty percent of the dc voltage and each switches were achieve here as 350 voltage from the figure we get the three level converter voltage stress for each switches in the converter using the value, compare the five level converter switches voltage stresses.

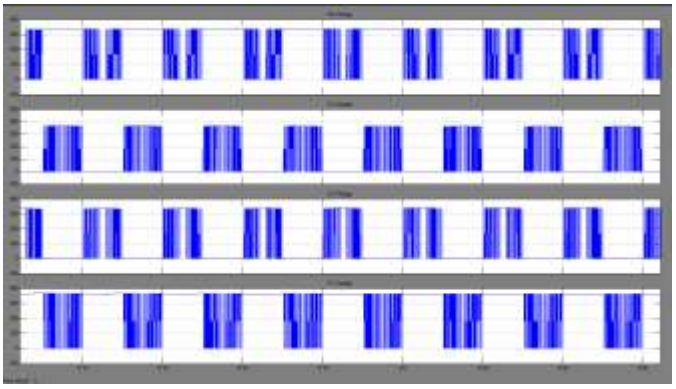


Fig.8. Voltage for each switches

Three level converter having the load as dc separately excited motor and the output wave forms are shown below figures.

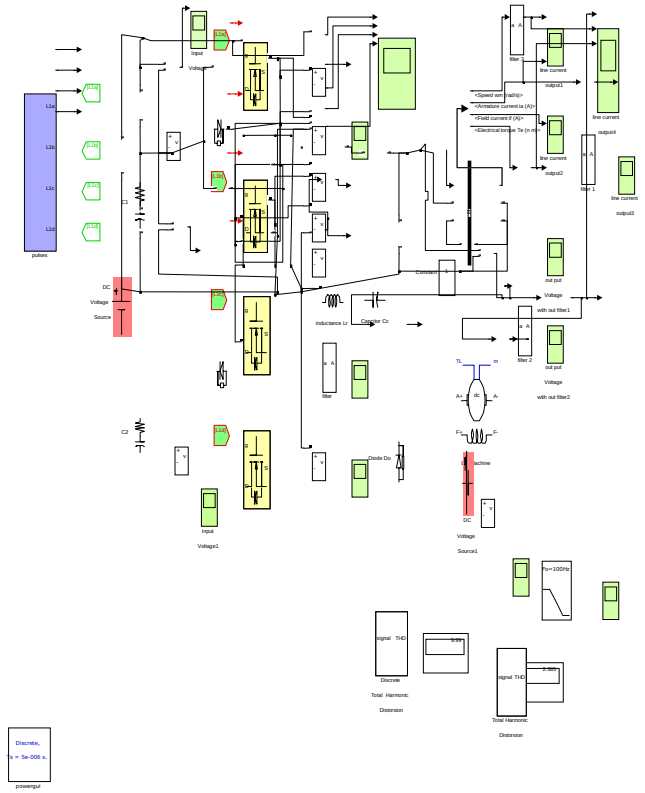


Fig.9. Simulation block with dc separately excited motor load

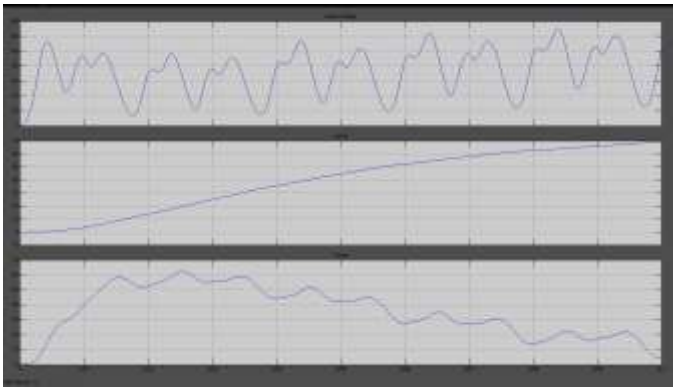


Fig.10. Output wave form for dc separately excited motor load

### *C. Five –level ZVS PWM buck converter*

Multilevel converter has become attractive in the power industries and it can be applied in many applications especially on improvement of the power quality. Using the diode clamped topology the five level converter is designed. Here the multi carrier PWM five level converter is designed which having the load as a dc separately excited motor.

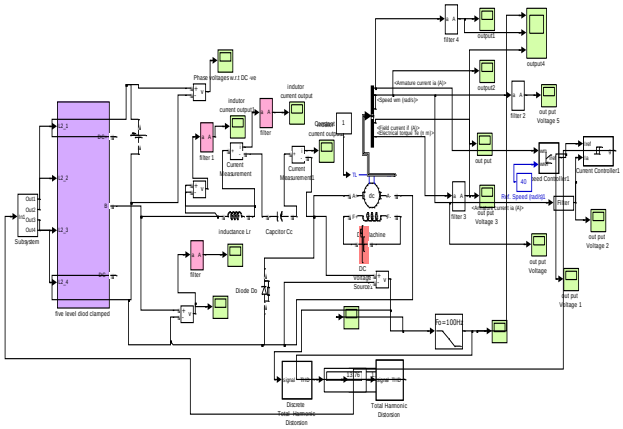


Fig.11. Sim block with dc separately excited motor load closed loop

For the multilevel, here the five level converter having the multi carrier PWM and ZVS soft switching technique and the eight switches in the five level converter are getting only the 25% of the input Dc supply the voltage stress of the switches are reduced as 75 % compare that the two and three level of converter . Depends upon the dc-dc buck voltage the connected load of dc separately excited motor is connected with closed loop control and the controller of speed control PI controller is connected and fed to the current controller then the output of the controller is connected through a switch with the both data and the reference data's the switch is compare the data's and produce the gate signals for the five level converter switches, via the closed loop control the entire system is controlled. The output and the voltage of each switch are shown in the figure.

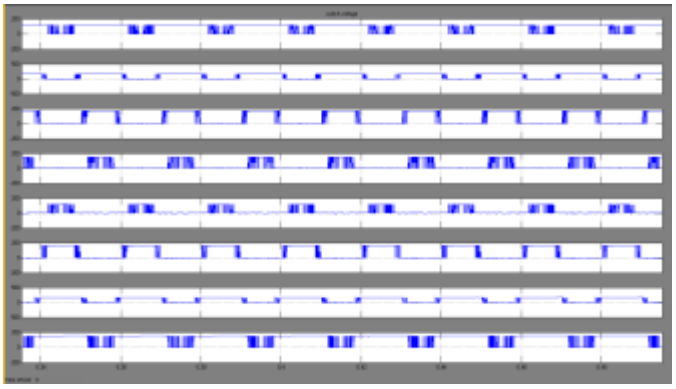


fig.12. Voltage achieve by each switch

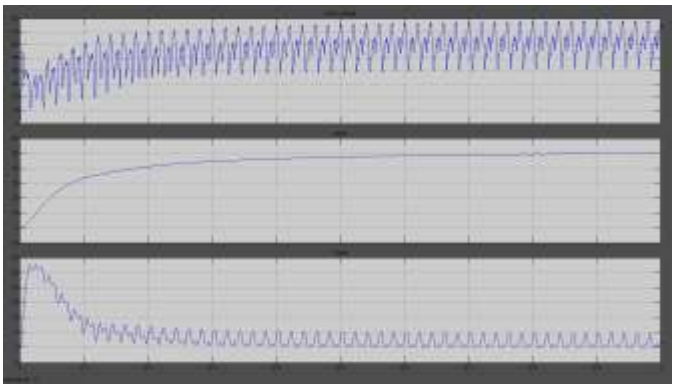


Fig.13. Output wave form for dc separately excited motor load closed loop control

## 4. Conclusions

This paper has presented a family of high-efficiency buck type dc–dc converters that are well suited for high-voltage applications. The proposed converters combine the advantages of a reduction of the voltages across the switches, which was achieved using a five level commutation cell, with decreased switching losses obtained from a ZVS technique Based on the premise that the converter should limit the voltage across the switches to half of the input voltage, a topology based on the buck converter and a buck-type three-level clamping circuit has been identified as the most suitable. This topology has been theoretically analyzed, in a closed loop application, the control of the two clamping voltages needs to be implemented, and, thus, requires more circuit complexity and extra voltage sensors. Consequently, the proposed converter is thought to be a suitable solution in applications where the switch technology poses a limitation to the available voltage ratings, no insulation is needed, and a high efficiency at high switching frequencies is required.

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