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Design of AMBA based AHB2APB protocol for efficient utilization of AHB and APB

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Abstract –*Advanced Microcontroller Bus Architecture (AMBA) is old as the on-chip bus in system-on-chip (SoC) designs. It is low performance bus. In the AMBA, Advanced High performance Bus (AHB) is a system bus which is employ to bind a analog additionally with a digital signal processor and high-execution memory controllers whereas the AMBA Advanced Peripheral Bus (APB) is employed to link up UART (Universal Asynchronous Receiver Transmitter). It too consist a bridge which links the AHB and APB buses together. The evaluation of AMBA-based embedded system is a challenging preposition. The agenda is to simulate as effectively as to combine the crossing point connection between Advanced High performance Bus and Advanced Peripheral Bus generally recognized as AHB2APB Bridge. Here to perform functional and timing simulation, we are using Verilog tool.*

Key Words: **Bus architecture, Peripheral bus, Synthesize, System on chip, Bandwidth**

1. INTRODUCTION

The Advanced Microcontroller Bus Architecture (AMBA) is a System-on-Chip means of transportation protocol. It is for high-performance buses to converse with low-power devices and within the AMBA Advanced High Performance bus (AHB) a system means of transportation is employed to attach a processor, a digital signal processor and high-performance recall controllers whereas the AMBA Advanced Peripheral Bus (APB) is employed to attach UART (Universal Asynchronous Receiver Transmitter). AMBA could be a widely used interconnection standard for System on Chip design. It too consist an association which links the AHB and APB buses together [1]. So in order to examine the bridge an AHB2APB bridge is designed and executed using verilog tool.

The AMBA identification has been acquired to satisfy the subsequent essential requirements.

1. To ease the right-first-time development of embedded microcontroller products with more than one signal processors.

2. To be not dependent on technology and make sure that system macro cells are often migrated across several range of IC processes and be preferable for gate array technologies and full-custom.

3. To relegate the silicon, infrastructure ultimatum economical on-chip and off-chip interaction for in cooperation manufacturing hardship as fighting fit as for operation [2].

The AMBA 4.0 specification clarifies five distinctive types of buses/interfaces namely:-

- Advanced extensible Interface (AXI)
- Advanced High-performance Bus (AHB)
- Advanced System Bus (ASB)
- Advanced Peripheral Bus (APB)
- Advanced Trace Bus (ATB)

2. AMBA BASED MICROCONTROLLER

AMBA is an open-standard, fixed of communication protocols for connection among countless blocks or IPs in a SoC. The AMBA description was trade by subdivisions and has crooked the de-facto prototype for interfacing mechanism in a SoC. AMBA is a suite of communication protocols for speak to all along with innumerable blocks or IPs in a SoC.

An AMBA-based microcontroller is composed of a high-performance system backbone instrument of relocate (AMBA AHB or AMBA ASB), proficient to sustain the outside memory bandwidth on which the CPU, on-chip remembrance memory and other campaign reside. This measures of move of records provides a high-bandwidth crossing point between the devices that are incorporate in the vital transfers and located on the high-performance means of transportation is a overpass to the minor bandwidth APB[3], where most of the peripheral devices in the system are positioned in the Fig.1.

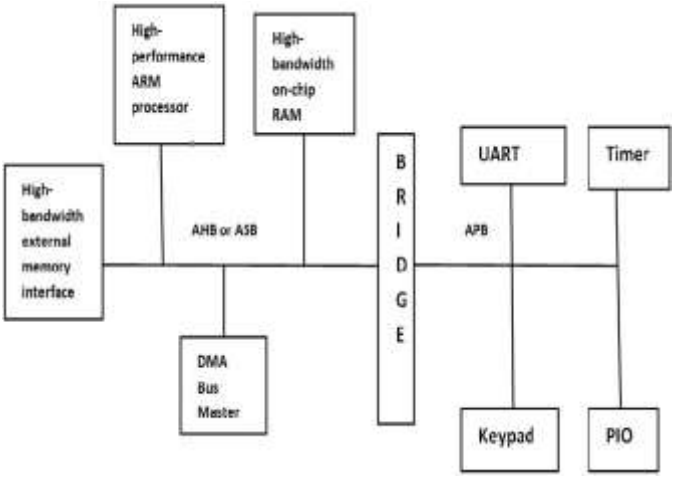

Fig.1: A typical AMBA system

The succeeding titles are used throughout this specification.

Bus cycle: A bus cycle is a data transfer series. It is the major function of AMBA AHB or APB protocol metaphors is explained from rising-edge to rising-edge transitions. An ASB bus cycle is defined as the progression of numbers from falling-edge to falling-edge transitions.

Bus transfer: An AMBA ASB or AHB bus transfer examine a line of action that is read, write of data which may handover or added than one bus cycles. The bus transfer handover is terminated by a completion rejoinder from the addressed slave.

Burst operation: A burst function is clear as one or extra registers transfer, initiated by a means of transfer bus master, which contains a drawn (fixed) width of transaction to an incremental vicinity of further size. The increment bulk for all transaction is firm by the width of handing over (byte, word).

3. AHB & APB

Advanced High performance Bus (AHB) is a new creation of AMBA bus means of transfer which is premeditated to dispatch the necessities of high-performance synthesizable designs. AMBA AHB is a new knockdown of channel of transport which sits above APB and outfits the most mandatory for high-performance, high protocol for frequency systems interfacing:

- Burst Transfers
- Split Transactions
- Single clock edge operation
- Single cycle bus master handover
- Non tri-state implementation
- Wider data bus configurations

Fig.2 illustrates the construction obligatory to put into operation an AMBA AHB pattern with decoder, master and slave.

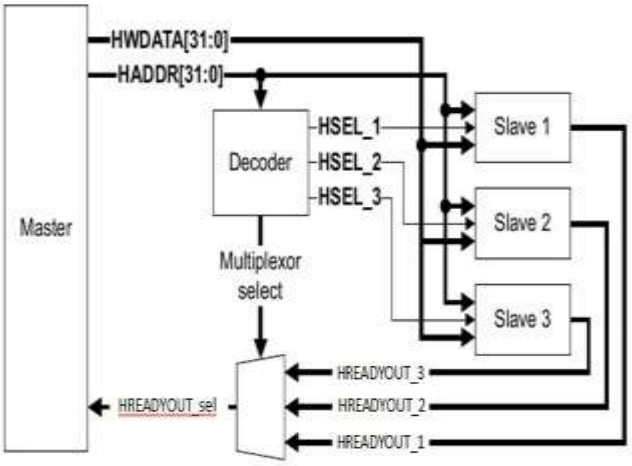

Fig.2: Structure of AMBA-AHB

The Advanced Peripheral Bus (APB) is an outcome of the Advanced Microcontroller Bus Architecture (AMBA) hierarchy of buses and is developed for nominal power expenditure for minimum weight (data) by means of up and cheap edge complexity[4]. The AMBA APB supposed to be interface to the boundary of any peripherals which are less bandwidth and act not need the tall carrying out of a pipelined means of transportation interface. The newest revision of APB ensures that everyone gesture all transactions are individual interrelated to rising edge of the clock. The perfection process of the APB peripherals protocols be integrated by a long way into any end flow, with the succeeding advantages:

- Performance is enhanced at high-frequency function.
- Performance is all-embracing of the mark-space ratio of the clock.

4. IMPLEMENTATION OF AMBA BASED AHB2APB BRIDGE

The AHB2APB interfaces AHB and APB i.e., it forms a interconnection between AHB and APB. It buffers the address, controls the data from the AHB, monitors the APB peripherals and returns the data along with the response signal to the AHB. The AHB2APB bridge is intended to drive while AHB and APB clocks give rise to any grouping of frequency and phase. The AHB2APB performs data transfer from APB to AHB for read cycle and it is explained further. Fig.3 illustrates the design and implementation of the AHB2APB interface [5].

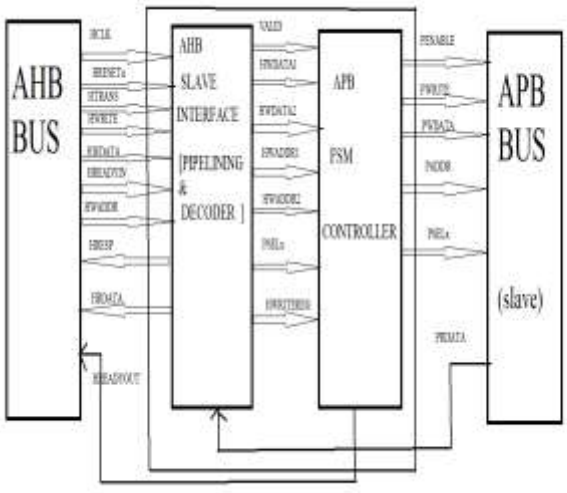

Fig.3: The AHB2APB interface

AHB2APB Bridge interfaces between the two buses i.e. AMBA high performance bus (AHB) and the other is AMBA peripheral bus (APB). It yields latching of address, controls and data signals for APB peripherals [6].

It also supports:

- APB accommodating slaves and peripherals.
- Peripherals which involve further additional wait states.

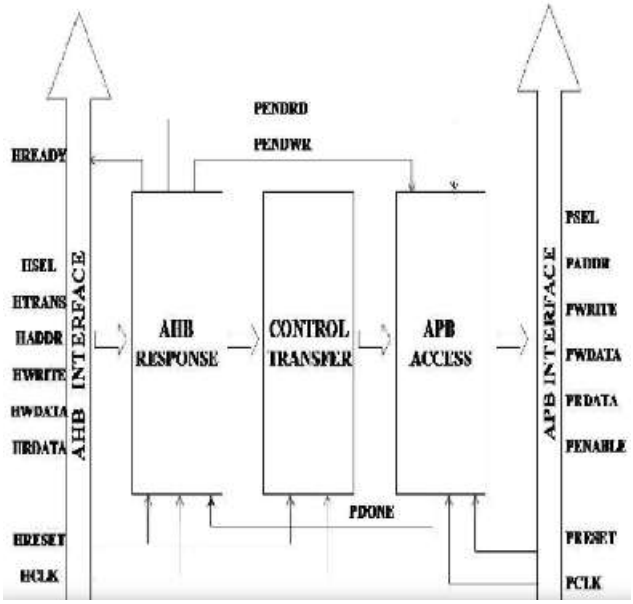

Fig.4: Internal Architecture of the Bridge

AHB2APB Bridge runs on HCLK and APB access sub module works on PCLK. AHB response and Control transfer is jointly termed as AHB interface and APB access is termed as APB interface. Fig.4 illustrates the interior architecture of the AHB2APB Bridge [7].

5. RESULTS AND DISCUSSIONS

Behavioural simulation verifies the functionality of our Verilog HDL code. The behavioural simulation result for various specifications are:

1. SINGLE WRITE

The Behavioural simulation result of single write represents inputs clk, resetn and outputs- Hwrite, Hreadyin, Hwdata [31:0], Haddr [31:0], Htrans[1:0] as illustrate in the Fig.5.

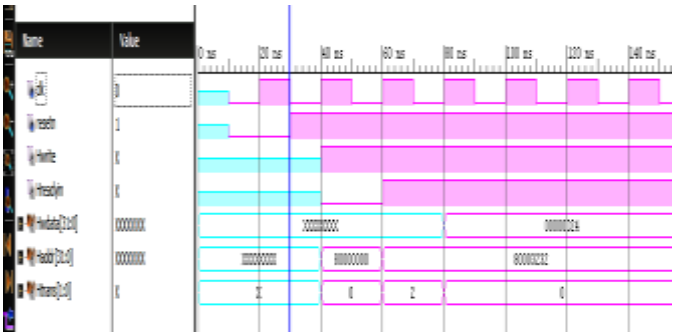

Fig.5: Single write

2. SINGLE READ

The Behavioural simulation result of single read represents inputs clk, resetn and outputs- Hsize, Hwrite, Hreadyin, Hwdata [31:0], Haddr [31:0], Htrans[1:0] as illustrate in the Fig.6.

Fig.6: Single read

3. BURST WRITE

The Behavioural simulation result of burst write represents inputs clk, resetn and outputs Hsize[2:0], Hwrite, Hreadyin, Hwdata [31:0], Haddr [31:0], Htrans[1:0] as illustrate in the Fig.7.

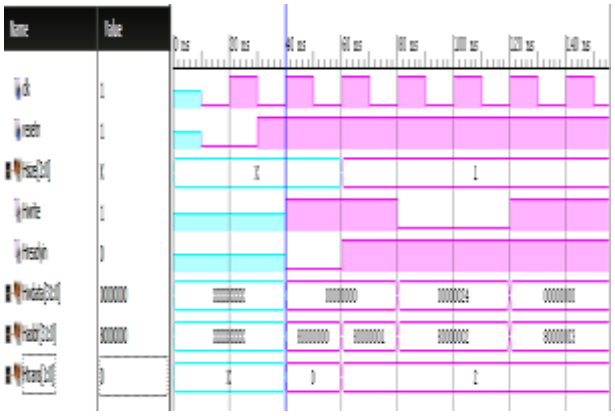

Fig.7: Burst write

4. BURST READ

The Behavioural simulation result of burst read represents inputs clk, resetn and outputs Hsize[2:0], Hwrite, Hreadyin, Hwdata [31:0], Haddr [31:0], Htrans[1:0] as illustrate in the Fig.8.

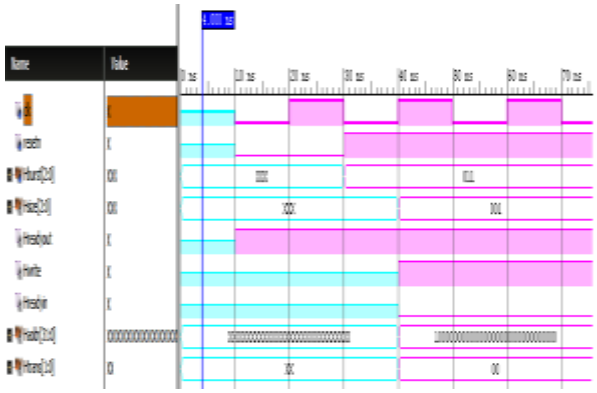

Fig.8: Burst read

5. BACK 2 BACK

The Behavioural simulation result of back 2 back represents inputs clk, resetn and outputs Hsize[2:0], Hwrite, Hreadyin, Hwdata [31:0], Haddr [31:0], Htrans[1:0] as illustrate in the Fig.9.

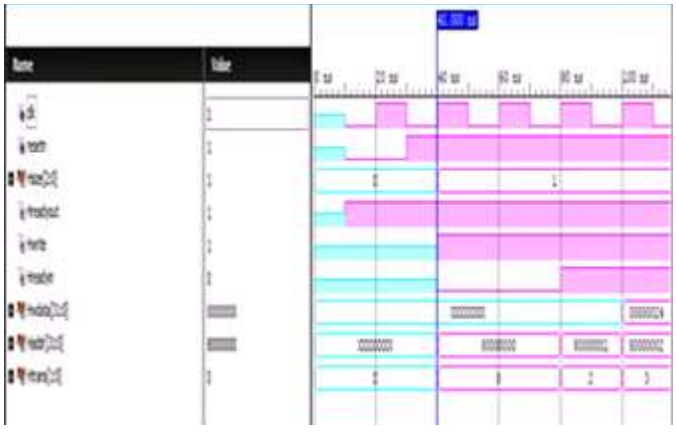

Fig.9: Back 2 Back

6. SYNTHESIS REPORT

Table.1 illustrates the ARTIX-7 BOARD Resources, Utilization, Available and Utilization percentage.

Table.1: ARTIX-7 board utilization

Resource	Utilization	Available	Utilization%
Slice LUTs	106	63400	0.17
Slice Registers	203	126800	0.16
IO	205	212	96.70
Clocking	3	32	9.38

Table.2 illustrates the VIRTEX 2 PRO BOARD Logic utilization, Used, Available and Utilization percentage.

Table.2: VIRTEX 2 PRO board utilization

Logic Utilization	Used	Available	Utilization%
Number of slices	104	13696	0%
Number of slice flip-flops	134	27392	0%
Number of 4 input LUTs	131	27392	0%
Number of bonded IOBs	205	556	36%
Number of GCLKs	2	16	12%

Table.3 illustrates the SPARTAN 3E BOARD Logic utilization, Used, Available and Utilization percentage.

Table.3: SPARTAN 3E board utilization

Logic Utilization	Used	Available	Utilization%
Number of slices	104	4656	2%
Number of slice flip-flops	134	9312	1%
Number of 4 input LUTs	131	9312	1%
Number of bonded IOBs	205	232	88%
Number of GCLKs	2	24	8%

These utilization tables of various boards explain that the protocol is easily acceptable for performing the required specifications.

6. CONCLUSION

The RTL simulation of AHB2APB bridge has been practiced by means of right analyze benches i.e. by via APB Driver and AHB Driver. The AHB2APB connection has been synthesized by performing extraction of synthesized netlist with proper delays and confirmed by correlating the gate extent simulation with the RTL simulation results. The back annotation of the bridge has been fruitfully concluded by the extraction of synthesized netlist with right delays & fixed by correlating the gate extent simulation with the RTL simulation results. Thus, AHB2APB bridge is a independent solution to extract the benefits of latterly progressed ARM based AMBA-AHB by bridging the aperture between the actual Advanced Peripheral Bus and the Advanced High Performance Bus.

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