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"Multicarrier Based SPWM Modulation for Diode Clamped MLI to reduce CMV and THD"

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Abstract *- Multilevel inverter has become most popular over the years in the area of high power medium voltage energy control. With the recent advancement in Power semiconductor switches, multilevel inverter fed induction motor drives are extensively used in industries. Common mode voltage (CMV) is the voltage measure between star point of load and system ground. CMV is produced in inverter causes current to flow through bearings which may cause premature failure of the motor bearings. This paper presents the reduction of CMV in Diode Clamped multilevel Inverter using multicarrier SPWM technique. A MATLAB Simulation of diode clamped multilevel inverter is presented by applying different multicarrier modulation techniques. CMV and THD are investigated.*

Keywords: *CMV, THD, Multicarrier Sinusoidal pulse width modulation, DCMLI*

1. INTRODUCTION

Power Electronics deals with efficient and effective use of electrical energy with the help of power semiconductor switches on-off control. The number of industry applications in which induction motors are fed by voltage source inverters is growing fast. Motor bearing life has been from six to ten years if distortion less ac power supply is given to the motor. Now a days motor bearing fails early than its life. This is because of high frequency bearing currents through motor bearing. Modern variable speed drives operates at high switching frequencies. In PWM switched 3-phase power supply to VSD, dc voltage is converted to ac voltage, but neutral point voltage is not zero. This voltage between system ground and load neutral is common mode voltage. Current flowing due to this voltage finds return path through motor bearing, shaft and inverter. Changes in inverter output voltage gives current pulses through bearings. This high frequency bearing currents may damage bearing [11].
Magnitude of this current can be reduced by reducing CMV.

Common mode voltage can be reduced in multilevel inverters by applying proper modulation technique in multilevel inverter. Multilevel inverters invented with the specific aim of overcoming the voltage limit capability of power devices. 3-level NPC has highest converter efficiency among available solutions and it is preferred choice in many industrial MV applications [5].

II. DIODE CLAMPED MULTILEVEL INVERTER

Diode Clamped Multilevel Inverter is the most widely used topology which gives the step in the output voltage with the used of clamping diode. Decrease in the power device voltage stress is the main concept of DCMLI with use of diode. An typical n-level DCMLI requires (n-1) voltage source, 2(n-1) switching device, (n-1)(n-2) diode [4],[5]. With the increase in the level of Diode Clamped Inverter the output voltage waveform improved and came closer to the sinusoidal waveform with decrease in CMV and THD [1],[3].

The Diode Clamped Multilevel Inverter structure is most suitable for high and medium voltage motor drives. The main drawback of DCMLI is that it uses an additional requirement of a clamping diode but this drawback can be overcome with the DCMLI advantages [4]. Magnitude of the harmonic is lowered and at low switching frequency THD is less, low switching losses, low dv/dt rating, reduced CMV. The fig1 (a), fig1 (b) and fig1 (c) shows structure of 3-level, 5-level, 7-level Diode clamped multilevel inverter with its step output in fig 2 (a), (b), (c) respectively.

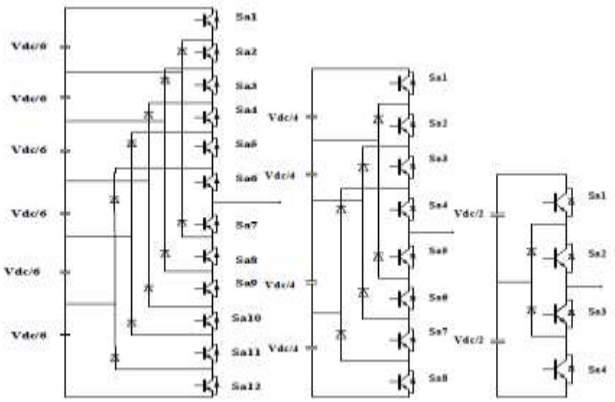

Fig.1(a)7-level DCMLI (b) 5-level DCMLI (c) 3-level DCMLI

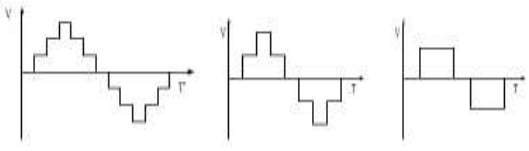

Fig2(a)7-level DCMLI (b)5-level DCMLI(c)3-level DCMLI Output voltage waveform

III. CLASSIFICATION OF MULTILEVEL INVERTERS

As shown in Figure 3.5, the classification of multilevel inverters is done on the basis of three topologies, the diode-clamped multilevel inverter (DCMLI), the flying-capacitors multilevel inverter (FCMLI) and the cascaded H-bridge multilevel inverter (CHBMLI) [2-4, 6]. These topologies can also be termed as classical topologies as a number of new configurations are derived from them.

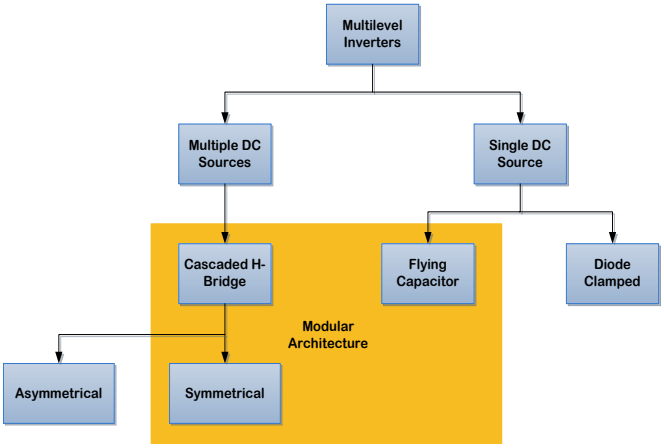

Figure 3.1 Multilevel inverter classifications

IV. DIODE CLAMPED MULTILEVEL INVERTER (DCMLI)

Values of various parameters used in this model are given in table 6.1 Fig. 6.2 show schematic diagram of basic Diode Clamped Multilevel Inverter. In 3-level DCMLI total of 8 IGBTs, 7 clamping diodes and 4 V_{cc} supply. The DC voltage source may be a battery or rectified voltage through uncontrolled/controlled bridge rectifier known as passive/active front end converter, respectively. To obtain $+V_{dc/2}$ voltage at inverter pole.

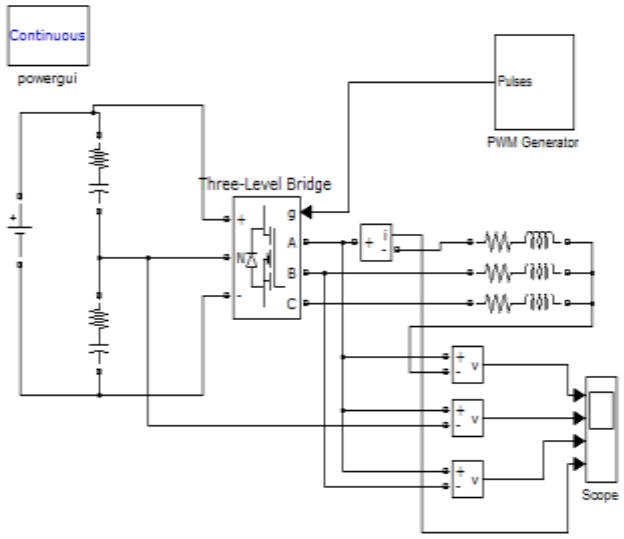

Figure 4.1 Five Level Diode Clamped Multilevel Inverter

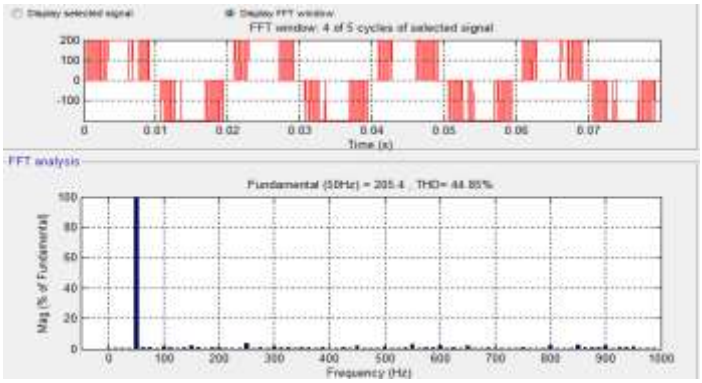

Figure 4.1 Simulation result of basic level multilevel inverters Vdc

V. FIVE LEVEL DIODE CLAMPED MULTILEVEL INVERTER SPWM

Values of various parameters used in this model are given in table 5.1 Nine different Modulation schemes is used. Figure. Shows the output line voltage whose amplitude is around 199.5 volts which is close to 200 volts. Figure 6.3 shows the harmonic profile of the output line voltage while Figure 5.4 shows the output phase voltage waveform whose amplitude is around 199.5 volts which is close to 200 volts. Figure 6.3 shows the harmonic profile of the output phase voltage. Fig. 6.3 refer to the line voltage, phase voltage and there harmonic profile respectively.

Different Modulation Schemes	*Fundamental Frequency-Line Voltage*	*(THD)-Line voltage*
PDPWM	*348.1*	*16.95*
VAPDPWM	*377.0*	*17.39*
PODPWM	*377.0*	*20.16*
VAPODPWM	*367.1*	*20.15*
APODPWM	*346.9*	*25.15*
VAAPODPWM	*376.9*	*21.23*
VFPWM	*346.8*	*18.78*
COPWM-A	*364.1*	*21.21*
COPWM-B	*364.1*	*23.87*

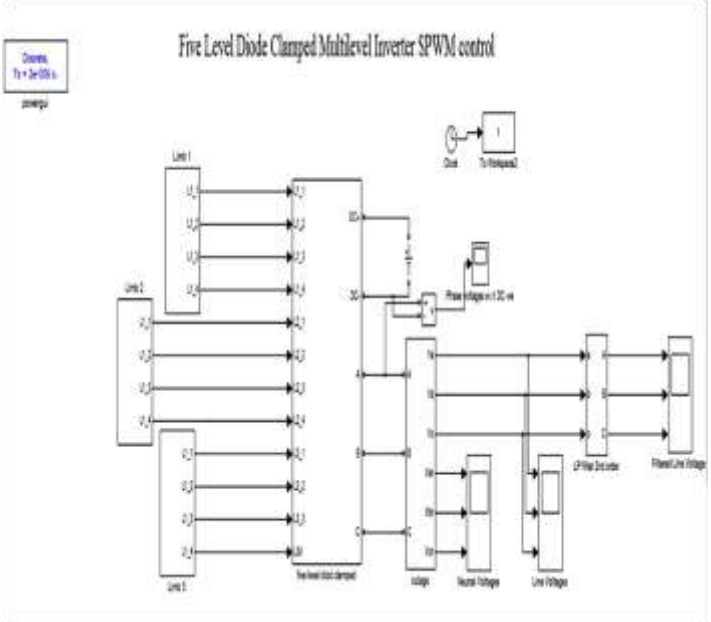

Figure 5.1 Five Level Diode Clamped Multilevel Inverter SPWM

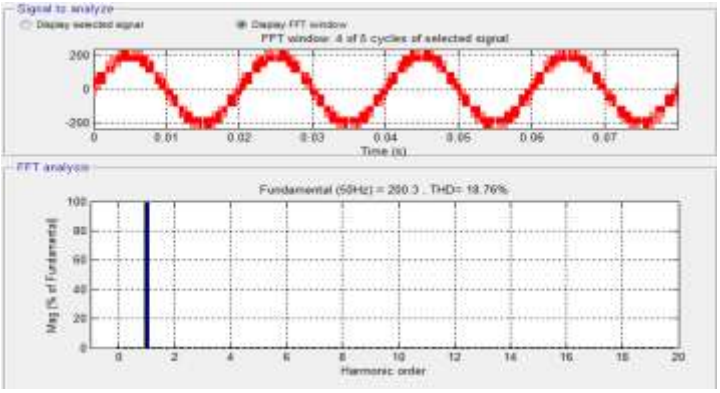

Figure 5.2 Simulation results of five level multilevel inverters Va

TABLE 5.1 FUNDAMENTAL FREQUENCY AND %THD OF LINE VOLTAGE

Table 1: CMV and THD of 3-level, 5-level

DCMLI	PD		POD		APOD	
	CMV	THD	CMV	THD	CMV	THD
3-Level	84.4	24.78%	47.49	24.78%	-	-
5-Level	39.98	13.91%	18.97	26.67%	30.56	22.44%

CONCLUSION

3-level, 5-level Diode clamped multilevel inverter is simulated in MATLAB Simulink. The simulation output gives a conclusion that by employing different multicarrier based SPWM technique we can reduce the CMV or eliminate the CMV. By applying multicarrier based POD SPWM strategy, CMV obtained is less as compared to PD and APOD strategy.

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