DESIGN AND ANALYSIS OF A COMPARATOR FOR ADC IN TANNER EDA

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ABSTRACT--- Flash ADC is the fastest ADC in the analog to digital conversion which is employed popularly in high-frequency applications. The comparator is a major block used in the flash ADC for analog to digital conversion. The use of comparators count is varied depends on the resolution of the flash ADC. Comparator count increases as 2n for an n-bit resolution flash ADC. As the resolution of the ADC increases, the use of comparator count in the ADC is also increased as large which increases the area utilization of the ADC. This paper analyzes the area and power utilization factor of the various types of comparators in order to solve the area utilization problem in the flash ADC. The comparator circuits are simulated in cadence virtuoso using CMOS 180nm technology. The power, area and delay of the different comparators are compared for best utilization in the flash ADC.

Keywords— ADC, Comparator, Resolution, CMOS, Track and Latch, TIQ

1. INTRODUCTION

Analog to digital converter (ADC) is the most frequently used analog and mixed-signal circuit for analog to digital data conversion in microprocessors and microcontrollers, DSP architectures, communication devices and consumer electronics applications. It is a strap between analog and digital processing techniques to process the real-world analog signal and to produce the equivalent digital outputs for fast and accurate processing in the high-performance digital devices. Flash types ADC is the fastest data converter which uses (2^N-1) number of comparators to simultaneously to compare the analog input voltage with the reference input voltages. In the flash ADC, the output of the comparator is obtained in the form of thermometer code and then using an encodes the thermometer code form of digital data converted into the binary outputs form. The flash ADC architecture does not require any linear amplification technique since it has the highest rate of the analog signal to digital data conversion speed at any given technology. In an ADC, many circuit techniques like folding, interpolation and sub-ranging are used in the implementation to reduce the power consumption and the area overhead of the circuit. The use of modified architecture for a flash ADC use to reduce the linearity of its transfer function due to the generation of the random offset voltage. The offset voltage is induced in the symmetric circuit configuration due to the mismatches of the transistors in the comparator circuit.

This paper provides the detailed design and analysis of the linear comparators of the ADC for area overhead, power dissipation and the conversion performance. A low noise latch track comparator has been introduced in [1] for high-speed low power flash ADC applications. A random-chopping comparator has been introduced in [2] to reduce the offset by observing the code density of the comparator. All the calibrations are performed in the digital domain through the characterized probabilistic distribution of the analog input and reference voltage. Offset fluctuation has been reduced drastically in the method introduced in [3]. A threshold inverter quantization (TIQ) based comparator has been introduced in [4-5] for high-speed low area flash ADC applications. The TIQ comparator provides the voltage swing up to the supply voltage. TIQ-comparator quantizes the analog input data to the thermometer code. The TIQ method is modelled to set the threshold voltage by varying the channel length and width of the transistor.

2. THE DESIGN STRUCTURE OF THE COMPARATORS

Latch-track comparators, Dynamic comparator, high-speed comparator, low power comparator and TIQ comparators are the popularly used comparators in the implementation of the flash ADC.

A. Dynamic Comparators

Usually, the use of a large number of comparators in the flash ADC increases the power dissipation. Dynamic comparator reduces the power dissipation of the ADC by eliminating the static power dissipation. The use of dynamic comparator in the ADC increases the value of offset voltage and reduce the gain of the circuit. In order to make a high speed and low power comparator, the preamplifier-based comparator is used in the high-speed comparator. A static mismatch developed in the comparator components due to the variations of the threshold voltage V_{Th} and $\mu_n C_{ox}$, are the critical issues in the comparators. A dynamic comparator proposed in Fig. 1 has a capacity to overcome the static mismatches present between the components. Although it has the advantage of low power dissipation but it suffers severely from the dependency of input evaluation on the common-mode input voltage (V_{cm}). In the differential amplifier of a high-speed comparator, observation of less common mode voltage is an attractive solution to increase common mode range. The double tail dynamic comparator is a popular circuit used with a different tail transistor for both pre-amplifier and latch stage to avoid the drawbacks like static mismatches and noise. A noise in the comparator

can be reduced using a cross-coupled inverter. From the power calculation, it can be easily seen that trans-conductance (gm) of the transistor in preamplifier plays an important role in power consumption. A small modification implemented in the pre-amplifier stage of dynamic comparator reduces power up to a great extent.

B. Latch Track Comparator

The schematic diagram of the latch-track comparator is shown in Fig.2. The first stage of the circuit is functioning as a preamplifier which amplifies the input signal to improve the sensitivity of the comparator. The second stage of the circuit compares the reference voltage with the input voltage for analog to digital data conversion. The circuit has two inputs. One input is an analog input and the second one is the reference input from the resistive ladder of the flash ADC. The first stage of the circuit amplifies the difference voltage of V_{in+}, V_{ref+} and V_{ref-}, V_{in-}. A clock signal to the NMOS transistor of the preamplifier erases the residual voltage stored in the previous sample. In the direct result of the preamplifier i.e., the first stage of the latch track comparator, the output may be affected with the noise of the clocked comparator due to large amounts of charge transfer from track to hold mode. The second stage of the comparator track the input sample and hold the output with respect to the changes of the clock signal. When clock (Clk) is high, the NMOS erases the previous sample and stores the new sample under track mode. When the clock is low, the circuit functions under hold mode and retains the voltage stored in the latest track mode. Usually, in the track and hold comparator, the gain of the first stage amplifier is not enough to drive the digital circuits. In order to improve the gain of the comparator output, the second stage of the comparator designed to provide large gain to the output. The input differential NMOS pair and the latch NMOS pairs form the cross-coupled inverter in the second stage to improve the gain. Here, latch-track technique increases the gain instead of increasing number of transistors.

C. Low Voltage Comparator

The importance and wide applications of an ADC push the researchers to design a comparator with low voltage, low power, low area overhead with the conversion improved speed. Fig. 3 shows the schematic circuit of the low voltage comparator [6-7]. The positive feedback configuration in the differential amplifier by adding a few transistors to form the feedback circuit without increasing large propagation delay. In the differential configuration of the comparator, A reference voltage is applied as one input and the analog input signal is applied as another input. When an analog input voltage is greater than the reference voltage the differential amplifier amplifies the difference as positive. When an analog input voltage is less than the reference voltage the differential amplifier amplifies the difference as negative or zero [8-9]. The point which differentiates the input voltages develop the difference voltage to amplify in the differential amplifier. The capacitor couples output transistors improve the gain of the difference output voltage with low power utilization.

D. High-Speed Comparator

Fig.4 shows the schematic circuit of the high-speed comparator which can be used to implement the linear comparison circuit functions. The circuit is constructed using a differential amplifier based op-amp circuit. The circuit of a high-speed comparator is formed with the combination of a high-speed comparator and the differential op-amp circuit. This circuit combination is a key point in the design of high-performance comparison sequences. Op-amp based circuit has the ability to provide high precision results with the feedback configuration [10-11]. The feedback loop has to be maintained for a long time in an op-amp for high precision results but in the comparator, the speed of the circuit is limited by the feedback loop of a large circuit and the yield of the comparator will be increased as high with the feedback approach.

Low-frequency operation in the comparator uses to provide high accuracy in the comparison. But in high-frequency comparison, the parasitic components and the component mismatches have to be eliminated in the circuit. The high-speed comparator shown in the figure provides the high-speed comparison by the use of a differential amplifier with an active load, a latch circuit for a gain improvement. A cross-coupled inverter in the circuit provides a low resistive regeneration process for rail to rail comparison. The proposed comparator architecture advances the logic comparison with typically problematic charge injection phenomenon for high-speed operation. The output inverter stage improves the gain of the comparator for the high voltage swing in the output voltage.

E. TIQ Comparator

Threshold Inversion Quantization (TIQ) comparator is a form of cascaded CMOS inverter which considers the threshold voltage (V_{th}) of an inverter as a reference voltage in the ADC [12]. Fig.5 shows the schematic circuit of the TIQ comparator as a form of cascaded CMOS inverters. In the cascade form of CMOS inverter, the combination of the PMOS and NMOS forms the first stage of an inverter functions as the comparator through the comparison of an analogue input voltage with the threshold voltage. And the combination of the PMOS and NMOS forms the second stage of the inverter functions as the gain comparator to provide the voltage swing in the output voltage equal to the supply voltage. In a TIQ comparator, the threshold voltage of an inverter is calculated as

$$V_{th} = \frac{V_{dd} - |V_{tp}| + V_{tn}\sqrt{\frac{K_n}{K_p}}}{1 + \sqrt{\frac{K_n}{K_p}}} \quad (1)$$

where V_{dd} is the supply voltage, V_{tp} is the threshold voltage of the PMOS transistor and V_{tn} is the threshold voltages of the NMOS transistor, $K_n=\mu_n C_{ox}(W/L)_n$, $K_p=\mu_p C_{ox}(W/L)_p$, μ_n is the mobility of the electronics, μ_p is the mobility of the holes, C_{ox} is the gate oxide capacitance of the MOS transistor, $(W/L)_p$ is the width and length ration of the PMOS transistor and $(W/L)_n$ is the width and length ratio of the NMOS transistor. The threshold voltage of the

inverter is varied by changing the width and length of the MOS transistor.

3. RESULT ANALYSIS

The schematic circuits of the comparators discussed above are simulated in cadence virtuoso using CMOS 180nm technology. The comparators are simulated with the supply voltage of 1V and the input frequency of 100kHz. The power, area and delay of the different comparators are compared for best utilization in the flash ADC. In an ADC, dynamic comparator, latch-track comparators, high-speed comparator, low power comparator and TIQ comparators are popularly used in the circuit the implementation. The comparators discussed above are simulated using the same setup mentioned above.

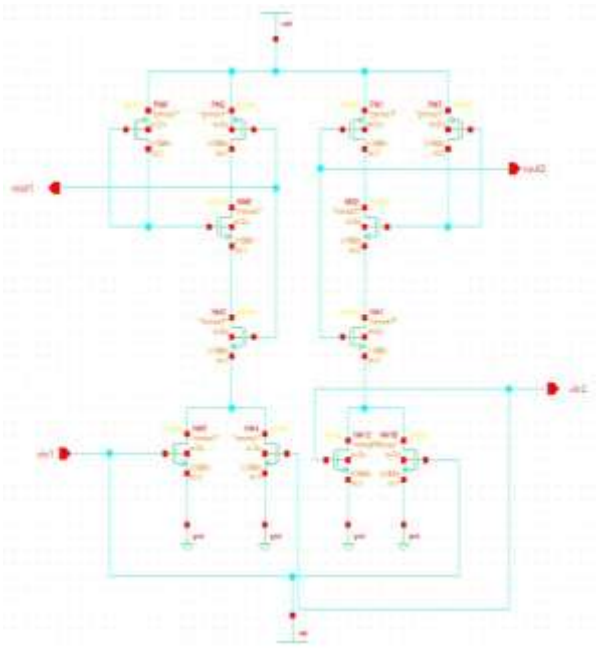


Fig. 1. Dynamic Comparator

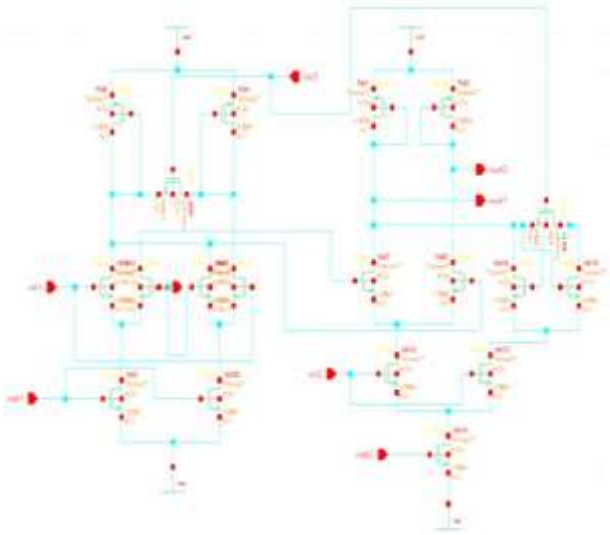


Fig. 2. Latch and Track Comparator

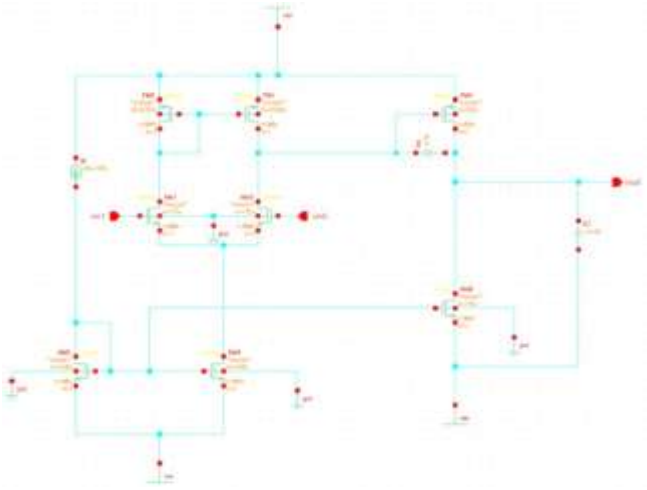


Fig. 3. Schematic Circuit of a Low Voltage Comparator

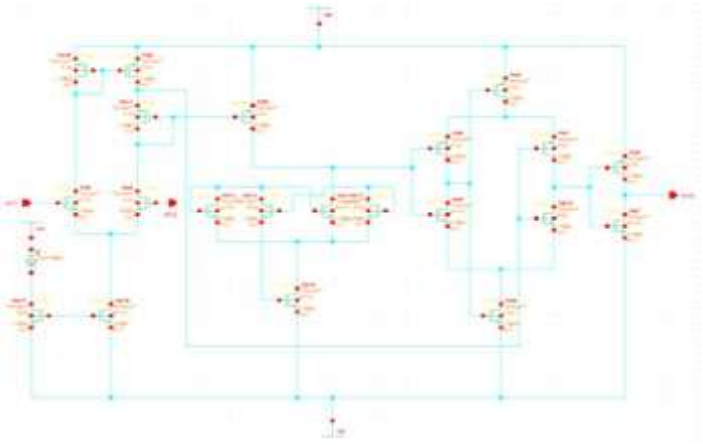


Fig. 4.Schematiccircuit of a High-Speed Comparator

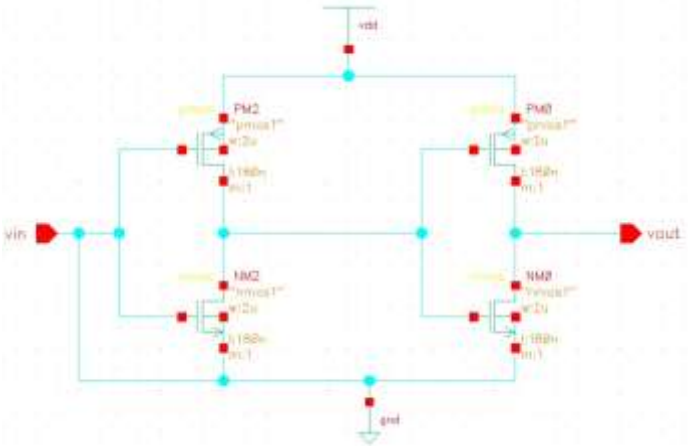


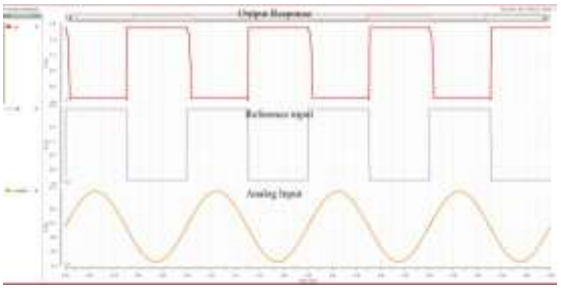
Fig. 5.Schematic of a TIQ Comparator

Table.1 Performance comparison of Comparators

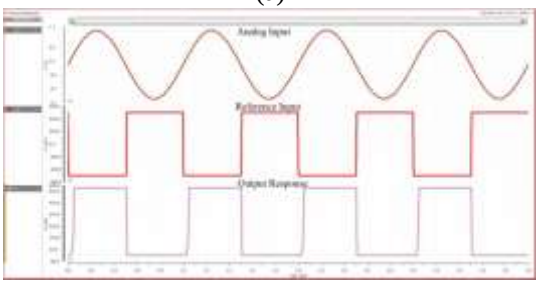
Parameters	Latch-track Comparator	Dynamic Comparator	Low Voltage Comparator	High Speed Comparator	TIQ Comparator
Technology	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS
Supply Voltage	1.8V	1.8V	1.8V	1.8V	1.8V
Input Signal range	1V	1V	1V	1V	1V
Input Frequency	100kHz	100kHz	100kHz	100kHz	100kHz
Power consumption	648.43µW	309.9nW	812.5 µW	1.084µW	5.098 fW
Delay	47.53 µsec	33.9 µsec	22.47 µsec	172.19 µsec	3.06 µsec
Number of Transistors	19	12	21	8	4
Speed/Power	32.447*10^6	95.187*10^9	18.256*10^9	5.357*10^9	64.1*10^18

The simulation results are recorded in Table.1 for performance comparison. In the Simulation, the latch track comparator results the average power consumption of 648.43µW and the delay of 47.53 µsec with the use of 19 transistors. The dynamic comparator has been constructed using 12 transistors and, in the simulation, the circuit consumed the average power of 309.9nW and 33.9 µsec of propagation delay. A high-speed comparator is constructed using 21 transistors and in the simulation, the circuit has been verified with the average power dissipation of 812.5 µW and the delay of 22.47 µsec. A low voltage comparator is implemented with 8 transistors. In the simulation, the low voltage comparator is verified with the average power consumption of 1.084µW and the propagation delay of 172.19 µsec. A TIQ comparator uses only 4 transistors in the circuit implementation. It has been simulated and verified with the average power consumption of 5.098fW and the propagation delay of 3.06µsec.

The simulation waveforms of the comparators are shown in Fig.6. Fig.6(a) shows the output waveform of the dynamic comparator in response to the comparison of the reference and analog input voltages. Fig.6(b) shows the output waveform of the latch track comparator in response to the comparison of the reference and analog input voltages. Fig.6(c) shows the output waveform of the high-speed comparator in response to the comparison of the reference and analog input voltages. Fig.6(d) shows the output waveform of the low power comparator in response to the comparison of the reference and analog input voltages. Fig.6(e) shows the output waveform of the TIQ mparator in response to the comparison of the threshold voltage of the invertor and analog input voltages.



(a)



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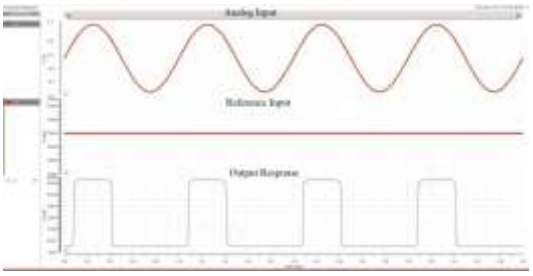
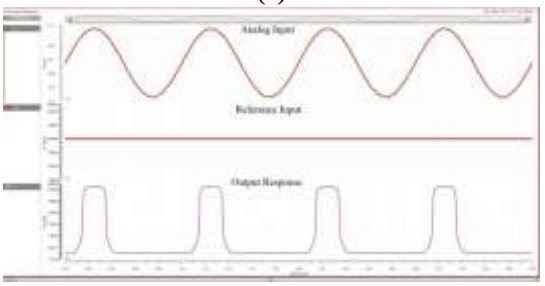
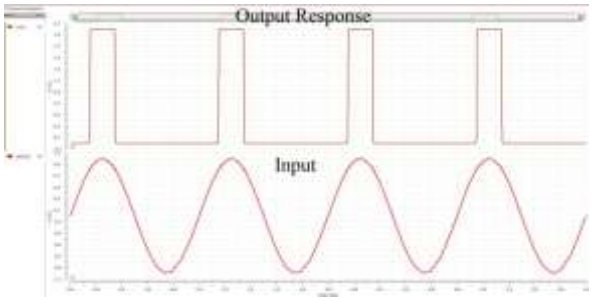


(c)



(d)



(e)

Fig. 6. The output response of the Comparators

4. CONCLUSION

In this paper, the design and analysis results of the comparators have been presented for CMOS flash ADC applications. The simulation results of the various CMOS comparators are obtained in cadence virtuoso using 180nm technology and compared with each other for performance evaluation. In comparison, a TIQ comparator has low power dissipation and the propagation delay. And the use of transistors is also less compared to all other comparators. Low voltage comparator used less transistor count next to TIQ comparator but it takes large power compared to TIQ comparators. Other types of comparators are using a relatively large number of a large number of transistors count in the comparison.

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