HIGH SPEED INEXACT SPECULATIVE ADDER USING CARRY LOOK AHEAD ADDER AND BRENT KUNG ADDER

K.Swetha Bai[1], S.Vijay Murugan[2]

[1]P.G Student, Department of Electronics and Communication Engineering, Adhiyamaan college of Engineering, Tamilnadu, India
[2]Professor, Department of Electronics and Communication Engineering, Adhiyamaan college of   Engineering, Tamilnadu, India

---***---

Abstract - *This paper presents the design of a novel architecture of a contemporary Inexact speculative adder with optimized hardware efficiency and advanced compensation technique with either error correction or error reduction which is fine grain pipelined to include few logic gates along its carry propagation chain which is considered as the critical path of the adder and thereby, enhancing the frequency of operation using carry look ahead adder and Brent Kung adder. The ISA enhances the performance of the adder by splitting the critical path into two or more shorter paths, reducing spurious glitching power and error management through an optimized speculative path and with a versatile dual direction error compensation technique. Pipelining is the process of shortening the critical path at the cost of area. The general topology of speculative adders improves performance and enables precise accuracy control.*

Key Words: **Carry Look Ahead Adder, ISA, Speculation.**

1. INTRODUCTION

High-speed adders are highly desirable in the present day scenario, though power (or energy) and silicon area are equally vital. Spectrum sensors used in intelligent cognitive-radio environment as well as internet of everything (IoE) devices focused on physical interfaces are largely-explored research areas in the recent time. Hardware for the algorithms of such applications is basically focused on sensing and actuating where the response time is key component to be optimized for real-time interfaces. Thereby, the design of highly optimized adders in terms of speed play significant role in the present era and hence this paper focuses in the design of same. With tolerable degradation in accuracy and performance, it is feasible to conceive high-speed, low power and area efficient design using inexact and approximate circuit technique. Accuracy of such circuits can be traded off to improve the power and speed by speculation.

1.1 BRENT KUNG ADDER

The type of structure of any adder greatly affects the speed of the circuit. The logarithmic structure is considered to be one of the fastest structures. The logarithmic concept is used to combine its operands in a tree- like fashion. The logarithmic delay is obtained by restructuring the look-ahead adder. The restructuring is dependent on the associative property, and the delay is obtained to be equal to (log2N) t, where N is the number of input bits to the adder and t is the propagation delay time.
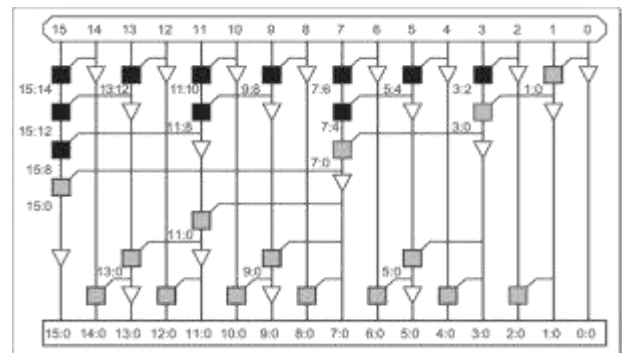

Fig -1: Block diagram of Brent Kung Adder

The above figure 1 shows all the carry signals generated at different stages in the structure. In the structure, two binary tree structure are represented -- the forward and the reverse trees. The forward binary tree alone is not sufficient for the generation of all the carry signals. It can only generate the signals shown as Co,0,Co,1, Co,3 and Co,7. The remaining carry signals are generated by the reverse binary tree.

1.2 BRENT KUNG IMPLEMENTATION

The Brent-Kung tree computes prefixes for 2-bit groups. These are used to find prefixes for 4-bit groups, which in turn are used to find prefixes for 8-bit groups, and so forth. The prefixes then fan back down to compute the carries-in to each bit. The tree requires 2 log2

N-1stages. The fan-out is limited to 2 at each stage. The diagram shows buffers used to minimize the fan-out and loading on the gates, but, in practice, the buffers are generally omitted. The basic blocks used in this case are
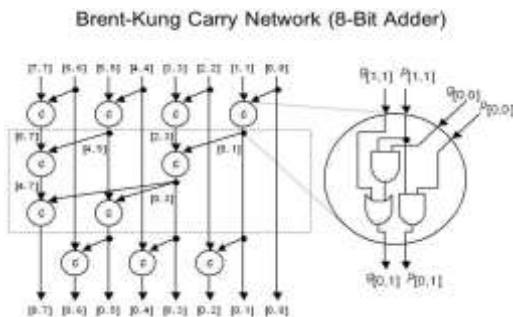
gray and black cells which are explained. This adder is implemented for 8 bit using CMOS logic and transmission gate logic.

Fig -2:8-Bit Brent Kung Network

2. PROPOSED SYSTEM

In the proposed architecture, we have segregated the *n*-bit input into 4-bit blocks (i.e., the value of *x* = 4 in Figure and each of these blocks is fed as operands to the *x*-bit adder. Unlike the conventional ISA architecture, the adder unit has been replaced with 4-bit CLA to further enhance the speed of operation. Comprehensive explanation with circuit details of various sub blocks of this adder are presented as follows:
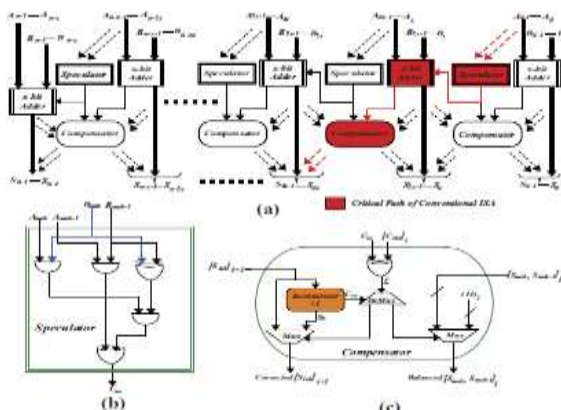

Fig- 3: (a) Basic block diagram of *n*-bit conventional In-exact speculation adder (ISA). (b) Gate-level circuit representation of speculator block. (c) Digital architecture of compensator block

2.1 SPECULATOR AND ADDER BLOCKS:

Prior delving into the circuit details, it is necessary to understand the notations used in this paper. Two *n*-bit operands for addition are represent $A = \{A_0, A_1, \ldots A_{n-1}\}$ and $B = \{B_0, B_1, \ldots B_{n-1}\}$; whereas, the sum, carry input and carry output are expressed as $S = \{S_0, S_1, \ldots S_{n-1}\}$, C_{in} and C_{out} respectively. Gate-level circuit diagram of the

speculator used in our adder design is presented. This block is based on CLA logic to speculate the output carry for each 4-bit adder block

2.2 COMPENSATOR BLOCK:

The digital architecture for compensator block used in the proposed ISA adder. This block compares the output carry from each 4-bit adder block with the corresponding speculated carry using a XOR gate. Thereafter, the output from XOR gate generates an error flag (f_e) that triggers the activation of one of the two compensation techniques error correction and reduction. The components of compensation block which are involved in the overall critical path of ISA are the XOR gate, de-multiplexer and multiplexer.

3. FINE-GRAIN PIPELINED ARCHITECTURE:

In the conventional ISA architecture, let us assume that the combinational delay of 4-bit adder, speculator and compensator blocks to be $\partial 4b\text{-}adder$, $\partial spec$ and $\partial comp$ respectively. In this architecture, carry in is speculated for each 4-bit adder block and based on this; adder block calculates the local sum. Thereafter, the faulty speculation is detected by comparing speculated carry-in and prior carry-out from 4-bit adder. Subsequently, compensator block performs the correction and balancing operation. Thus, the critical path of the conventional ISA architecture includes delays of speculator of the ith instant and the 4-bit adder plus compensator delays of $(i+1)th$ instant, as shown, (with coloured lines and blocks) For the ease of understanding, pipelining process of this work has been explained using *n* = 16 bit ISA architecture. Even though the value of *n* increases, critical path delay is unaffected because the value of *x* is always 4 bit (as discussed earlier) and the adder, speculator as well as compensator architectures remain unchanged.
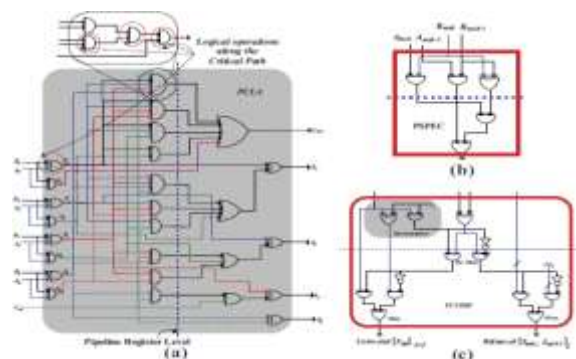

Fig- 4: Gate-level circuit of (a) Four-bit pipelined-carry look-ahead adder (PCLA) (b) Pipelined speculator (PSPEC) (c) Pipelined

compensator(PCOMP) used in the proposed ISA VLSI architecture

Sub blocks PSPEC, PCLA and PCOMP contain two pipelined stages. Overall architecture of the suggested ISA adder has been designed with five pipelined stages and there are six levels of registers included in this design. It shows the gate-level designs of PSPEC, PCOMP, PCLA and their respective pipelined stages. On observing the proposed VLSI architectures, it can been seen that the critical path of suggested architecture lies in PCLA and it includes only four two- input gate delays (one XOR and three AND gate delays).

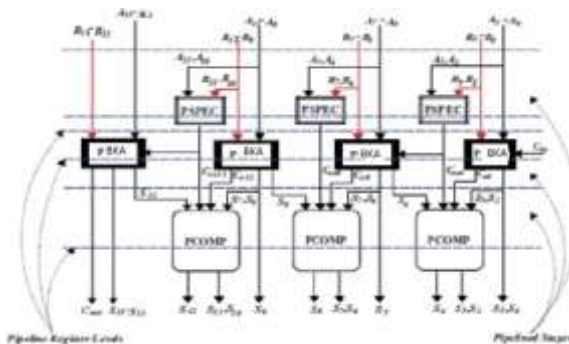## 4. PROPOSED PIPELINED ARCHITECTURE FOR IN-EXACT SPECULATIVE ADDER USING BRENT KUNG ADDER

Fig -5: Deep-pipelined VLSI architecture of the proposed ISA for n = 16 bits and x = 4 bits, with five pipeline stages, for high speed applications

In the proposed architecture the adder unit has been replaced with 4-bit Brent Kung adder to further enhance the speed of operation. The Brent-Kung adder is a parallel prefix adder. Parallel prefix adders are special class of adders that are based on the use of generate and propagate signals. Compared to CLA the propagation delay is the reduced using Brent Kung Adder. Thereby, the design of highly optimized adder in terms of speed. play significant role in the present era and hence this project focuses in the design of same as CLA.

5. IMPLEMENTATION

The use of a normal CMOS technology to implement a logic gate will normally result in a huge delay as each gate is implemented implemented in terms of a universal gate

and then the NOT gate. This is basically because CMOS follows an inverted logic. For example, AND is implemented using NAND gate and a NOT gate. The inputs are given to NAND gate and the output of NAND gate is given as input to the NOT gate.
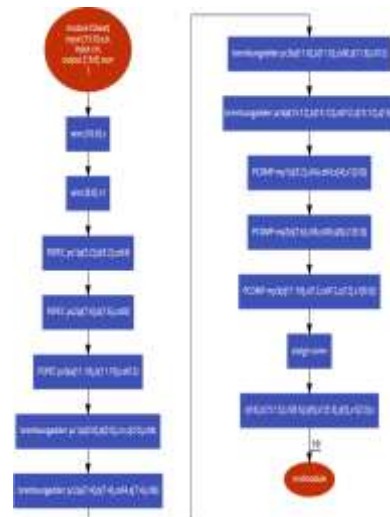
Fig -6: Flow chart of 32-bit pipelined architecture of in-exact speculative adder using CLA

We will be the linux terminal to open the MAGIC tool. First, open a file using the command *magic <filename>.mag* . . The various cells are copied into the design file using the command *getcell <filename>* (Example; *getcell And*, where 'And' implies 'And.mag' which is the magic file for the And gate for the design under consideration).

To obtain the total time delay in obtaining the output from the input we can use the command *path input node output node*. For example, to find the delay between input 'b1' and output 'sum7' we give the command '*path b1 sum7*'.

6. RESULTS AND DISCUSSIONS

The proposed venture is simulated and tested their functionality. Once the useful verification is done, the RTL model is taken to the synthesis technique the use of the Xilinx ISE device. In synthesis process, the RTL model may be transformed to the gate level internet listing mapped to a particular era library. Here on this ISE challenge navigator of Spartan 3E family, many distinctive devices were to be had inside the Xilinx ISE device. In order to synthesis this layout the tool named as "XC3S500E" has been chosen and the package deal as "FG320".

Fig- 7: RTL block of implemented adder using CLA

Fig-8: Schematic diagram of 32-bit pipelined In-exact Speculative adder using carry look ahead adder

Fig-9: Input/output waveform simulation of implemented 32-bit pipelined in-exact speculative adder using Carry look ahead adder.

Fig-10: Simulation of implemented adder based unsigned values

7. CONCLUSION

In this paper, we provided excessive-pace and coffee-strength model of the modern-day ISA layout. This structure has been nice grain pipelined and clock gated to enhance speed and alleviate strength intake respectively. Experimental consequences confirmed that the counseled ISA may want to function in Xilinx model. Thereby, such layout would truely play extensive role inside the layout of modern as well as future electronic gadgets for IoE and many other contemporary programs. However, the location problem may be resolved to some extent with the aid of the use of decrease era nodes inside the design procedure.

8. FUTURE SCOPE

The design can be in addition more suitable for sixty four bit as properly 128 bit. Even different design variants also can be tried for even better evaluation. In fact through combining the numerous tree adders in addition to the technology used to put into effect them, a completely suitable adder with massive much less postpone can be completed**.**

REFERENCES

[1]. High-Speed and Low-Power VLSI- Architecture for Inexact Speculative Adder, Rahul Shrestha, Member, IEEE. School of Computing & Electrical Engineering, Indian Institute of Technology (IIT) Mandi.

[2].software implementation on embedded processors," in International Conference on Multimedia and Expo (ICME), 2015 IEEE, 2017.

[3]. V. Camus et al., "Energy-efficient inexact speculative adder with excessive overall performance and accuracy control," in Circuits and Systems (ISCAS), 2015 IEEE International Symposium, 2017, pp. 45–forty eight.

[4]. X. Jiao et al., "Supervised mastering based version for predicting variability induced timing mistakes," in New Circuits and Systems Conference (NEWCAS), 2015 IEEE 13th International, 2016, pp. 1–four.

[5] R. Ragavan et al., "Adaptive over clocking and errors correction based on dynamic hypothesis window," in Symposium on VLSI (ISVLSI), 2015 IEEE Computer Society Annual, 2016, pp. 325–330.

[6] X. Jiao et al., "Wild: A workload-based mastering model to expect dynamic postpone of purposeful devices," in Computer Design (ICCD), 2016 IEEE thirty fourth International Conference on, 2016

[7]. A New Approximate Adder with Low Relative Error and Correct Calculation J. Hu and W. Qian, in Design, Automation and Test in Europe(DATE), 2015 IEEE Conference and Exhibition on, March 2015

[8]. Performance Improvement with Circuit-level Speculation, T. Liu and S. L. Lu, 33rd Annual IEEE ACM International Symposium on - architecture(MICRO-33), pp. 348-355, 2000.

[9] F. C. Cheng, S. H. Unger, M. Theobald, and W. C. Cho, "Delay-Insensitive Carry-look ahead Adders", VLSI Design Proceedings, 1997, pp. 322-328.

[10]J. Lim, D. G. Kim, and S. I. Chae, "A sixteen-bit carry-appearance in advance adder using reversible energy recovery good judgment for extremely-low-power structures", IEEE Journal of Solid-State Circuit