International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 07 Issue: 03 | Mar 2020 www.irjet.net p-ISSN: 2395-0072

Design and Analysis of a SEPIC Integrated Boost (SIB) Converter using Coupled Inductor

Gajalakshmi M[1], Dr Karpagavalli P[2]

[1]*Gajalakshmi M, M.E. Power Electronics & Drives, Government College of Engineering, Salem, Tamilnadu, India*
[2]*Dr P Karpagavalli, Associate Professor, Government College of Engineering, Salem, Tamilnadu, India*

Abstract - *In this paper, design of a SEPIC integrated Boost (SIB) converter using coupled inductor is presented. The proposed converter has various advantages such as lower voltage stress on the switches, non-inverting output voltage, high efficiency, and high voltage gain. It is difficult to operate at higher duty ratios and hence achieve high-voltage transfer gains .Without using transformer, the high output voltage gain is achieved. In the proposed converter, the converter can be controlled easily in the continuous conduction mode (CCM). Due to the gate pulses given for the two switches are similar, it has obtained a wide output voltage range by adjusting only the duty cycle. This effect allows low conduction losses by using lower voltage rating switches and also additional clamping circuit is not needed. The detailed operation of the introduced converter is discussed. Simulation results for the open and close loop topology are compared and presented to verify the performance of the proposed SIB DC-DC converter.*

***Key Words*: SEPIC integrated Boost (SIB), DC-DC Converter, CCM, Coupled inductor**

1. INTRODUCTION

As renewable energy becomes increasingly important and prevalent in worldwide power generation systems nowadays, dc–dc step-up converters have been frequently adopted for low-power conversion applications [1]. The converter can be easily controlled in CCM mode operation. Because the gating pulses for both of the switches are the same and a wide output voltage range is achieved only by changing the duty cycle. The number of the components and the voltage stress across the switches are less than the other non-coupled inductor SEPIC- based converters which provide near voltage gain to the proposed converter. [1].

The high static gain concept is achieved by voltage divider technique with the modified SEPIC converter structure is discussed in the paper [2].In the paper [3], it consists of two switches and its duty cycle .It has advantages:

(i) The two switches in the proposed converter operates with same duty ratios is to attain high voltage gain

(ii) The stored inductor energy is supplied to the load without additional clamping circuit;

(iii) Reduced voltage stress on the diodes and switches

Different types of isolated dc dc converter topologies are proposed in the literature to determine a high voltage gain [4] [13]. The serious problem oriented with this type of the converter is transformer core saturation. Hence, non-isolated dc dc converters are used in order to improve the voltage gain with reduced cost and size, since it does not have galvanic isolation. Such converters are quadratic boost [6], Cascade boost [10], the switched-capacitor technique [4] and the conventional sepic converter integrated with voltage lift techniques [15]. The inclusion of switched capacitor a switched-inductor stage increases the cost and complexity of the circuit. [16].

Due to its simple structure of a coupled inductor with boost converter design it is recommended for low to medium power applications. Since it has a major drawback of input side discontinuous current as it is in boost converter. It needs additional circuit to suppress the voltage spike at switch [4]. The comparison of boost, buck, buck boost, CUK converters is discussed and its voltage stress across the semiconductor elements and the number of components [5]. As described in the papers [4] [5], the efficiency and voltage gain of dc–dc boost converter are restrained by either the parasitic effect of power switches or the reverse-recovery issue of diodes.

The cascaded high step up dc dc converter is used to improve the voltage gain of the converter interfacing through the dc ac inverter. It deals with the main electricity grid. It termed as a quadratic boost converter which is the combination of the boost and fly back converter [6] [7]. Although an alternative solution is the dc–dc flyback converter along with some advantages such as simple structures, easy control, and cost effective, the energy of leakage inductor of the transformer leads to low efficiency and high-voltage stress across the active switch.

The main advantages are to avoid more switches or multiple switches since it formed complex structure. In the VL

techniques, these are segregated by re-lift circuit, self-lift circuit, triple lift and quadruple lift circuit. All circuits perform positive to positive DC–DC voltage increasing conversion with higher voltage transfer gains, small ripples and high efficiency in simple structures. Therefore they will be used in computer peripheral equipment and industrial applications, especially for high output voltage projects. [11].In series Sepic converter with voltage lift technique converter are used because of its suitable advantages discussed further. However, it has both inductor and capacitors plays important roles in the VL technique, and using external power source, inner capacitors are charged fully. Moreover, it has lesser power switches i.e. one or two synchronous switches are implemented in Voltage lift techniques [12] [13].

Considering the main limitations of the classical boost converter, several works have been proposed in the literature to improve key issues, such as the static gain, voltage stress across the semiconductors, efficiency, power capacity and many other aspects of the original topology. By adopting coupled-inductor and switched-capacitor techniques [13],it has increase the voltage transfer gain without a high turns ratio of the coupled inductor. In a switched capacitor and a switched coupled inductor in a single converter has been implemented in the paper [13], it has very simple circuit design. It has even more advantages as its turns ratio of the coupled inductor can be also reduced. It has lower conduction loss and higher power conversion efficiency.

The proposed converter is simply composed of six components, which can be further derived to varied converters for different purposes, such as bidirectional converter [17] .The so-called quadratic converters allow obtaining high-voltage step-up or step-down by simply considering that the total static gain is equal to the product between the static gains of two individual converters.

In the writing, various non-confined high-gain DC–DC converter topologies with voltage boosting strategies have been talked about, few of them are cascaded boost [11], quadratic lift [12], and switched inductor (SI)/capacitor (SC) [13]. In cascaded boost converter, the high-voltage gain has been accomplished with more segments, thereby expanding the system complexity and results in poor proficiency [14]. In this converter [15], the level of the voltage stress on the diodes and switches concerning the yield voltage are less.

The proposed converter has high voltage gain by choosing appropriate duty cycle for the two switches and by planning legitimate inductor and capacitor esteems. It has the accompanying points of interest: (I) the two switches in the proposed converter works with same duty ratios to accomplish high voltage gain; (ii) the stored inductor energy is provided to the load without extra clamping circuit; (iii) the voltage gain accomplished by the proposed converter is more prominent than the traditional boost converter (iv) diminished voltage stress on the diodes and switches dependent on the rate yield voltage; and (v) the proposed converter is fit for accomplishing high voltage gain without Voltage Multiple Cell as well as hybrid switched capacitor techniques.[18]

2. PROPOSED HIGH GAIN CONVERTER TOPOLOGY:

The proposed SEPIC integrated boost converter circuit diagram is given below Fig. 1. The Current and Voltage of the components are shown. Some assumptions are made to simplify the steady state analysis as follows:

1) The switches, diodes and other components in the circuit are kept ideal.

2) All capacitors are large enough so that the voltage across them is constant during one switching period.

3) The number of turns in the 2 inductors is L_1 and L_3 are different. It acts as a coupled inductance in the proposed circuit.

4) The average inductor voltages are zero and the average capacitor currents are zero for the steady state analysis. The steady state analysis of CCM mode is discussed as follows.

The proposed high increase DC-DC converter appeared in Fig-1 comprises of two dynamic switches M_1 and M_2 , three inductors L_1 and L_3 are coupled inductors and ,L_2 as inductor, two diodes D_1 and D_2 and three capacitors C_1,C_2 and C_0. The switches M_1 and M_2 works at a switching frequency of fs. The duty ratio of the switches M_1 and M_2 is D. The Proposed SIB circuit diagram is shown in the fig 1. The leakage inductance in the coupled inductance can be used to limit the diode current falling rate, thus minimizing the diode reverse-recovery problem.

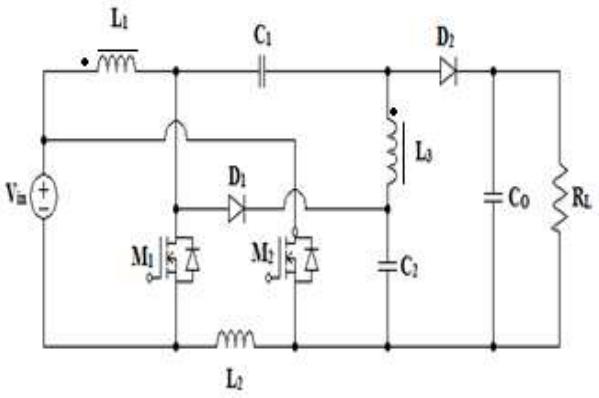


Fig-1: Proposed SIB circuit diagram

3. MODES OF OPERATION:

Based on the aforementioned assumptions, there are two operating modes in one switching period of the proposed converter under CCM. The operating modes of the proposed Converter in continuous conduction mode (CCM) is discussed. The operating modes are described as follows.

***Mode 1 (0<t<DTs)*:** At the beginning of this mode, the MOSFET switches M_1 and M_2 are turned on simultaneously. The diodes D_a and D_o are blocked and the source energy is transferred to the inductors L_1, L_2, and L_3. The input voltage V_{in} is across the input inductors L_1 and L_2 while they are in parallel. The energy stored in the output capacitor C_o is discharged to the load. The voltages across L_1 and L_2 are obtained as

$$V_{L_1} = V_{L_2} = V_{in} \quad (2)$$

And the voltage ($V_{C_2} - V_{C_1} + V_{in}$) is across the inductor L_3.

$$V_{L_3} = V_{C_2} - V_{C_1} + V_{in} \quad (3)$$

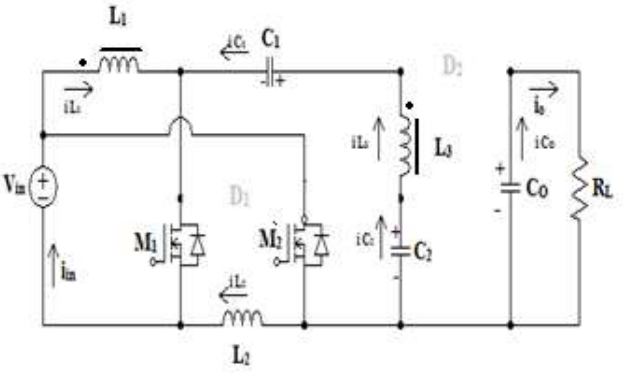


Fig-2(a): Mode 1 : Proposed SIB circuit diagram

Mode 2 (DTs <t<Ts): In this mode, the switches M1 and M2are turned off and the diodes D_1 and D_2 are turned on. The current flow path in this mode is illustrated in Fig. 2(b). The source energy iL_3 and the input inductors L_1 and L_2 are in series and their energies are transferred to the load by the output diode D_2 and also to the auxiliary capacitor C_2 by the auxiliary diode D_1. Also, the energy stored in the inductor L3 is transferred to the output by the diode D_2. The currents and turns ratio of the input inductors are equal.

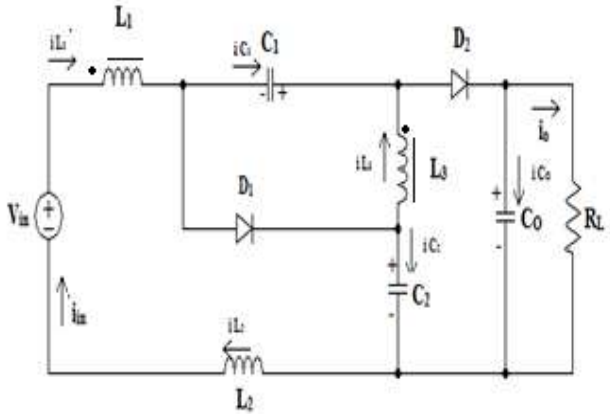


Fig 2(b): Mode 2 of Proposed SIB circuit diagram

Thus, voltages across L_1 and L_2 in this mode are obtained as (4).

$$VL_1 = VL_2 = \frac{(V_{in} - Vo + Vc_1)}{2} \quad (4)$$

Also, the voltage across the L_3 is given by,

$$VL_3 = -VC_1 \quad (5)$$

The voltage transfer gain M in CCM operation can be found as follows.

$$M = \frac{V_o}{V_{in}} = \frac{3D+1}{1-D} \quad (6)$$

The input current is calculated according to (7). However, in the real case, the components are not ideal and equation (7) is divided by the efficiency η of the converter.

$$I_{in} = \frac{3D+1}{1-D} I_O \quad (7)$$

MODE 3: DCM operation

The proposed converter will operate in DCM if the current i_{D2} reduces to zero during the switching-off interval. Therefore the proposed converter operation can be divided into three modes under DCM operation. Mode 1 and Mode 2 are the same as those of CCM operation, and in Mode 3, the switches M_1 and M_2 and the diodes D_1 and D_2 are turned off and also the voltage across the inductors L_1, L_2, and L_3 are approximately zero.

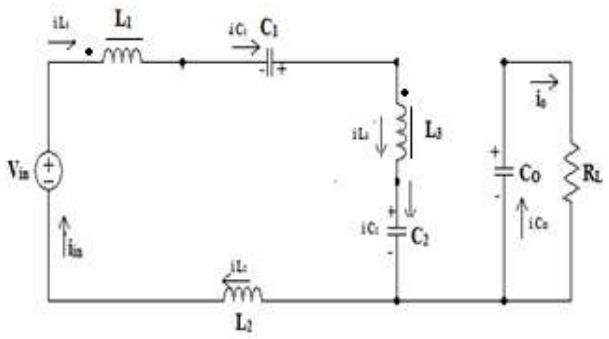


Fig 3 : Mode 3 of Proposed SIB circuit diagram

4. SIMULATION RESULTS AND DISCUSSION

The proposed SIB converter topology is simulated in the open and closed loop by the MATLAB/Simulink environment as shown in the Fig 4 and Fig 5.

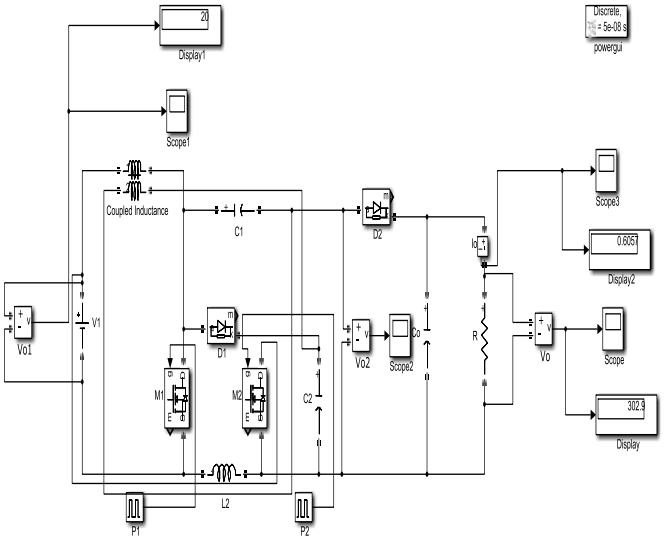


Fig 4: Simulation diagram of Open loop Proposed SIB converter

For the proposed converter , the values of the capacitors C1 and C2 are taken as same of 4 μF .The output capacitor Co value is taken as 15 μF . The waveforms of the converter while operating in CCM at 40 kHz switching frequency with 74.2% duty cycle The simulation parameters are shown in the table 1.For the open loop circuit, the input voltage is given as 20V ,it achieved an output voltage as 239V. And for the closed loop PI circuit, the same input voltage is given as 20V, it gives the result of 249V.The comparison between the open and closed loop of the proposed converter are done using simulation environment. Higher efficiency is achieved from the closed loop structure of proposed system than the open loop structure of proposed system

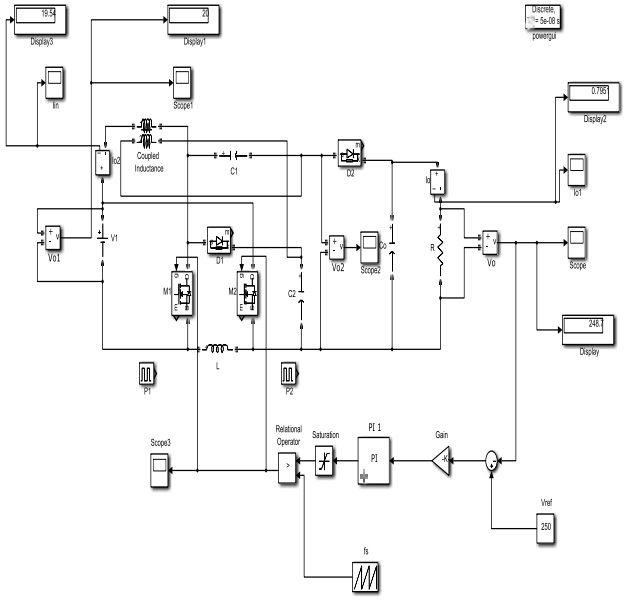


Fig 5: Simulation diagram of Closed loop Proposed SIB converter

The output waveforms of the voltage V_o and Current I_0 for the proposed open loop converter configuration are shown in Fig. 6(a) and (b) respectively. The output waveforms of the voltage V_o and Current I_0 for the proposed closed loop converter configuration are shown in Fig. 7(a) and (b) respectively .It shows the effective output voltage for the closed loop topology which is similar to the theoritical value.The current value of the open loop and closed loop topology is 0.45A and 0.8A respectively. The waveform of current through the capacitor C_0 is shown in the Fig. 8.

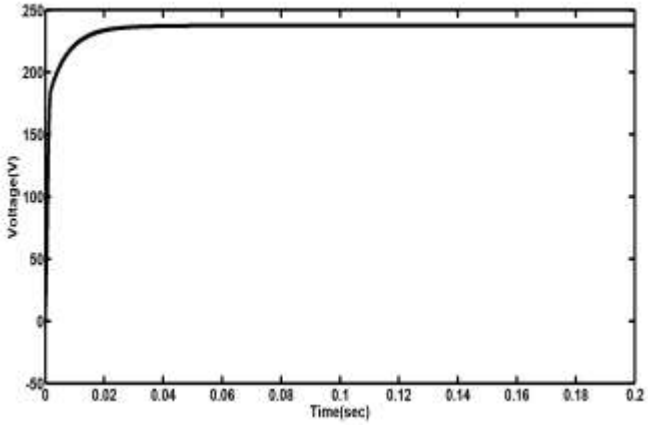


Fig 6(a): Output voltage waveform of the proposed open loop converter topology

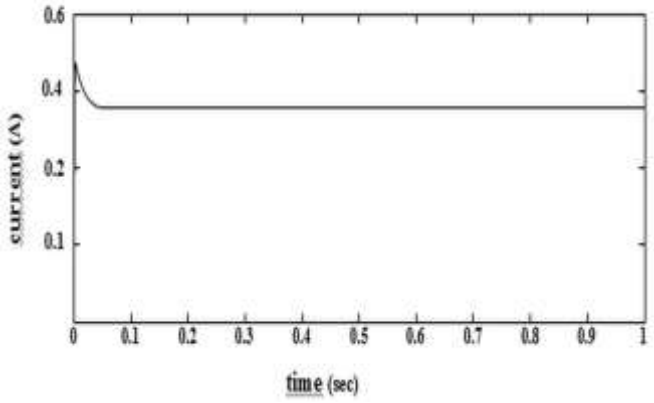


Fig 6(b): Output current waveform of the proposed open loop converter topology

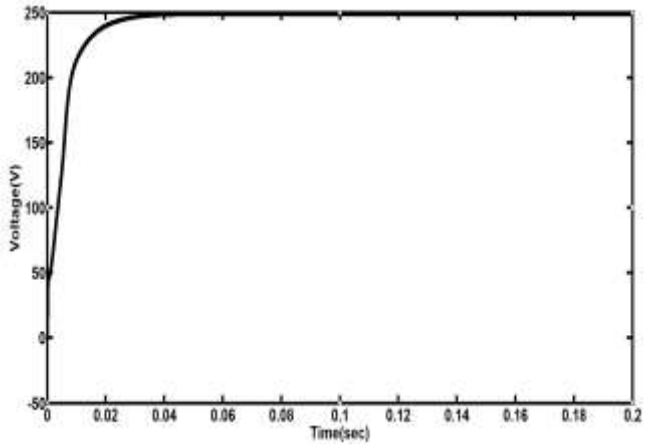


Fig 7(a): Output voltage waveform of the proposed open loop converter topology

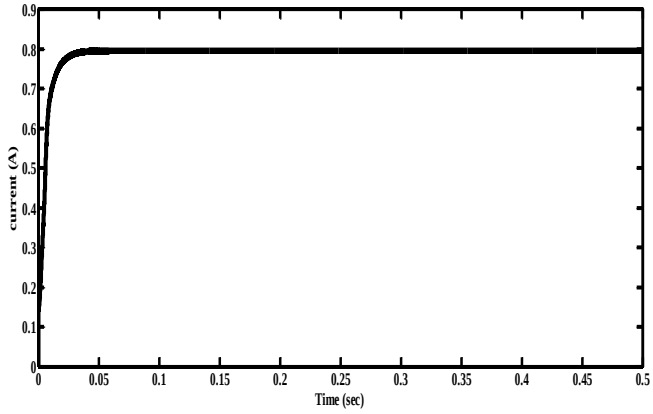


Fig 7(b): Output current waveform of the proposed open loop converter topology

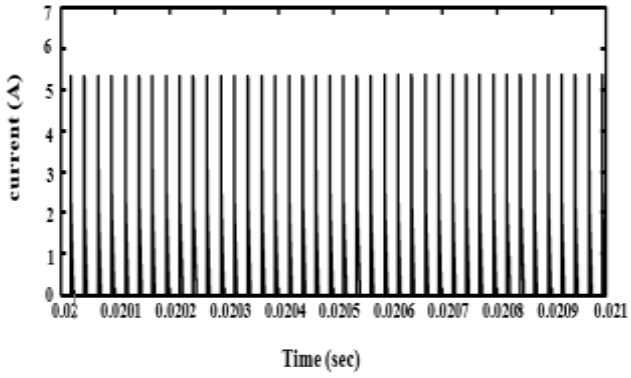


Fig 8: Waveform of current through the capacitor C_0

The below waveforms Fig 9(a) and Fig 9(b) are shown for the gate pulse for the switch M_1 and M_2 .

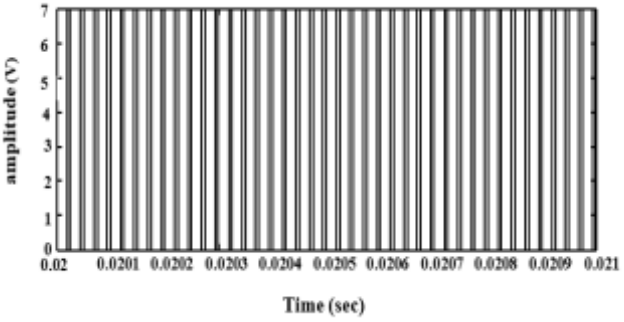


Fig 9(a): Gate pulse to the switch M_1 of the proposed converter

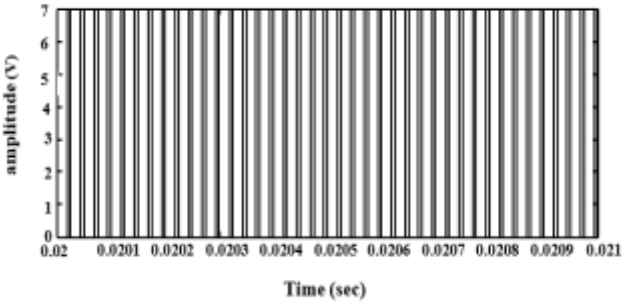


Fig 9(b): Gate pulse to the switch M_2 of the proposed

The input current is twice the value of the inductor current $iL1$ (or $iL2$) when switches M_1 and M_2 are ON and the input current is equal to the inductor current i_{L1} (or i_{L2}) when switches M_1 and M_2 are OFF. The output voltage of 250V is obtained from the simulated environment for the input voltage of 20V. It has 12.5 times of voltage gain is achieved from the simulated values which is similar to that of theoretical value of the proposed converter. The output

waveform of the voltage and the current of the proposed converter are also discussed for both open and closed loop design. By comparing the open and closed loop structure the below tabulation Table 1 are done for given input values.

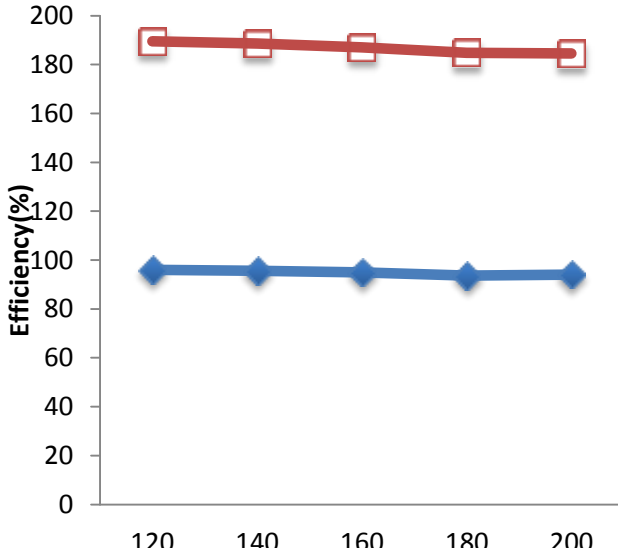
Table -1: Comparison tabulation for proposed SIB open & closed loop converter topology

Proposed SIB converter Parameters	Input Voltage(V)	Output Voltage(V)
Theoretical value	20V	250V
Simulation Value of Open loop topology	20V	239V
Simulation Value of Closed loop topology	20V	249V

Table -2: Simulation parameters of proposed SIB converter.

Circuit parameters of proposed converter. Symbol	Quantity	Value
Po	Output power	200 W
V_{in}	Nominal input voltage	20 V
V_o	Output voltage	250 V
fs	Switching frequency	40 kHz
L_1,L_3	Coupled inductor	123 µH ,246
L_2	Third inductor	246 µH
C_1, C_2	Main capacitors	4 µF
Co	Output capacitor	15 µF

In order to verify the proposed converter, a prototype of 200W has been built which is shown in Table 2.In the Table 1, the comparison study is made between open and closed loop topology of the proposed SIB converter. Considering the closed loop proposed SIB converter, its waveforms of the converter while operating in CCM at 40 kHz switching frequency with 74.2% duty cycle .The output current i_o, the output voltage V_o, and the voltage of the auxiliary capacitor V_{C1}. The voltage gain with 74.2% duty cycle is approximately 12.5 and the output voltage is 249V.The output voltage ripple with the output capacitor of 15µF will be less than 1V which is acceptable. The output current is 0.8A, which indicates that the output power is 200W. However, considering them does not influence on the voltage gain considerably. In addition, from this figure, it can be observed that, the input current is continuous. Therefore, the proposed converter is suitable for renewable energy applications.



As the result, in Fig. 10, the power efficiency curve of the proposed converter is demonstrated and compared with open and closed loop topology of proposed SEPIC-based boost converter. In addition, with the similar parameters with the PI controller , closed loop structure achieved highest efficiency. Finally, the experimental results and efficiency comparison were presented to validate the advantages of the proposed converter.

5. CONCLUSIONS

In this paper, a SEPIC Integrated Boost (SIB) converter is proposed. The introduced converter is simple and modification of the SEPIC converter is accomplished by adding only four components. The proposed converter has many advantages such as continuous input current, very high voltage gain, non-inverting output voltage, and simple control system. Moreover, the very high voltage gain is achieved without using any transformers and coupled inductors. Therefore, there is not any voltage overshoot across the switches and no clamping circuit is needed. This effect reduces the conduction losses by using lower voltage switches with lower Rds(on) and allows more compact design. The steady-state analysis of the converter under CCM and DCM operation and design considerations has been presented. The voltage gain, voltage stress on the switches and diodes, and the number of the elements are compared between the proposed converters. According to the presented results, the voltage gain of the proposed converter is higher than the other topologies. Also, the percentage of the voltage stress on the switches with respect to the output voltage is less in the proposed converter. In addition, the total number of the elements in the suggested converter is less than the other converters which provide near voltage gain to the introduced converter. Finally, the simulated results and

efficiency comparison were resented to validate the advantages of the proposed converter.

REFERENCES

1. Sajad Arab Ansari and Javad Shokrollahi Moghani "A Novel High Voltage Gain Non-coupled Inductor SEPIC Converter," ieee transactions on industrial electronics, 2018.

2. Priscila Facco de Melo, Roger Gules,Eduardo Felix Ribeiro Romaneli,and Rafael Christiano Annunziato "A Modified SEPIC Converter for High Power Factor recitier and universal Input Voltage Applications," ieee transactions, vol. 25, no. 2, February 2010.

3. M. Lakshmi and S. Hemamalini, "Non-isolated High Gain DC-DC Converter for DC Microgrids," IEEE transactions on industrial electronics, 2017.

4. Shih-Ming Chen, Tsorng-Juu Liang ,Lung-Sheng Yang,nd Jiann-Fuh Chen, "A Cascaded High Step-Up DC–DC Converter With Single Switch for Microsource Applications," ieee transactions on power electronics, vol. 26, no. 4, April 2011.

5. Ali Ajami, Hossein Ardi, and Amir Farakhor,"A Novel High Step-up DC/DC Converter Based on Integrating Coupled Inductor and Switched-Capacitor techniques for Renewable Energy Applications," IEEE Transactions on Power Electronics 2018

6. K.C. Tseng and T.J. Liang "Novel high-efficiency step-up converters," IEE Proc.-Electr. Power Appl., Vol. 151, No. 2, March 2004.

7. R. Nicole, "Title of paper with only first word capitalized," J. Name Stand. Abbrev., in press.

8. K. Elissa, "Title of paper if known," unpublished.

9. Mojtaba Forouzesh, Keyvan Yari, Alfred Baghramian and Sara Hasanpour, "Single-switch high step-up converter based on coupled inductor and switched capacitor techniques with quasi-resonant operation," IET Power Electronics.

10. F. M. Shahir, E. Babaei, and M. Farsadi, "Analysis and design of voltage-lift technique-based non-isolated boost dc–dc converter," IET Power Electronics, vol. 11, DOI 10.1049/iet-pel.2017.0259, no. 6, pp. 1083-1091, Nov. 2017.

11. K.-B. Park, G.-W. Moon, and M.-J. Youn, "Nonisolated high step-up boost converter integrated with sepic converter," IEEE Transactions on Power Electronics, vol. 25, DOI 10.1109/TPEL.2010.2046650, no. 9, pp. 2266-2275, Sep. 2010.

12. H. Ardi, A. Ajami, and M. Sabahi, "A Novel High Step-Up DC–DC Converter with Continuous Input Current Integrating Coupled Inductor for Renewable Energy Applications," IEEE Transactions on Industrial Electronics, vol. 65, DOI 10.1109/TIE.2017.2733476, no. 2, pp. 1306-1315, Feb. 2018.

13. R.-J. Wai, C.-Y. Lin, R.-Y. Duan, and Y.-R. Chang, "High-efficiency DC-DC converter with high voltage gain and reduced switch stress," IEEE Transactions on Industrial Electronics, vol. 54, DOI 10.1109/TIE.2006.888794, no. 1, pp. 354-364, Feb. 2007.

14. D. W. Hart, Power electronics, 1rd ed, ser. series 1, vol. 1, ch. 7, pp. 196-259, The address of the publisher: Tata McGraw-Hill Education, Feb. 2011.

15. A. Ajami, H. Ardi, and A. Farakhor, "A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications," IEEE Transactions on Power Electronics, vol. 30, DOI 10.1109/TPEL.2014.2360495, no. 8, pp. 4255-4263, Aug. 2015.

16. S.-M. Chen, M.-L. Lao, Y.-H. Hsieh, T.-J. Liang, and K.-H. Chen, "A novel switched-coupled-inductor DC–DC step-up converter and its derivatives," IEEE transactions on industry applications, vol. 51, DOI 10.1109/TIA.2014.2332642, no. 1, pp. 309-314, Jan. 2015.

17. M. Mohammadi, M. Taheri, J. MiliMonfared, B. Abbasi, and M. R. M. Behbahani, "High step-up DC–DC converter with ripple free input current and soft switching," IET Power Electronics, vol. 7, DOI 10.1049/iet-pel.2013.0881, no. 12, pp. 3023-3032, Nov. 2014.

18. M.-K. Nguyen, T.-D. Duong, Y.-C. Lim, and Y.-J. Kim, "Isolated boost DC–DC converter with three switches," IEEE Transactions on Power Electronics, vol. 33, DOI 10.1109/TPEL.2017.2679029, no. 2, pp. 1389-1398, Feb. 2018.

19. M. A. Salvador, T. B. Lazzarin, and R. F. Coelho, "High Step-Up DC–DC Converter With Active Switched-Inductor and Passive Switched-Capacitor Networks," IEEE Transactions on Industrial Electronics, vol. 65, DOI 10.1109/TIE.2017.2782239, no. 7, pp. 5644-5654, Jul. 2018.

20. F. L. Tofoli, D. de Castro Pereira, W. J. de Paula, and D. d. S. O. J□nior, "Survey on non -isolated high-voltage step-up dc–dc topologies based on the boost converter," IET power Electronics, vol. 8, DOI

10.1049/iet-pel.2014.0605, no. 10, pp. 2044-2057, Jul. 2015.

21. Y. Berkovich and B. Axelrod, "Switched-coupled inductor cell for DC–DC converters with very large conversion ratio," IET power electronics, vol. 4, DOI 10.1049/iet-pel.2009.0341, no. 3, pp. 309-315, Mar. 2011.

22. W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," IEEE Transactions on Industrial Electronics, vol. 58, DOI 10.1109/TIE.2010.2049715, no. 4, pp. 1239-1250, Apr. 2011.

23. F. L. Luo and H. Ye, "Positive output cascade boost converters," IEE Proceedings-Electric Power Applications, vol. 151, DOI 10.1049/ip-epa: 20040511, no. 5, pp. 590-606, Sep. 2004.

24. M. R. Banaei and S. G. Sani, "Analysis and implementation of a new SEPIC-based single switch buck-boost dc-dc converter with continuous input current," IEEE Transactions on Power Electronics, DOI 10.1109/TPEL.2018.2799876, Jan. 2018.