LOW POWER ADDER AND MULTIPLIER CIRCUITS DESIGN OPTIMIZATION IN VLSI

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Abstract - *Designing multipliers which might be of high-speed, low power, and regular in the format are of big studies interest. The Speed of the multiplier can be expanded by lowering the generated partial products. This paper describes an efficient method to lay out a 4-bit multiplier having low power, area and excessive velocity using the Dadda set of rules and the basic building block of multiplier's used a 14T Full adder having low power dissipation. Full and half adder blocks were designed the usage of 4T XOR gate to minimize the electricity. Design and Implementation using faster Dadda set of rules to reduce the propagation delay. Further reduction in the glitches and thermal dissipation of the circuit will maximize the output efficiency. Full adder and half adder blocks have been designed for the usage of pass-transistor logic and using CMOS process technology to minimize the electricity dissipation and propagation delay. We have also implemented the Faster Dadda set algorithm to minimize the propagation delay. Reducing power dissipation, thermal dissipation, propagation delay, glitches will boost the efficiency of the circuit up to 93% of maximum operating boost-up. The model has been structured using Mentor Graphics Tanner v2019.02, ModelSim Altera v17.1, Microwind Lite DSCH v3.5.*

Key Words: **CMOS, Dadda Algorithm, Full Adder, Half Adder, Multiplier, Power, Propagation Delay, Speed, AND, OR, XNOR, XOR, VLSI.**

1. INTRODUCTION

The advancement in the area of CMOS generation has motivated the studies to implement greater and more complicated signal processing structures on a VLSI chip. Adder and Multiplier circuits are widely used in ALU, Graphical and Image Processing units, and in the implementation of multimedia algorithms. These circuits are designed with the basic logic gates implementation which includes AND, OR, NAND, XOR, and XNOR gates respectively. This combinational logic implementation is done using PMOS and NMOS transistor logic devices. The basic necessities of these signal processing units are to consume less energy. The chip area, speed, and power intake are considered to be the criteria for comparing the excellent of the system. The growth in functionality, operating frequency, and lengthy battery existence has made a low strength transportable electronic gadget pragmatic in the latest years. The reduction in strength consumption of a system increases its battery existence. Building blocks used in multipliers are a full adder and a half adder. Different design implementations of a full adder and half adder circuits were used to reduce energy and delay in order to design an optimized multiplier circuit which includes Skipping transistor good judgment, CMOS manner technology, split percentage data-driven common sense and CMOS method technology. Besides this, distinctive multiplication algorithms also had been used to attain optimized energy and postpone product which consists of Dadda, Wallace tree, and Vedic and Booth algorithms. The Recent multiplier used Dadda Algorithm technique. This design operates at high frequency and consumes less energy as compared to previous designs, but still, strength needs to be considerably reduced, so, it will help within the large circuits wherein multiplier itself becomes the building block. In proposed work, a multiplier has been designed in which Full adder and half adder has been used as its building block to lessen the energy dissipation by using Hybrid Full Adder and CMOS technology system.

2. EXISTING SYSTEM

In order to design an optimized multiplier, various designs of a full adder and half adder circuits have been used to reduce power and delay This multiplier circuit is based on the full adder which uses 12 transistors i.e., 12T. The model has AND gate for the multiplication of 4*4 multiplier. Consequently, for the 4*4 multiplication, a total of 16 products are generated. Therefore, it has used 16 AND gates for multiplication. Different techniques such as merged delay transformation, genetic algorithm, evolutionary algorithm, delay path Un-equalization, carry-look-ahead logic, etc. have been used and implemented to design digital circuits. Techniques include pass-transistor logic CMOS process technology, adiabatic static CMOS logic, reversible logic, etc. Multiplier using Pass transistor logic technique is one which uses a reduced number of transistors and offers small node capacitances which produces minimum delay and increase the speed of the circuit.

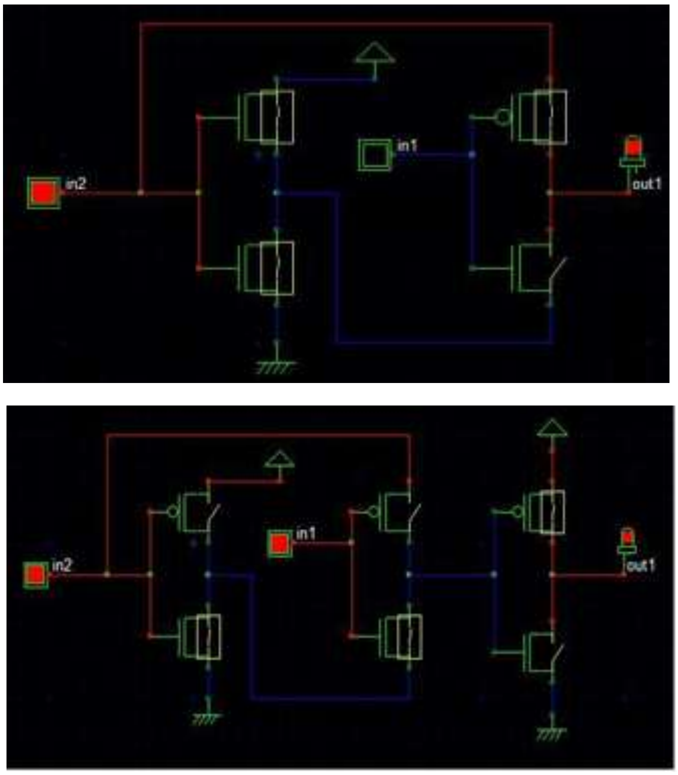
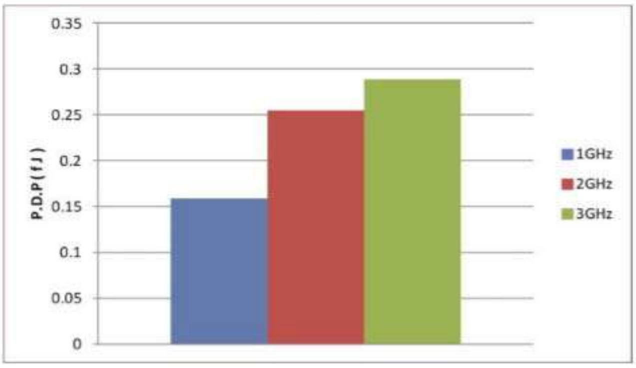


Fig 1. The Existing system design analysis using *p – type* and *n – type* transistors.

The average dynamic power of AND gate at 5GHz is 7.65µW with a delay of 0.05 nS. A full adder is a major block in the multiplier. In existing model Full adder has been modified in order to reduce the propagation delay and also to have less power dissipation in the circuit so that, it can be also used to design optimized multiplier parameters including Power, delay, and less layout area. Four transistors are totally composed for the design of modified XOR module in Full Adder. The buffer is an amplifier having unity gain. Buffer circuit is used to provide drive capability to pass signals to the final stage. Voltage buffer is used to increase the available current for the circuits having low impedance while maintaining the voltage level. On the other hand, current buffers keep the current same and drive the high impedance inputs at higher voltage levels. The average dynamic power of buffer at 3GHz is 6.877µW with a delay of 0.03 nS. Hence, the IC can accommodate more number of transistors.



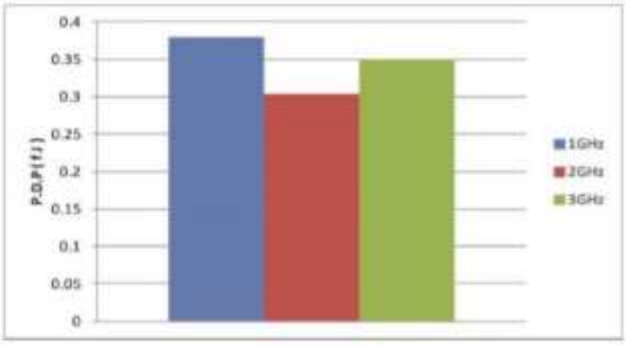


Fig 2. Graphical representation of Power delay product of *Half Adder* and *Full Adder.*

Drawbacks

Improvements can be made in the existing system with respect to the following parameters.

- Transistor count.
- Performance of cascaded transistor.
- Footprints of the IC, since a large number of transistors are used.
- Physical dimensions of the cascaded transistors used.
- Size of the rendered layout and design complexity of transistors.

3. PROPOSED SYSTEM

In the proposed design, a modified circuit consisting of a 4*4 multiplier is proposed. This multiplier circuit is based on the highly optimized full adder which uses 9 transistors i.e., 9T. Hybrid Full Adder design is used for designing. The design consists of two techniques namely, pass-transistor logic, and CMOS process technology. Full adder and half adder circuits have low power delay product and low propagation delay. Three modules of gates have been reduced to two modules with the help of advanced transistor logic. This ultimately results in the design implementation of multipliers having low propagation delay, minimum power dissipation and maximized performance.

4. FASTER DADDA ALGORITHM

The process of multiplication begins with the generation of all partial products, present in parallel using an array of AND gates. The next design process is the partitioning and reduction process. We consider two n-bit operands an-1 an- 2…a2 a1 a0 and bn-1 bn-2…b2 b1 b0 for n by n Baugh-Wooley multiplier, the partial products of two n-bit numbers are aibj where i, j go from 0,1,…n-1. The partial products will form a matrix containing *n* rows and 2*n*-1 columns. It is shown in Fig. 3(a). To each partial product are assigned with a number as shown in Fig. 3(a), e.g. *a0 b0* is assigned as index 0, *a1b0* as index 1 and so on. For convenience it has been rearranged as shown in Fig 3(b).

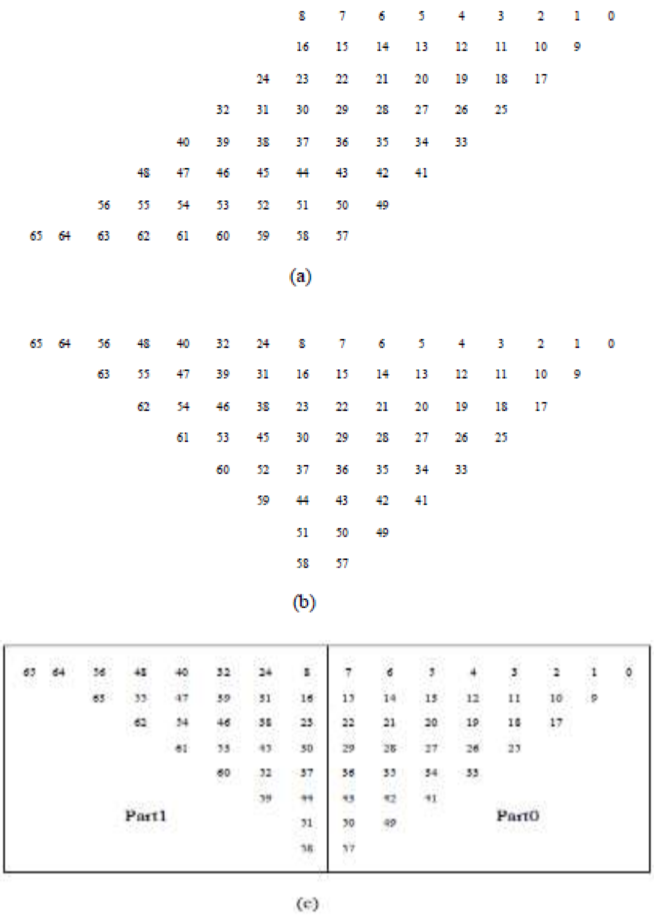


Fig. 3. (a) Partial product array diagram for 8*8 multiplier, (b) An Alternative Representation, (c) Partitioned structure of multiplier.

Based on the regular Dadda reduction as shown in Fig. 4 and Fig. 5, the partial products of each part have been reduced to 2 rows by the using (3, 2) and (2, 2).. The 3-bit and 2-bit grouping indicates (3, 2) and (2, 2) counters respectively. The different colors are used to classify the difference between the columns, where s and c denote partial sum and carry respectively. The sum *s1* of a (3, 2) counter adding *7, 14* and *21*, the *c0* is carried to the next column where it is to be added up. The carry *c1* of (3, 2) is added to the proceeding column. The last two rows of each part are processed using a Carry Look-ahead Adder (CLA) is used to form the partial final product which has been indicated at the bottom of Fig. 4 and Fig. 5.

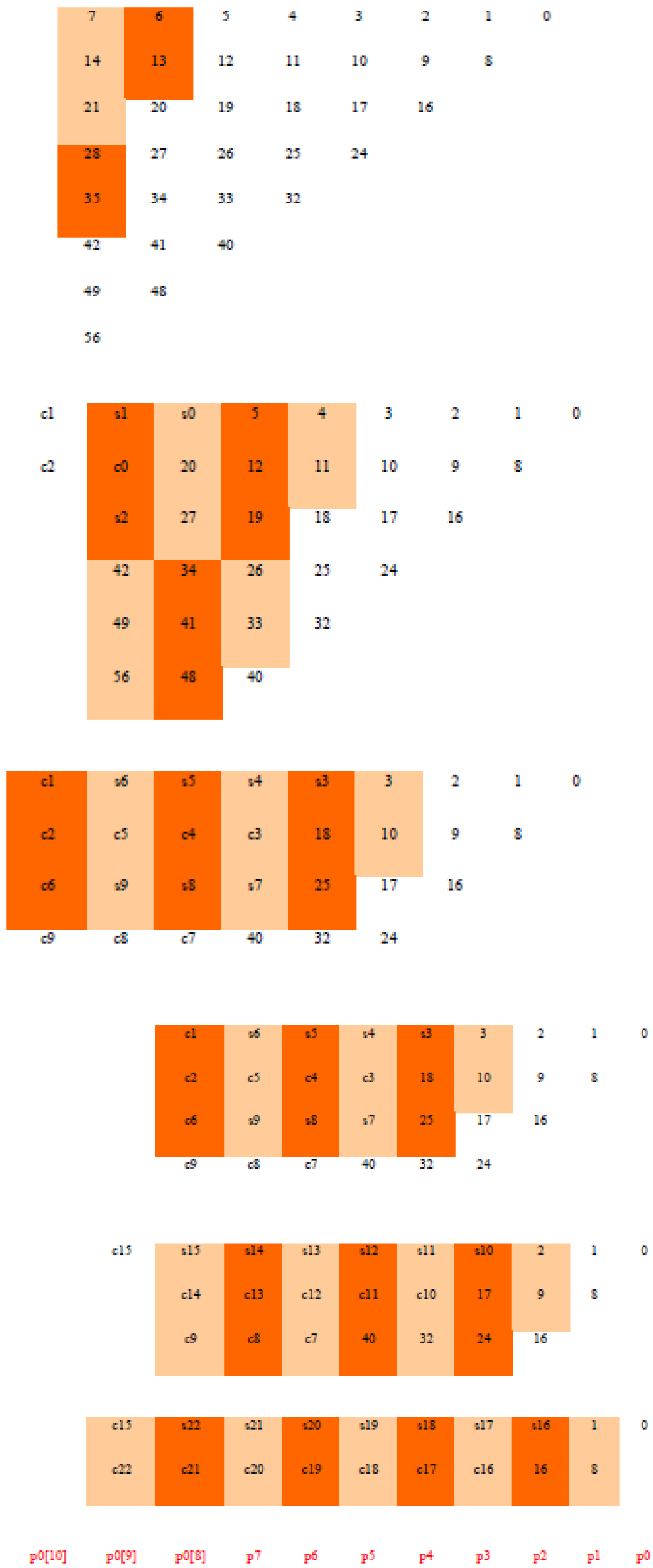


Fig. 4. Reduction of the partial products of part1 based on the Faster Dadda approach.

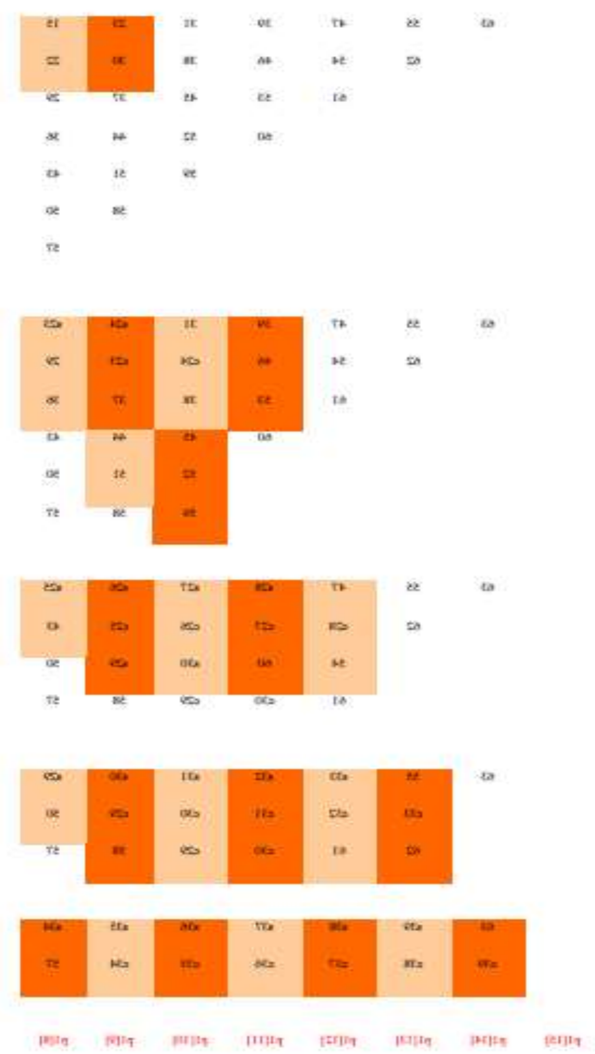
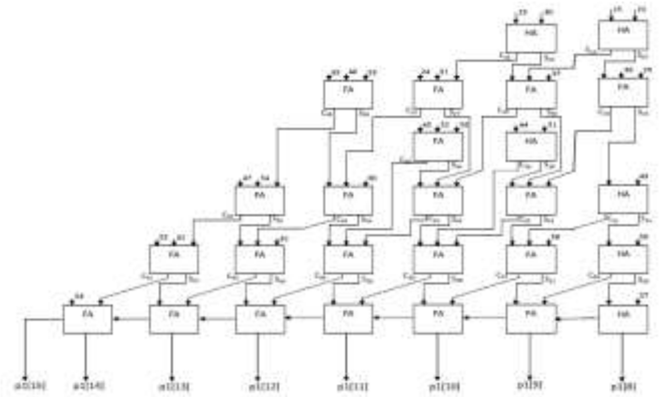


Fig. 5. Reduction of multiplier partial products of part2 based on the Dadda reduction tree.

The two parallel structures for Fig. 4 and Fig. 5 designed using the Dadda approach are shown in Fig. 6, where p0, p1 and p denote Half Adder((2,2)counter)), Full Adder ((3,2)counter), partial final product from part0 and part1 respectively. The numbers on the Half Adder and Full Adder indicates the position of partial products. The output of part 0 and part 1 has been computed independently. To get the final product, those values are added using a high speed hybrid adder. With the increase in the word size, speed improvements, area and power of the partitioned multipliers increases. There is a maximum improvement in delay for the 64-bit multiplier 10.5% with only a slight increase in the 1% area and 1.8% of power.

To further enhance the speed of the proposed multiplier, the reduction in the delay of the Dadda multipliers due to the partitioning of the partial products has been done. By replacing the CLA with the proposed hybrid final adder structure, the further improvement in the performance can be achieved. The hybrid final adder designs were used in previous works to achieve the faster performance in parallel multipliers were made up of Carry Lookahead Adder (CLA) and Carry Select Adder (CSLA). The CSLA occupies more chip area than other adders due to the structure. The proposed hybrid adder uses Multiplexers with Binary to Excess-1 Converters (MBEC) and Ripple Carry Adder for fast summation of input arrival time of the signals originating from the PPST to achieve the optimal performance. The MBEC adder gives optimal performance than Carry Save Adder (CSA) and Carry Look Ahead (CLA) adder. The MBEC consumes less area and power than the Carry Select Adder (CSLA).



(b)

Fig. 6. The Dadda based implementation:

(a) Implementation of part 1 (b) Implementation of part 2

ALGORITHM IMPLEMENTATION:

Faster Dadda algorithm is applied on this tree to reduce its height. First stage is, the tree has a height of 4 which we need to reduce by using full adders and half adders. To reduce the height, we have applied a full adder on the 4th column. To adjust the tree height to 3, we have applied half adder on the 2nd column and two more full adders on the 3rd and 5th column. No one is dependent on the previous stage, since these HA and FA is working in parallel.

BUILDING BLOCKS:

The blocks that are used in the proposed design of Multiplier are explained in detail as follows.

A. AND GATE:

The proposed model has been designed with AND gate for the multiplication of 4*4 multiplier. A total of 16 products are generated for the 4*4 multiplication. The average dynamic power of AND gate at 5 GHz is 7.21µW with a delay of 0.02 nS.

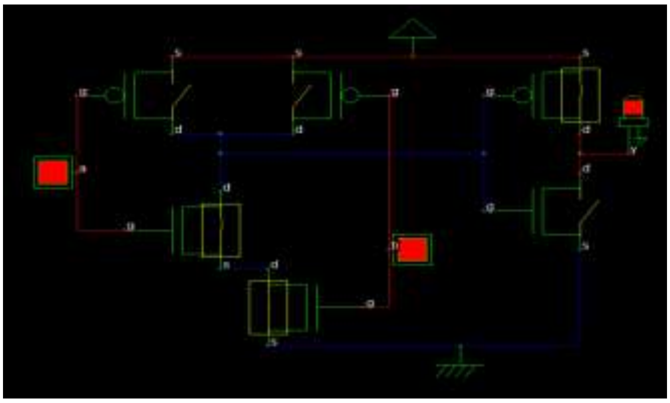


Fig. 7. Schematic of two input AND gates.

B. FULL ADDER:

A full adder is a major building block in the multiplier. In proposed model Full adder has been modified in order to produce minimum propagation delay and less power dissipation of the circuit, so that it can further be used to design multiplier having optimal parameters including Speed, power, delay, and less layout area. Proposed XOR module in the Full adder is designed with four transistors. The average dynamic power of Full adder at 3 GHz is 14.7 μW with a delay of 0.02 nS.

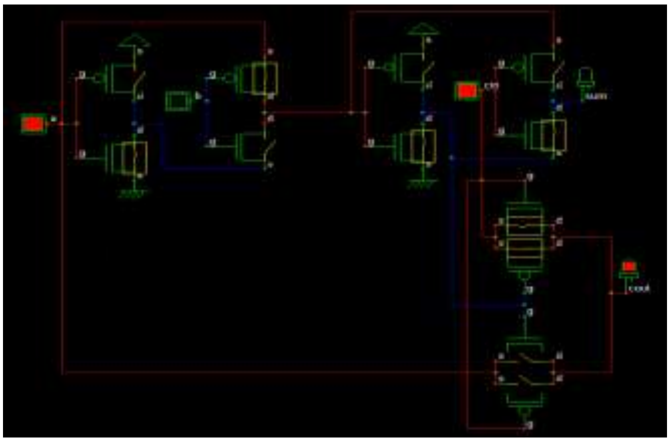


Fig. 8. Schematic of proposed Full Adder design

C. HALF ADDER:

A half adder is major part of designing full adder and multiplier. We have used a total of four half adders for the multiplier design. The average dynamic power of half adder at 3 GHz is 7.90μW with a delay of 0.02 nS.

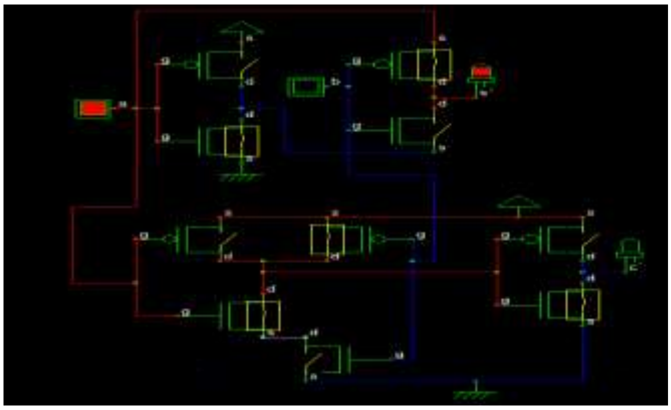


Fig. 9. Schematic of proposed Full Adder design

D. BUFFER:

The buffer is an amplifier having unity gain. Buffer is used to provide drive capability to pass signals to the final stage. For those circuits having low impedance while retaining the voltage level, voltage buffer is used to increase the available current. At higher voltage levels, current buffers keep the current same and drive the high impedance inputs. The average dynamic power of buffer at 3GHz is 6.13μW with a delay of 0.02 nS.

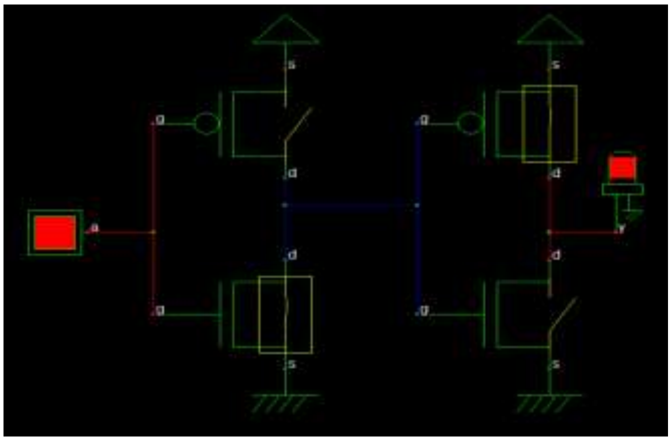


Fig. 10. Schematic of proposed Buffer design

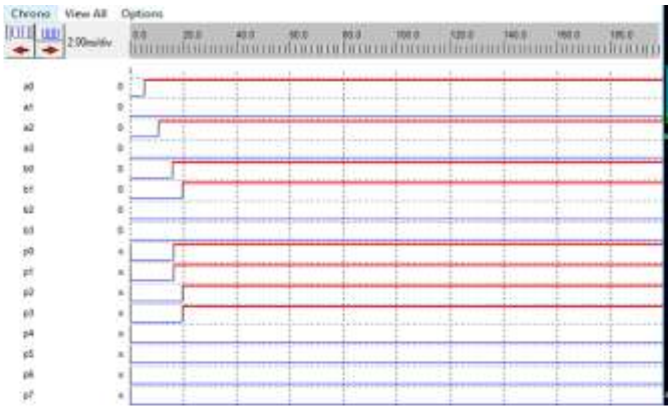


Fig. 11. Simulation of proposed design

5. APPLICATIONS

- The ALU uses half adder to compute the binary addition operation.
- To generate memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU uses Full Adder.
- For graphics related applications, where there is a very much need of complex computations, the GPU uses optimized ALU which is made up of Half Adders, Full Adders and Multipliers.
- In general, all computational logic in IC's are carried out with Half Adders, Full Adders and Multipliers. Thus increasing its performance will have best performance with higher efficiency.

6. CONCLUSION

The proposed model have been designed to have high speed, low latency and minimum delay are being designed which has two modified circuits in it. The design consists of two techniques namely, pass-transistor logic, and CMOS process technology. Hybrid full adder has low propagation delay. So that maximum throughput can be achieved in minimum response time. A high speed 4*4 multiplier has been designed using the hybrid Full adder as its building block and Faster Dadda Algorithm has been applied to achieve this. The proposed 4*4 multiplier operates at a frequency of 3.81 GHz and has an average dynamic power of 171.8 μW with a delay of 0.07 nS which is higher as compared to existing multiplier designs. Multipliers having low latency, minimum power dissipation and less layout area have been designed by the proposed model.

7. REFERENCES

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