LAYOUT DESIGNING OF LESS DELAY FULL ADDER BY EXPLORING NEW XOR AND XNOR GATES USING 32NM TECHNOLOGY IN VERILOG

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ABSTRACT- In this paper XOR-XNOR gates are used in many arithmetic and logical circuits. So, the combination of XOR and XNOR gates by using the full adder we also are used in transmission gate and CMOS inverter to reduce area and power consumption. So, the gates have been designed using 32 nm technology on micro wind 3.1. there is a layout is discussed in this paper. We also proposed circuits XOR and XNOR gates to be used in the full adder circuit. The proposed circuits are investigated in terms of area and power consumption and delay so the full adders are designed to reduce power consumption and chip area occupied by it.

INTRODUCTION:

In this paper, we propose a new design of XOR and XNOR circuits with CMOS inverter. The advantage of the transmission gate has to provide higher speed and lower delay. These circuits are being used in error detection and arithmetic circuits and code converter. The performance of complex logic circuits affected by the XOR and XNOR circuits in VLSI technology the MOS circuits are widely used in many fields. there are two types of mos. i.e NMOS and PMOS. So the NMOS transistor is "ON" when it is the high state.so the PMOS transistor is "on" when it is a low state.

The full adders are used for purpose of addition in many VLSI Circuit such has application with microprocessors, portable devices, etc… so these performances of parameters power consumption, chip area and delay depend on the design full adders and XOR and XNOR gates.

The proposed circuits are designed in the micro wind and the simulations result in the DSCH module. By using this we can see the layout in 2D and 3D of the proposed circuit and also can get resultant output waveforms. The speed and power of a circuits

1. XOR design:

The XOR circuit is consists of 4 transistors so the number of transistors to be designed .so these transistors to vary the area and power consumption and delay. So, in this paper to be considered the 4-transistor circuit.XOR circuit is consists of two inputs and one output. So, the inputs are in1 and in2. And the output is out1. The truth table is consisting of two inputs is the same and the output will be the low state. so the inputs are different and the output will be a high state.

In the below figure of the XOR circuit is designed the simulation of DSCH software. The simulation is continued with the XOR gate. So, the in1=0 and in2=0 so the PMOS transistor is on and the NMOS transistor is off in in1=0. So, the NMOS transistor is off and the PMOS transistor is on in in2=0 conditions. So, the output will be low state i.e. out1=0. So, the in1=0 and in2=1 so the PMOS transistor is on and the NMOS transistor is off in in1=0. So, the NMOS transistor is on and the PMOS transistor is off in in2=1 condition. so, the output will be high state i.e. out1=1. So, the in1=1 and in2=0 so the PMOS is off and the NMOS transistor is on in in1=1. So, the NMOS transistor is off and the PMOS transistor is on in in2=0 conditions. So, the output will be the high state.i.e out1=1. So, the in1=1 and in2=1 so the PMOS is off and the NMOS transistor is on in in1=1. So, the NMOS transistor is on and the PMOS transistor is off in in2=1 condition. So, the output will be low state.i.e.out1=0.so these conditions verified in the truth table.
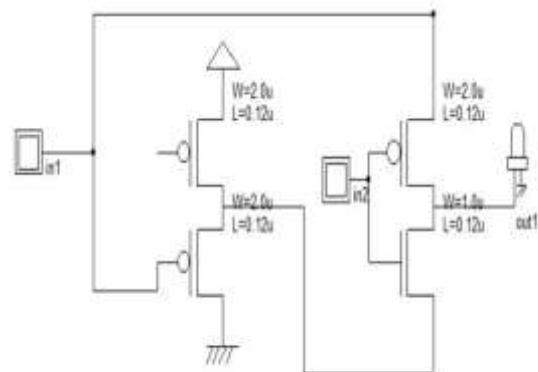

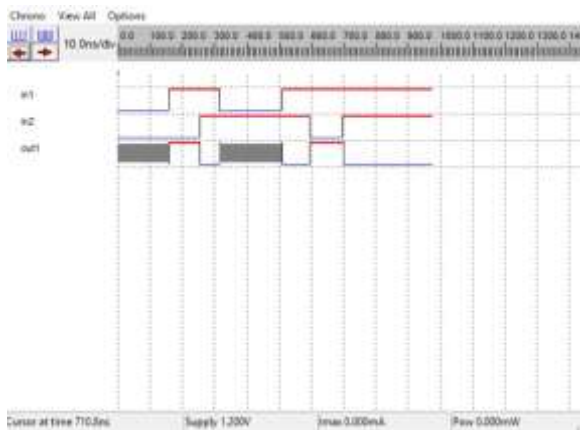Fig1: XOR circuit diagram with 4 transistors

Fig2: DSCH waveform of XOR circuit

The DSCH timing diagrams to represent the CMOS full swing circuits. It consists of PMOS and NMOS so the timing diagram represents the delay and power. The above timing diagram to be represented in the XOR gate truth table.

3. XNOR design:

XNOR gate is consists of 3 transistors so the many numbers of transistors to be Very delayed and power and area. So, the XNOR circuit is consists of two inputs and one output. So, the inputs are in1 and in2. And the output is out1.XNOR truth table is consists of two inputs that are the same the output will be the high state. So, the inputs are different the output will be the low state.

In this below figure XNOR gate circuit is the simulation of DSCH software. The simulation is continued with the XNOR gate. So, the inputs are in1=0 and in2=0 so the PMOS transistor is on and the NMOS transistor is off state in in1=0. Otherwise, the PMOS transistor is on and the NMOS transistor is off state in in2=0. So, the output will be high state i.e. out1=1. So, the inputs are in1=0 and in2=1.so the PMOS transistor is on and the NMOS transistor is off state in in1=0. Otherwise, the PMOS transistor is off and the NMOS transistor is on the state in in2=0. So, the output will be high state i.e. out1=1. So, the inputs are in1=1 and in2=0.so the PMOS transistor is off and the NMOS transistor is on the state in in1=1. Otherwise, the PMOS transistor is off and the NMOS transistor is on the state in in2=0. So, the output will be low state i.e. out1=0. So, the inputs are in1=1 and in2=1.so the PMOS transistor is off and the NMOS transistor is on the state in in1=1. Otherwise, the PMOS transistor is off and the NMOS transistor is on the state in in2=1. So, the output will be high state i.e. out1=1.so these conditions are verified in the truth table.

In the below fig4 the DSCH timing diagrams to represent the CMOS full swing circuits. It consists of PMOS and NMOS so the timing diagram represents the

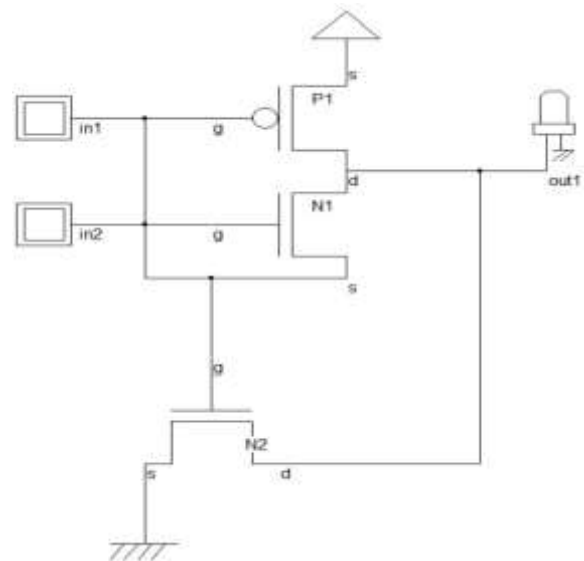delay and power. The above timing diagram to be represented in the XOR gate truth table.
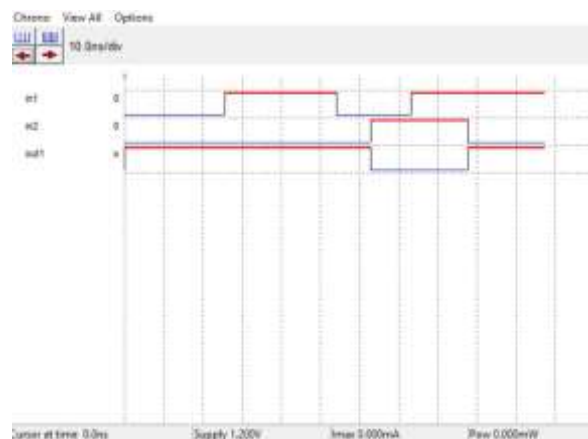

Fig3: XNOR circuit diagram

Fig4: DSCH timing diagram of XNOR circuit

4. Full adder design:

The full adder design is to be consists of XOR and XNOR gates so it is consists of new XOR and XNOR gates to be implemented in full adder circuit. The full adder circuit consists of three inputs and two outputs .so the inputs are in1,in2,in3, and the outputs are the sum and carry.i.e out1 and out2. Full adder circuits to be designed in DSCH software.

In the below figure full adder circuit is consists of 8 transistors. So it is a minimum number of transistors to b used. It is finding the area and delay and power consumption of circuits. So these conditions to be verified in the truth table. So the simulation occurs in the DSCH software. In full adder circuit is proposed with DSCH software. So the inputs are in1=0 and in2=0 and in3=0 the operation is included is p1 is on and n1 is off and n2 is on so the p2 is on and n2 off state. And the n3 is

on state and n4 is off state. So the p3 on state and n5 off state. So the out1 will be a low state. I.e. sum=0 and the out2 will be low state.i.e carry =0.otherwise these conditions to be verified in that of the truth table. So the inputs are in1=0 and in2=0 and in3=1 the operation is included is p1 is on and n1 is off and n2 is on so the p2 is on and n2 off state. And the n3 is on state and n4 is off state. So the p3 on state and n5 off state. So the out1 will be a high state. I.e. sum=1 and the out2 will be low state.i.e carry =0. So the inputs are in1=0 and in2=1and in3=0 the operation is included is p1 is on and n1 is off and n2 is on so the p2 is on and n2 off state. And the n3 is on state and n4 is off state. So the p3 on state and n5 off state. So the output

Will be the high state. I.e. sum=1 and the out2 will be the low state. I.e. carry=0
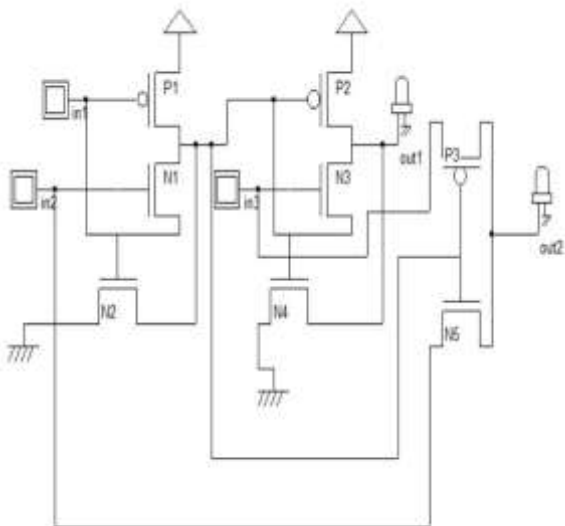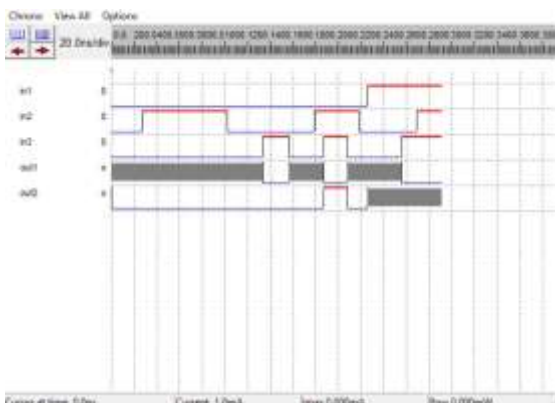

Fig5: Full adder circuit diagram

Fig6: DSCH waveform of full adder Circuit

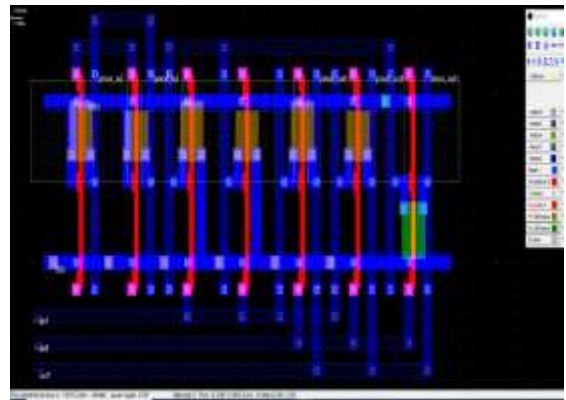## 5. SIMULATION ANALYSIS

5.1 simulation of XOR circuit:

Fig7: simulation of XOR layout

The layout simulation occurs in micro wind 3.1 on the voltage range is 0.6v to 1.2v in 32nm technology. The simulation results of the XOR gate layout is consist of diffusion and n diffusion and contact cuts and metals and NMOS and PMOS transistors are used. The layout consists of the XOR circuit is due to the time and delay and power consumption. The time is very less is compared to the XOR gate. So minimum number transistors due to increase and time are high .layout designing in 32nm technology in   6metals and 1NMOS and 3PMOSes are used. So the simulation occurred due to the MOS characteristics.
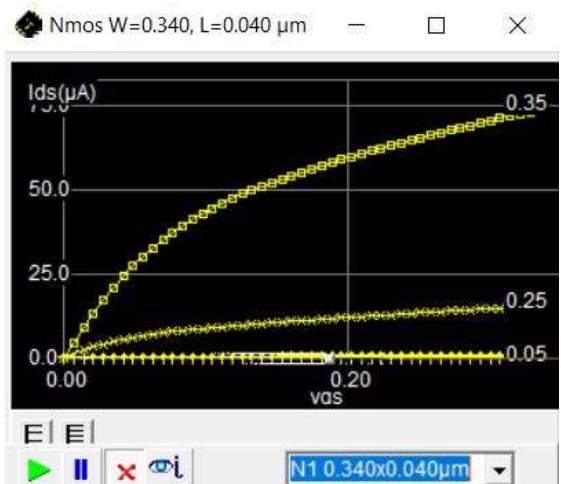

Fig8: characteristics of the layout

The characteristics of layout due to the current and voltage. So the voltage occurs due to 35% and the current is due to 75%. So the current is increased and the voltage is decreased. So the simulation of layout time is 5ns and the delay is 1.3ms. so the delay is low and compared to that of the XNOR gate.

The analog simulation id due to the Ids and VDS. So the power consumption is due to width to length.
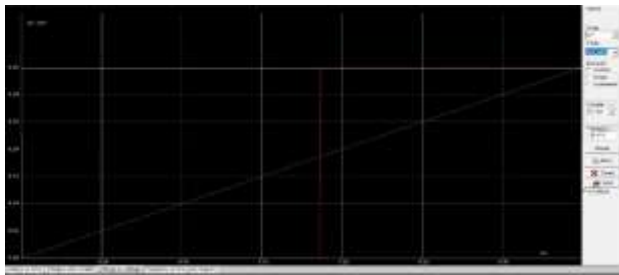
Fig9: analog simulation of XOR circuit

5.2 simulation of the XNOR circuit:

Fig10: layout simulation of XNOR circuit

The layout design of XNOR circuit I due to the micro wind 3.1 of the voltage range is 0.6v to 1.2v by using the 32nm technology. The layout simulation of the XNOR circuit is due to the p diffusion and p diffusion and metal and contact cuts. the simulation of the voltage range is due to 0.6v to 1.2v using 32nm CMOS delay is 823ns so the time is compared to that of high is XOR circuit. The layout simulation is due to voltages and currents and characteristics. So the 2NMOS and 1PMOS of being used for layout simulations.

Fig11: characteristics of the layout

The characteristics of the layout are due to current and voltages so the drain-source current ids and drain to source voltage VDS is t be considered. So the characteristics due to the current are the same constant and the voltage is varied to the difference. So the current

is due to 75% and the voltage is due to the 45%. So the simulation of time is 5ns it is compared to that of the XOR gate is the same. So the delay is due to the low.

Fig12: analog simulation of XNOR gate

So the analog simulation of the XNOR gate is due t the current and voltages so the simulation is occurring the current to voltage and voltage to current and voltage to voltage characteristics. so the is simulated in 45nm technology.
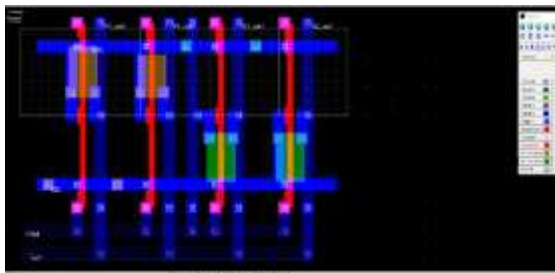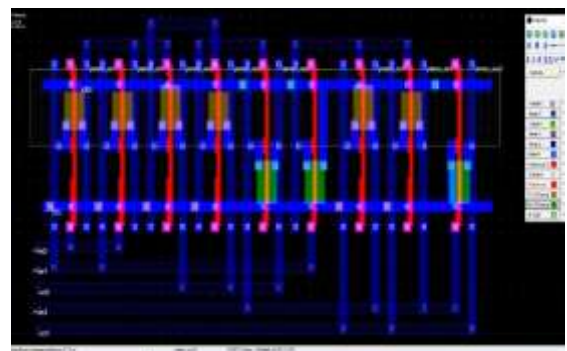
5.3 simulation of full adder circuit

Fig13: layout simulation of full adder diagram

The layout simulation of the full adder circuit is designed in XOR and XNOR circuits. So the layout is simulated by using the micro wind 3.1 in the voltage range is 0.6v to 1.2 v using the 32nm CMOS technology. So the consists of power and delay of the full adder layout are 20ns and delay is 505s so it is the minimum number of transistors to be increased to the low delay and time is high.
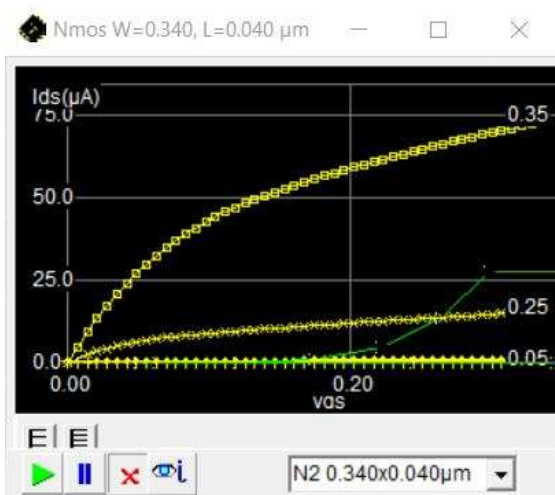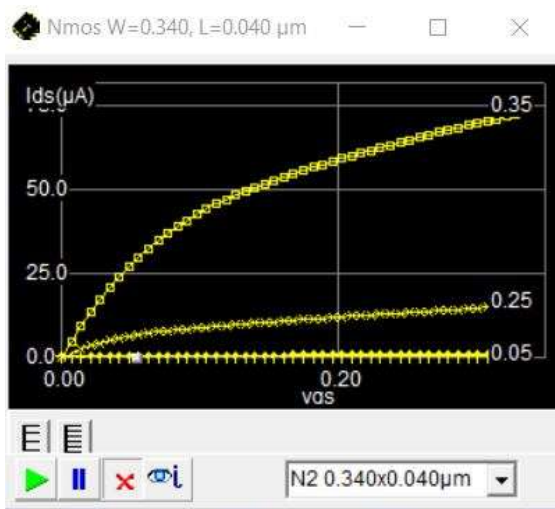
Fig14: characteristics of full adder circuit

The characteristics of full adder simulation are due to the drain to source current and drain to source voltage. So the vary the IDS and VDS. So the IDS are due to increase and VDS is decreased.
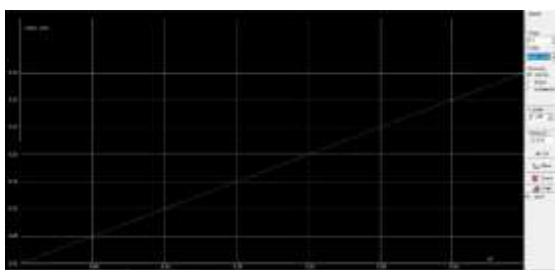
Fig15: analog simulation of the full adder circuit.

The analog simulation of full adder circuit id due to the current and the voltage. So it is compared to that of delay is less compared to that of high XNOR and XNOR circuits. So the time is very high compared to that of XOR and XNOR circuits. so the voltage is increases and current is due to decreases.
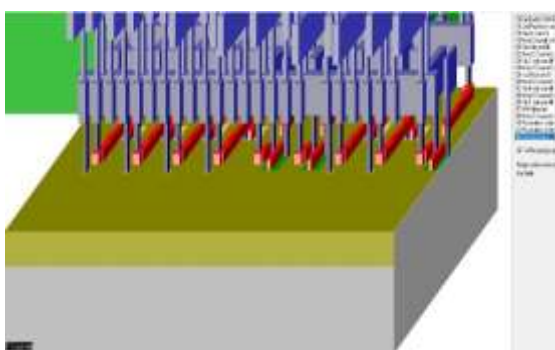
Fig16:3d view of full adder circuit

The 3d view of the full adder circuit is due to all process is completed.

RESULTS:

The comparison of the circuits is XOR and XNOR gates by exploring are due to the full adder circuit in microwind3.1 by using 32nm technology. So the time and delay and number of transistors to be included.

Table1: comparison between the XOR and XNOR and full adder circuits

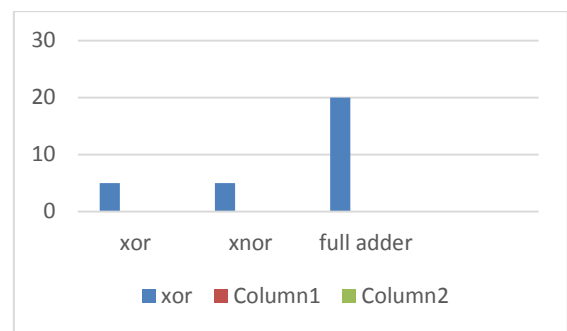| Parameter	XOR	XNOR	Full adder
Time	5ns	5ns	20ns
delay	1.3ms	8.2ms	5.0ms
no of transistors	4	3	8

TIME

Fig17: Time graph

The time graph to be represented in the XOR and XNOR gates due to the same time and these gates are explored by the full adder. So the time is very high in CMOS circuits. So the time graph to represent the time is increased and due to delay id increased. So the power is due to the high and compared to that of the full adder circuit.
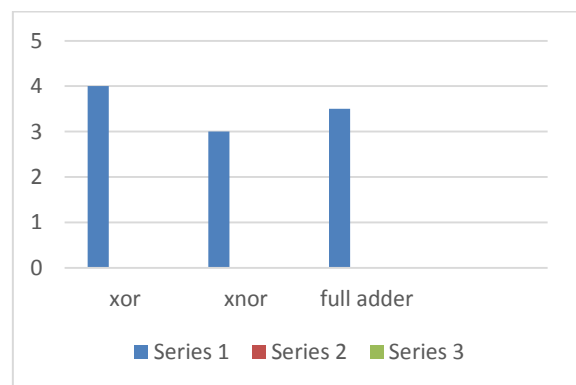
NO OF TRANSISTORS

Fig18: number of transistors graph

In the above graph to be represented In the XOR gate consists of 4 transistors and the XNOR gate consists of 3

transcistors and it is due to the XNOR and XOR proposed with the full adder circuit with 8 transistors.

CONCLUSION:

In this paper, we proposed a new design of XOR and XNOR gates explored by using a full adder circuit. The performance of this circuit is compared to that of power and time and delay. So the simulation results are based on the 32 nm technology n microwind3.1 the proposed design circuits are less time and high delay. The simulation results id based on good driving ability with a good output signal and better performance. The proposed circuit is suitable for the low delay of circuits and the minimum number of transistors.

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