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COMPARATIVE ANALYSIS OF TWO LEVEL, THREE LEVEL, FIVE LEVEL, AND SEVEN LEVEL H BRIDGE INVERTER

Utkarsh Chourasia[1], Pulkit Tiwari[2]

[1]M.Tech Scholar, VEC Lakhanpur Sarguja District
[2]Assistant Professor, VEC Lakhanpur, Sarguja District

Abstract: Two-level, Three- level, Five- level, and seven-level multilevel inverters are being simulated and analyzed in this paper. The schematic can be useful to photovoltaic applications. It is assumed that the output terminal voltage of a photovoltaic panel is a DC voltage. Load and the photovoltaic panel are connected via a multilevel inverter. The power quality of the power that reaches the load is being monitored. FFT analysis using MATLAB software is done. Total harmonic distortion (THD) of the output voltage waveform and output current waveform of all inverters are compared, the voltage and current load of each switch in each inverter is also shown. The simulation result shows that as the number of levels in the inverter is increased the voltage and current load on the switches are reduced; harmonic content of voltage as well as current waveforms are reduced and thus power quality is improved.

Index terms: Current Harmonics Reduction, Multi-Level Inverters, Voltage Harmonics Reduction, Voltage Load Reduction.

Introduction: The demand for electrical energy is increasing day by day due to which there is always energy shortages, due to this the integration of renewable energy sources to the electricity grid becomes a necessity and thus the integration of renewable energy with the grid is an interesting research topic in the present scenario. There is a rapid expansion of renewable energy resources and distributed generations due to which there occur problems associated with the grid integration the number of renewable energy sources and distributed generators is expanding rapidly which also brings some coercion to the power grid. To maintain or even to develop the power supply reliability and superiority of the power system with distributed generation, it is essential to have some new strategies for the operation and the management of the electricity grid. **SOLAR ENERGY** is one of the approving renewable energy resources, and the multilevel inverter has been proven to be one of the important capacity improving technologies in photovoltaic (PV) consumption. Multilevel voltage-source inverters present several advantages compared with their usual counterparts. By employing the output ac voltage, the terminal voltage from several levels of voltages, staircase waveforms can be produced, which approaches the sinusoidal waveform with little harmonic distortion, therefore reducing filter requirements. The requirement of several sources on the dc side of the converter makes multilevel technology eye-catching for PV applications [1]. though the multilevel inverter needs more components than traditional two-level inverters, lesser voltage-rated devices can be used, along with that the multilevel inverter offers various advantages such as the likelihood of lower switching frequency (which leads to higher efficiency) and lower electromagnetic interference (EMI).

"Various configurations and new inclination of photovoltaic power conditioning systems, employing a range of static converter topologies, can be found in technical literature [2], [3]". A cascaded multilevel inverter with a split dc source is proposed in this paper for supplying the load employing the solar PV panel. It is assumed that through a proper maximum power point tracking algorithm the output of the Photo Voltaic array is a constant DC source and simulations are carried out for two-level, three-level, five-level, and seven-level multilevel inverter, and the results obtained are compared mutually. The multilevel inverters need a large number of semiconductor switches and hence its cost gets increased, the use of multilevel inverters can be justified by viewing the voltage and current load on each switch and hence it is showed that despite the increased number of switches there may not be much cost dissimilarity, the burden on switches gets reduced, lesser rating semiconductor devices can be used to implement the module. What's more, the control strategy is very a lot simpler, so there will not be much cost difference. Moreover, it is shown that the total harmonic distortion of voltage and current gets reduced on increasing the number of levels in a multilevel inverter.

Two-level inverter

Figure 1 indicates a single phase H bridge inverter having 4 switches. Usually, an IGBT is used as a switch in an inverter. It is observed that an R-L load is connected between the two-leg of the inverter. Two-level inverters utilize the two voltage levels at the output of the inverter

they are the +V volt and –V volt. For output voltage to be +V volt switch S1 and S2 are closed together and S3 and S4 are kept open. To obtain –V volt at the output S3 and S4 are closed together and S1 and S2 are kept open. The switch table of a Two-level inverter is shown in table 1. The output voltage waveform of a two-level inverter is shown in figure 2

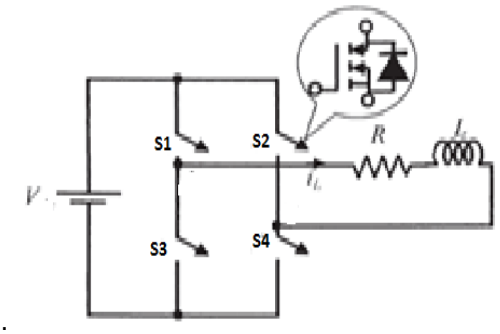

Fig 1 circuit of a two-level and three-level inverter

Voltage level	S1	S2	S3	S4
+V	1	0	0	1
-V	0	1	1	0

Table 1 A two-level inverter switching pattern

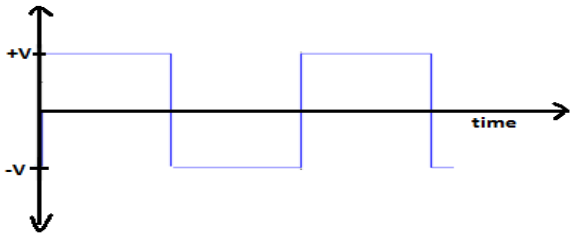

Fig 2 voltage waveform of a two-level inverter

Three-level inverter

By changing the switching signals to some extent of the H Bridge inverter shown in figure 1, a Three-level inverter can be obtained. A three-level inverter consists of three-level of voltage at the output side exclusively 0-volt level, +V volt level, and –V volt level. The switching table of a three-level inverter is shown in table 2. The output waveform of a three-level inverter is shown in figure 3.

Table 2 switching pattern of a three-level inverter

Voltage level	S1	S2	S3	S4
0	0	0	1	1
+V	1	0	1	0
-V	0	1	1	0

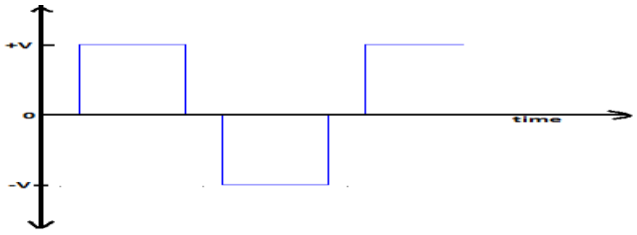

Fig 3 voltage output of a three-level H bridge inverter

Five level inverter

Figure 4 represents the circuit diagram of a five-level inverter. Its requirements are Two H Bridge inverter is connected in cascade having a sum of eight switches. The output voltage levels are 0 volt, +V/2 volt, -V/2 volt, +V volt, and –V volts. The switching signals to obtain 0, +V/2, -V/2, +V, and –V is given in table 3. The output voltage waveform of a five-level inverter is as shown in figure 5.

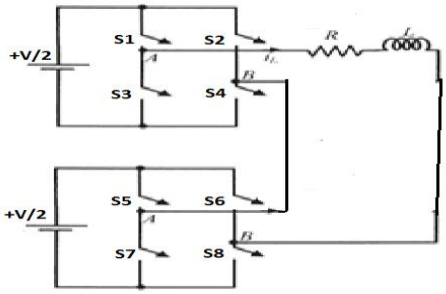

Fig 4 schematic circuit of a five-level inverter

Voltage	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	1	1	0	0	1	1
+V/2	1	0	0	1	0	0	1	1
-V/2	0	1	1	0	0	0	1	1
+V	1	0	0	1	1	0	0	1
-V	0	1	1	0	0	1	1	0

Table 3 switching sequence of a five-level cascaded H bridge inverter

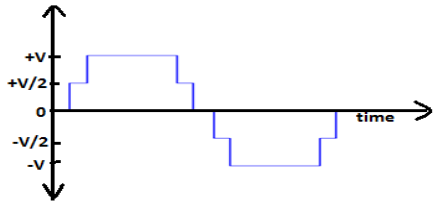

Fig 5 output voltage waveform of a five-level inverter

Seven Level Inverter

Figure 6 represents the circuit diagram of a seven-level inverter. It needs three dc voltage sources and 12 switches. The voltage level of a seven-level inverter is 0, V/3, 2V/3, V,-V/3,-2V/3, and –V volts. On appropriate switching, these voltage levels at the different instant of time output voltage that resembles nearly sinusoidal signals can be obtained. The switching cycle to obtain the needed voltage levels is shown in table 4. The output waveform of the seven-level inverter is shown in figure 7.

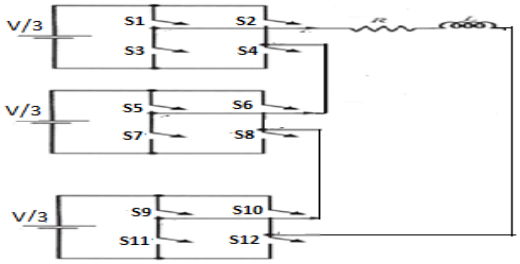

Fig 6 schematic circuit of a seven-level inverter

Volt	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	0	1	1	0	0	1	1	0	0	1	1
+V/3	1	0	0	1	0	0	1	1	0	0	1	1
-V/3	0	1	1	0	0	0	1	1	0	0	1	1
+2V/3	1	0	0	1	1	0	0	1	0	0	1	1
-2V/3	0	1	0	0	0	1	1	0	0	0	1	1
+V	1	0	0	1	1	0	0	1	1	0	0	1
-V	0	1	1	0	0	1	1	0	0	1	1	0

Table 4 switching pattern of a seven-level inverter

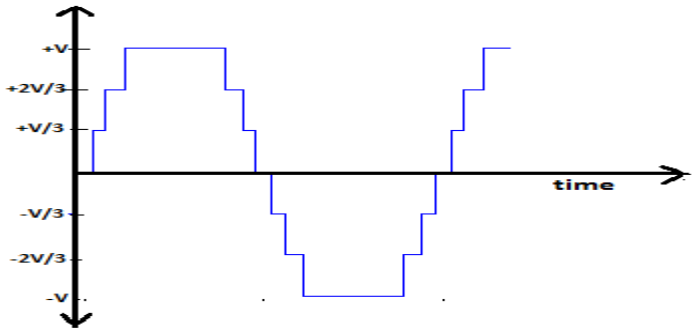

Fig 7 output voltage waveform of a seven-level inverter

Control structure

Fibonacci series based open-loop control is used in this research. Fibonacci series is used to determine a constant value, the reference sinusoidal signal is compared with that constant value and then accordingly the switching signal is generated. Switching signals are shown in the switching tables, while observing the switching table it is clear that the lower limb has a gate signal which is the complemented value of the upper limb gate signal.

Taking a case, if the gate signal of switch S3 which is the lower branch of S1 complemented by the gate signal of S1. Now to obtain the preferred signal a sinusoidal signal whose frequency equals 50 Hz is compared to a constant value signal and a gate signal is being generated.

If we assume that the sine wave signal which is being compared with a constant value signal obtained by Fibonacci series be named by F.

If we take the case of a two-pulse inverter there is only one fixed value signal whose magnitude is 0. If the value of F is greater than 0 then switch S1 will be turned ON.

If the value of F is lesser than 0 then switch S2 will be turned ON. The gate signal which is specified to S3 and S4 is a complemented value of the gate signals specified to S1 and S2 respectively.

If we take the case of a three-level inverter, the only difference present is that S1 is turned ON when the value of F is greater than 2, and S2 is turned on when the value of F is lesser than -2.

In the case of a five-level inverter, four more switches have been used the switching provided to S1 and S2 are similar when compared to that of a three-level inverter. Switch S5 is turned ON when the value of F is greater than 5 and the switch S6 is turned on when the value of F is less than -5.

Switch S7 and S8 are the complemented signals of S5 and S6 respectively.

For a seven-level inverter S9 is turned ON when F is greater than 9 and S10 is turned ON when F is less than -9. Switches S11 and S12 get the gate signal from the complemented values of gate signals of S9 and S10 respectively.

Thus with the addition of each bridge, the sinusoidal signal F is compared with the fixed value which is a Fibonacci series starting with 2. Such as 2,5,9,14,……. The magnitude of the sinusoidal signal has to be controlled in such a manner that it ought to be the next number in the Fibonacci series following the largest constant value of the fixed signal applied for controlling. For example, the amplitude of F for 2,3,5 and 7 levels should be 2,5,9, 14 respectively.

Simulation diagram and result

The simulation model of an inverter that is having different voltage levels are modeled is a Mat Lab Simulink using a sim power system toolbox.

The schematic simulation diagram of a two-level inverter with various control inputs is shown in figure 8. The magnitude of the dc voltage used in the model is $230\sqrt{2}$ which is the crest value of a desired sinusoidal signal having an RMS value of 230 Volt.

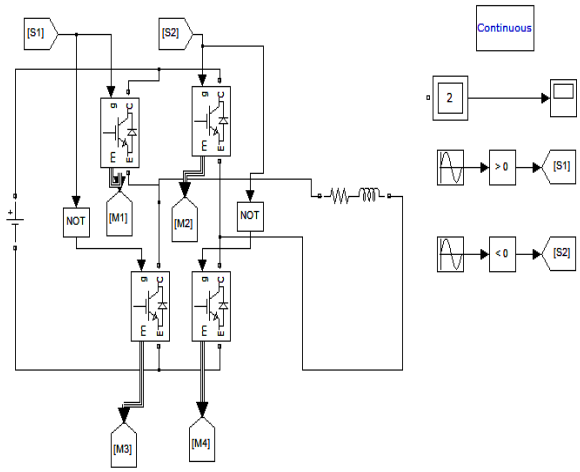

Fig 8 schematic simulation circuit of a two-level inverter

Load resistance of 2Ω and inductance of 2 mH is connected at the output end of the inverter. The output voltage waveform and the output current waveform is analyzed and it is shown in Figure 9.

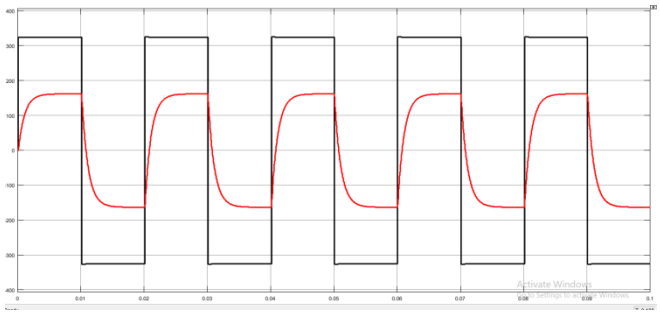

Fig 9 Output voltage waveform and output current waveform of a two-level inverter.

The simulation circuit of a three-level inverter with its control inputs is shown in figure 10. The output voltage waveform and output current waveforms are analyzed and are shown in figure 11.

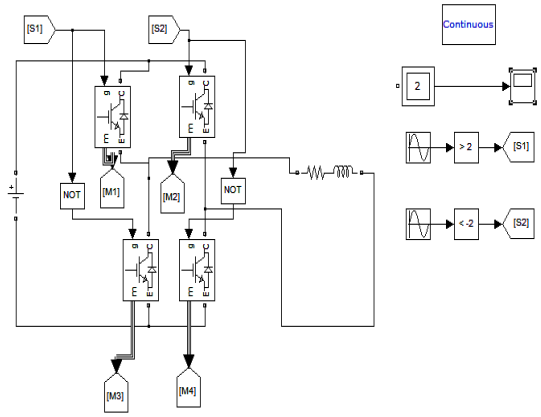

Fig 10 schematic Simulation circuit of a three-level inverter

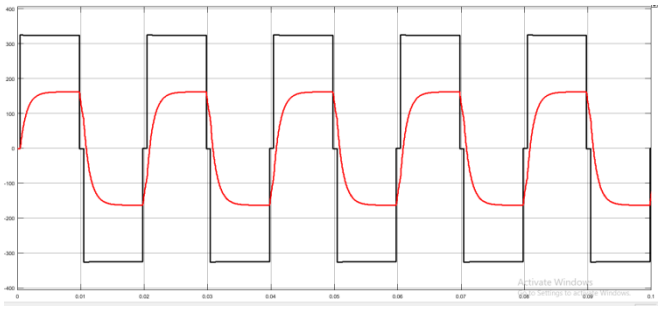

Fig 11 Output voltage waveform and output current waveform of a three-level inverter.

The schematic simulation diagram of a five-level inverter along with its control inputs is shown in figure 12. The output voltage waveform and output current waveform are analyzed and shown in figure 13. Here two h bridge

inverter are used so the voltage source is divided into two cells. So the voltage source value is $\frac{230\sqrt{2}}{2}$.

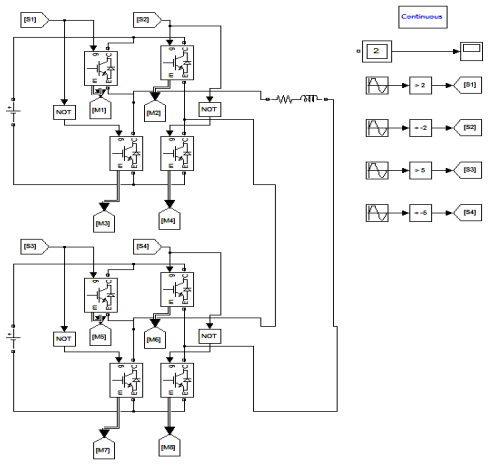

Fig 12 schematic Simulation circuit of a five-level inverter

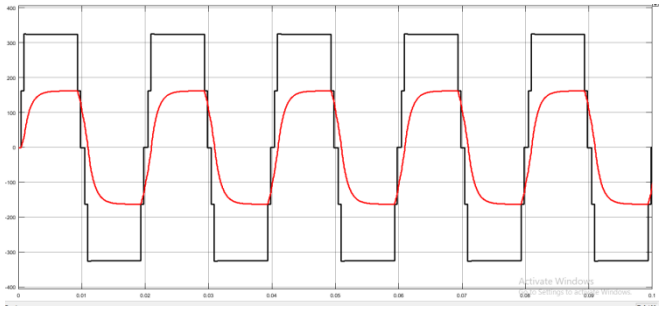

Fig 13 Output voltage waveform and current waveform of a five-level inverter.

The schematic simulation circuit diagram of a five-level inverter along with its control inputs are shown in figure 14. The output voltage waveform and output current waveform are analyzed and are indicated in figure 15. Here three H-bridge are connected in cascade so the overall supply is divided into three cells and thus voltage source used is $\frac{230\sqrt{2}}{3}$.

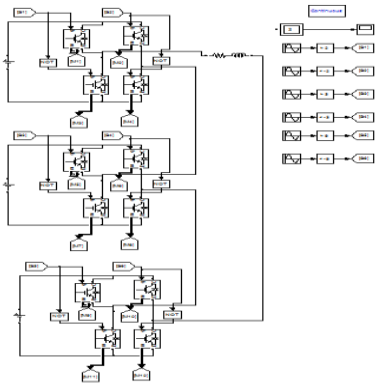

Fig 14 schematic Simulation circuit of a seven-level inverter

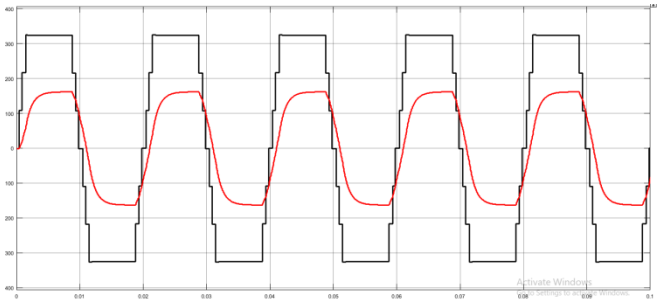

Fig 15 Output voltage waveform and current waveform of a seven-level inverter.

Analysis of the waveforms from all the levels of the inverter is done. The voltage load, current load of the switches used, voltage THD, and current THD that are present in the output voltage waveform, and output current waveform are tabulated in table 5.

Characteristics	Two-level inverter	Three-level inverter	Five level inverter	Seven level inverter
Voltage THD	48.38%	40.71 %	32.95%	25.09%
Current THD	29.07%	26.88%	23.19%	18.10%
Voltage burden on switch	325.3 V	325.3 V	162.6	108.4
the current burden on the switch	153 A	153 A	153 A	153 A

Table 5 Comparative Analysis of all the Levels of Multilevel Inverter

Conclusion: by comparing the different parameters associated with the multilevel inverters it is concluded that with increasing the number of levels in the multilevel inverters the output voltage waveforms can be made nearly sinusoidal waveforms by which ac distribution of the power from the photovoltaic module can become simple and attainable. An increase in the number of levels

drastically reduces the harmonic content in the voltage and current waveforms. The voltage burden on each switch also goes on reducing with the increase in the number of levels in a multilevel inverter.

References

[1] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid-connected photovoltaic systems—An overview," in Proc. ISIE, 1998, vol. 1, pp. 224–229.

[2] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. PortilloGuisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," IEEE Trans. Ind. Electron., vol. 53, no. 4, pp. 1002– 1016, Aug. 2006.

[3] L. Quan and P. Wolfs, "Recent development in the topologies for photovoltaic module integrated converters," in Proc. IEEE Power Electron. Spec. Conf., Jun. 18–22, 2006, pp. 1–8.

[4] J. Rodríguez, J. S. Lai, F. Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Application" IEEE Transaction on Industrial Electronics, vol. 49, no. 4, pp. 724-738, August 2002.

[5] L. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel converters for large electric drives" IEEE Trans. Ind. Application., vol. 35, pp. 36-44, Jan./Feb. 1999

[6] R. L. Naik, U. Kumar, "A Novel Technique for Control of Cascaded Multilevel Inverter for Photovoltaic Power Supplies ", European Power Electronics and Application Conference (EPE), 2005.

[7] Lennart Ängquist, Antonios Antonopoulos, Daniel Siemaszko, Kalle Ilves, Michail Vasiladiotis, Hans-Peter Nee, "Open-loop Control of Modular Multilevel Converters using Estimation of Stored Energy," accepted for publication at IEEE Transactions on Industry Applications.

[8] Tang Xisheng "Study on SCES systems used in distributed generation system", Master thesis, Chinese Academy of Sciences, 2006.

[9] J. S. Lai, F. Z. Peng, "Multilevel Converters- A New Breed of Power Converters" IEEE Transaction on Industrial Applications, vol. 32, no. 3, pp. 691-697, May/June 1996.

[10] L. M. Tolbert, F. Z. Peng, "Multilevel Converters as a Utility Interface for Renewable Energy Systems" IEEE Power Engineering Society Summer Meeting, 2000.