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FPGA based Inter-IC Design and Interface it with Ultrasonic Sensor for Machine Learning Application

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Abstract: In this paper, a novel master-slave Inter-IC bus regulator is developed, and then this slave plan is controlled by master gadgets. Thus, a master Inter-IC bus regulator has been implemented. The plan is the first simulation and synthesis utilizing Xilinx Vivado 2020.1 HLx Editions suite. Lastly, manufacture design, attain on FPGA, then concatenating between the FPGA (Basys 2 Spartan 3E) and this ultrasonic Sensor has been accomplished by using master Inter-IC bus regulator.Ultrasonic Sensor, which is acting as a slave gadget for the masters. Ultrasonic Sensor uses to compute the separation of the objects, which can be utilized for many applications like self-driving vehicles. This paper introduces the latest sensing applications using smart sensor systems supported by ML. First, well-known ML algorithms execute in smart sensor organizations for sensible sensing submission. They are converse with the modern age of information where high-tech vehicles like self-driving cars have become the vehicle for our use. Believing a microchip to regulate a car's speed and precision is certainly something guaranteeing travelers' assurance. The cutting-edge vehicle's request against crash framework utilizes sensors around the vehicle to detect nearness to environmental surroundings. The framework auto-draws the brakes to slow down. This sort of innovation makes driving to such an extent more comfortable and safe. Sequential statement procedure is generally used in electronics in according to transfer data.

Keywords: Inter-IC, Master, Slave, Concatenating Sensor, Machine Learning, Xilinx Vivado HLx Editions suite.

I. INTRODUCTION

The advancement of the new car requires new sensors that can calculate distances in small ranges. Recently, many accidents around the country are increasing because of the absence of an appropriate plan and safety infrastructure. Therefore, for proposed parking and common safety application, the electronics command circuit (ECU) required precise information of a coming object. They Measured the length between any item possible with the assistance of an Ultrasonic Sensor. Ultrasonic - sensors are entirely adaptable in distance measurement. Sensors are the critical components in automotive electronic control circuits, which must have a high-grade accuracy, precision, robustness, and low cost. The ultrasonic arrangement is utilized to compute the distance is probably the most inferior expensive choice. An analysis was finished by numerous authors about the usage of ultrasonic sensors, as explained here. Ultrasonic transmitting waves are sounds with a frequency which is higher than that of 20 kHz. This frequency cannot hear by humans. This hypothesis depends on the concept of calculating the pulse reflection time from the object. The ultrasonic transducer sends a wave signal and receives a reflection signal called echoes, as describe in Fig.1. When the transmitted wave pulse detects any object, the reflected wave called echo wave, is bounce return to the transducer.

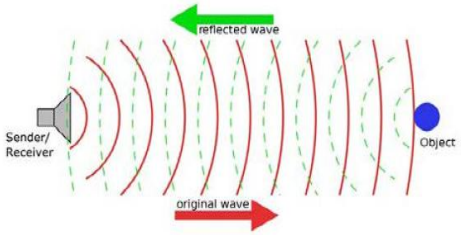

Fig. 1 Ultrasonic Sensing Principle

This ultrasonic Sensor, which is a transducer, works on the same principle as like radar system. An ultrasonic sensor will convert electrical energy generated to an acoustic wave conversely. The acoustic signaling waves are ultrasonic waves traveling with a frequency of more than 18kHz. The HC-SR04 is an ultrasonic sensor that generates ultrasonic waves at a frequency 40kHz.

Inter-IC Theory -Now a days, Inter-IC usage is simpler as a contrast with other sequential statement pedestal procedure as it utilization just only two wires for concatenating gadgets. Accessibility of several master potential, potential to support significant integer of devices, the capability to attach by the usage of only demanding Start - Stop situation, and read-write tasks are various skin texture innate to Inter-IC protocol.

Start Condition It is used to start the address outline. The master gadget leaves an SCL to high with pulls to an SDA to low.

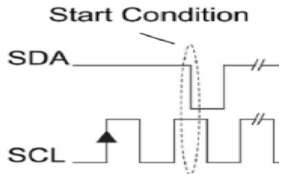

Fig. 2 Start the address outline.

• This notifies that all slave gadgets give an indication that transmission is going to begin.

• When two master gadgets want to take holding to any of the bus at same time, whichever gadget pulls SDA to low first dominates the bus and deals with the bus.

Address Frame

The address data outline is always the primary goal in any new communication arrangement. For the 7-bit address, the address of the slave clocked to the most significant bit (MSB) first, trailed by an R/W bit showing if is a read (1) or write (0) activity.

Data Frames

After an address outline has been sent, information can start being communicated. The master will just keep producing clock pulses at a standard interval, and the information will be set on SDA by anyone master or slave, depending upon whether an R/W bit showing a reading or writing activity.

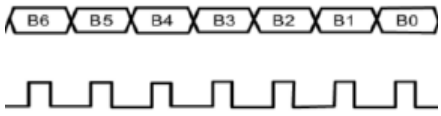

Fig. 3 Data frame communicated bit by bit

Stop condition

When all the information frames have been transmitted, the master will produce a stop condition. Stop conditions are characterized by an 0 to 1 (low to high) transition on SDA after a 0 to 1 change on SCL, with SCL staying high.

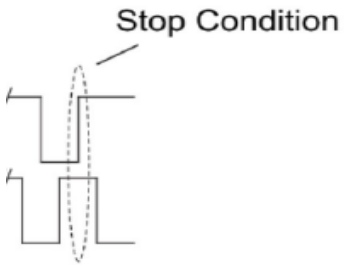

Fig. 4 stops the address outline

During normal information writing activity, the data on SDA bus should not alter when SCL bus is at high, to avoid any wrong stop conditions.

Inter-IC Protocol

It is at last followed by an single bit representation whether is it wants to PISO write [0] - SIPO read [1] from any slave device. Master uses SCL clock cycle and slave uses SCL_16 clock to detect data

RTL synthesis of SCL generator - It generate two signals

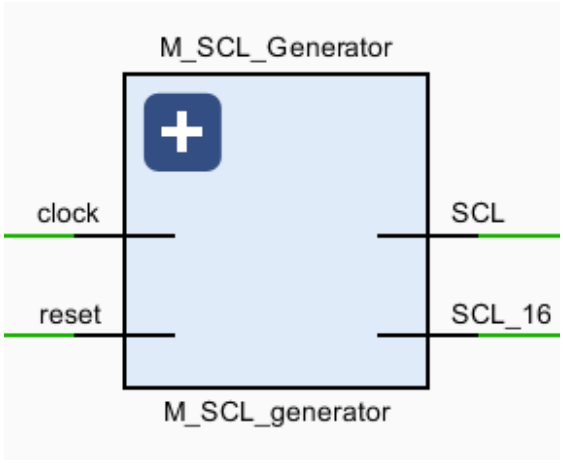

Fig.5 SCL_16 generator

SCL_16 clock should be faster than master.

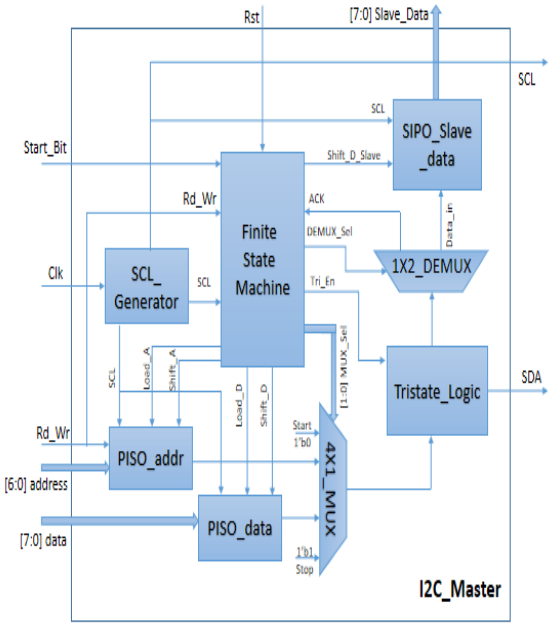

Fig. 6 PISO_data shift activity block architecture

1. Master FSM - It consists of the following states

IDLE_STATE- It is used to start the address outline; the master gadget leaves an SCL to high with pulls to an SDA to low.

ADDRESS_DETECTOR - For the 7-bit address, the address of slave clocked to the most significant bit (MSB).

RD/WR_STATE - R/W bit showing if is a read (1) or write (0) activity.

SEND_DATA - Shift of data activity performed.

STOP_STATE - Stop conditions are characterized by an 0 to 1 (low to high) transition on SDA after a 0 to 1 change on SCL, with SCL staying high

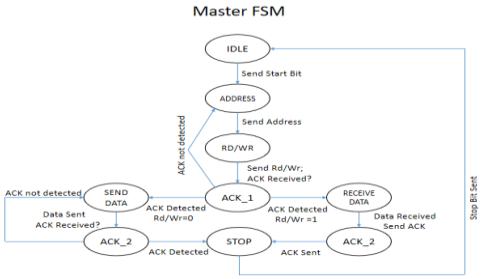

Fig. 7 FSM state diagram master architecture

APPLICATION

VR technology, a physical experience through virtual space with an AR/VR(like in manufacturing) for calculating the separation to an object and ultrasonic Sensor are attracting impressive attention.

The automatic landing of drones.

II. PROPOSED WORK

First most importantly master-slave Inter-IC bus regulator is developed and then, this design control by master gadgets. Thus, the master Inter-IC bus technique has been implemented. The plan is first simulation is performed and then synthesize performed by xilinx vivado 2020.1 HLx Editions suite. Finally, the synthesized plan, obtained on FPGA, then concatenates with an ultrasonic Sensor to compute the objects' separation, which can be utilized for many applications instead of DC motor.

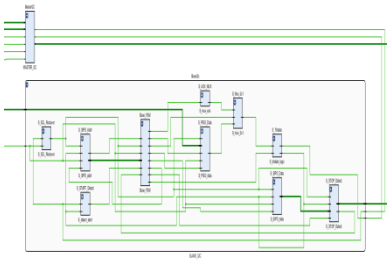

Fig 8 single master - slave Inter-IC bus regulator

Interface with Ultrasonic Sensor for Machine Learning Application

Whenever echo detected by Ultrasonic sensor then the measurement of any object is calculated with the assistance of RTL design given in fig 9. This distance data can be fetch with the assistance of Inter-IC bus regulator. The address data outline is always first priority to any new communication arrangement. Ultrasonic Sensor is behaves as a slave for master has unique address to transfer data this master is at first in master send mode by transmitting an START bit followed by a 7-piece address to the slave it wants to convey known as start bit detector. For the 7-bit address, the address of slave clocked to the most huge significant bit (MSB) first, trailed by a R/W(1) bit showing in the event that is a read (1) activity performed.

After the address frame has been sent, information can start being communicated. The master will just keep producing clock pulses at a standard interval, and the information will be set on SDA by either master or slave, once all the information frames have been transmitted, the master will produce a stop condition. Stop conditions are characterized by an 0 to 1 (low to high) transition on SDA after a 0 to 1 change on SCL, with SCL staying high. During normal information writing activity, the data on SDA bus should not alter when SCL bus is at high, to avoid any wrong stop conditions. If the master wishes to take a reading from the slave, then it continuously receives the data byte from the slave, then the master is transmitting with ACK bit afterward each byte except the last one. (In this state, the master will be in the master receiving state, and the slave will be in slave transmitting mode). When this sensor data is obtained from Inter-IC, this analysis of data can be processed to the machine learning algorithm.

Whenever the Ultrasonic sensor detects echo, the measurement of the distance to any object is calculated with the assistance of the RTL design given in Figure 8.

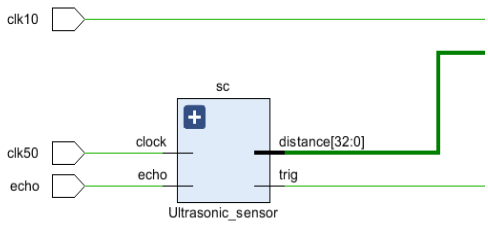

Fig 9 RTL Schematic to an Ultrasonic_sensor

III. RESULTS

Synthesis Results

The design of inter-IC bus regulator code schematic fig description which is generated with the assistance of verilog language which is used on software vivado HLx edition.

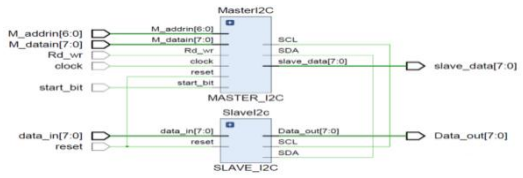

Fig. 10 RTL synthesis result for single master slave Inter-IC bus regulator

IV. SIMULATION RESULTS

Simulation reports for single master slave Inter-IC bus regulator obtained from xilinx vivado 2020.1 HLx Editions having a 500Hz clock R/W(1) bit meaning is that READ signal to 1 if is a read (1) activity performed in Fig.11. At last, it is followed by a single bit representation of whether it wants to PISO write [0] - SIPO read [1] from any slave device. If the master wishes to take a reading from the slave, then it continuously receives the data byte from slave, then the master is transmitting with ACK bit afterward each byte with the exception of the last one.

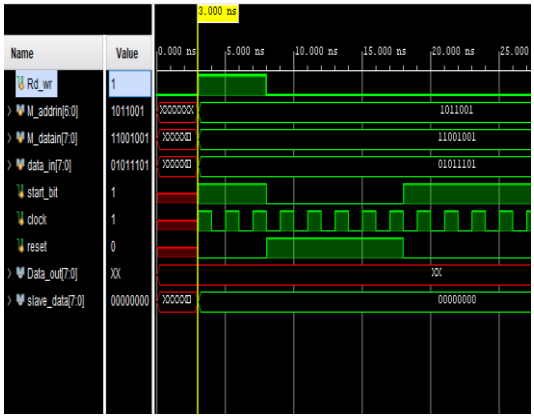

Fig. 11 READ activity performed by master.

Ultrasonic Sensor behaves as a slave for master has a unique address to transfer data this master is at first in master send mode by transmitting a START bit followed by a 7-piece address to the slave it wants to convey known as start bit detector.

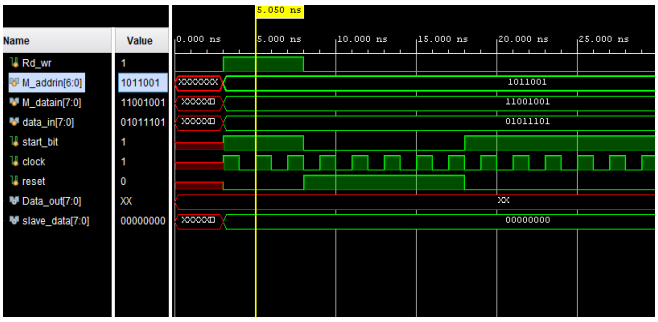

Fig. 12 Describes 7-piece address of slave.

If the master wishes to take a reading from the slave, it continuously receives the slave's data byte from the slave, SIPO read [1] from Ultrasonic sensor device. Master uses SCL clock cycle, and slave uses SCL_16 clock to detect data, SCL_16 clock should be faster than master.

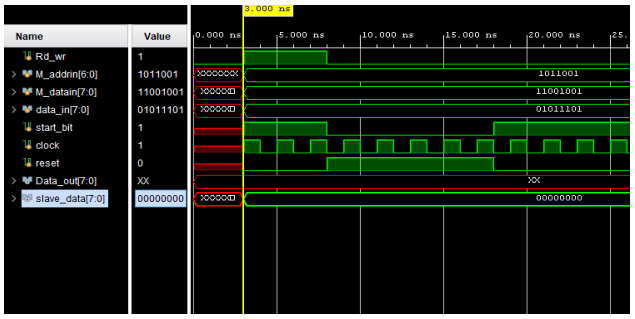

Fig.13 Slave 8-piece data transfer to the master

Whenever the Ultrasonic sensor detects echo, the measurement of the distance to any object is calculated with RTL design assistance given in Figure 9. This distance data can be fetched with the assistance of the Inter-IC bus regulator.

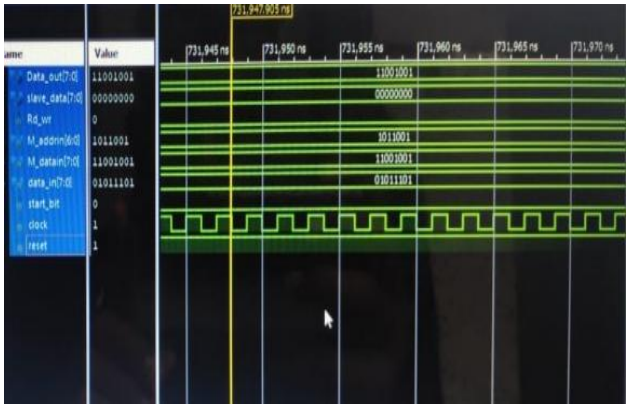

Fig. 14 Slave 8-piece data transfer to master

Table 1 Inter-IC utilization summary

S No.	Site Type	Utilized	Available	Util%
1	Slice LUTs	62	41000	0.15
2	Slice Registers	104	82000	0.13
3	Logical nets	204		

VI. CONCLUSION

This paper begins with the Inter-IC bus regulator's introduction and gives a brief note on communication between master to slave. Out of all protocol standards, Inter-IC is very efficient and simpler to implement. The main objective of this work is to connect the sensor components of the Inter-IC and the ultrasonic and obtain the sensor information. The sensor is modest and flexible, has a wide cover, can measure speed directly, and is not affected by light. Or the weather. For the rapidly growing demand for high-quality data analysis, the ML algorithm has become an integral part of the modern measurement system,

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REFERENCES

1. Deepika, Neetika Yadav, “Design of Dual Master I2C Bus Controller and Interfacing it with DC Motor ”, 2018.
2. Cang Liu,Xianqiang Bao,Chengcheng Xu,Qingyun Meng,Tao Liao, “A Flexible Hardware Architecture for Slave Device of I2C Bus”.
3. Suryono Suryono, Ainie Khuriati, “Wireless Sensor System for Photovoltaic Panel Efficiency Monitoring Using Wi-Fi Network”.
4. Anagha A, M. Mathurakani, “Prototyping of Dual Master I2C Bus Controller”.
5. Bharath.K.B, K. V. Kumaraswamy and Roopa K Swamy, “Design of Arbitrated I2C Protocol with DO-254 compliance”.
6. Hardik Kaneriya, Santosh Jagtap, “Design of I2C Master with Multiple Slave”.
7. Anagha A, M. Mathurakani, “Design of Single Master Inter-Integrated Circuit Bus Controller”.
8. NXP Semiconductors, “I2C Bus Specifications”, April 2014.
9. Prasanna Bagdalkar, Layak Ali, “Interfacing of light sensor with FPGA using I2C bus”.