International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 07 Issue: 12 | Dec 2020 www.irjet.net p-ISSN: 2395-0072

HARMONIC MITIGATION SOLUTION OF THREE PHASE INVERTER

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Abstract - *This research paper consist theory and simulation of Mitigation of Harmonic from the output of the three phase inverter. Paper deals with the concept of new model of feedback inverter with sin wave pulse width modulation at gate input and focused on output parameter like Total Harmonic Distortion percent of voltage, Total Harmonic Distortion percent of current and Fundamental value of the voltage and fundamental value of current. Using the concept of Clark and Park transformation the three phase feedback loop is build. All result is formed by maintaining the IEEE standard.*

Key Words: Mitigation of harmonic, feedback inverter, Clark, Park.

1. INTRODUCTION

Research deals with the concept of harmonic reduction using feedback network. One can remove the harmonic from the circuit basically in two ways, first way is by increasing the stage of inverter and second way is by building filter at output side. Only focusing on Stage increment and output side maintenance the nature of circuit became bulky and complex. By using different gate pulse variation techniques one can also achieve pure sine graph at output as per dependent on load. So by increasing number of stage of inverter, the circuit became complex and gate pulse formation logic will be also complicated. By designing and implementing huge size filter one can achieve better output but there will be huge power loss and drastic reduction in fundamental voltage. So to solve the problem of both the situation the feedback network is design which is the major part of this research study. So the research paper deals with the study and implementation of Inverter design using feedback network logic with the help of some transformation techniques.

1.1 Simulation of single phase SPWM inverter:

The design of different stage of this type of inverter with the help of sin wave pulse width modulation is discussed in this section. This technique is used to produce various duty cycles for a single period presented by maintaining the pulse with constant amplitude. The output voltage will produce with different magnitude whenever there will be the variation in the pulse width of gate pulse which give rise to the control over the output voltage and reduction in harmonic content. This method is one of the most common industrial method used for the motor controlling mechanism and the application based on an inverter. To produce the signal of desired frequency the carrier wave is compared with the sin wave where carrier wave is in the form of triangle wave [1]. The minimum voltage level required for voltage source inverter is two levels that are from zero to positive amplitude and zero to negative amplitude. This inverter with two levels is controlled with respect to various patterns of gate signals like square wave, quasi-square wave and PWM (pulse width modulation). Various gating pattern results to the formation of different level of harmonic pattern at the output of an inverter. By making control over pulse width of gating pulse the conduction time of power switches can be maintained which gives rise to the formation of the different voltage level [3].

1.2 Concept of single phase 5 level (multilevel) inverter:

Symmetrical five levels Cascade H-bridge multilevel inverter is introduced by using the concept of multiple carrier pulse width modulation techniques. This type of an inverter includes an array of power semiconductor (Switches). Desired output voltages are produced by the multiple levels of DC voltages as inputs. The sin wave can be formed by arranging multiple DC voltage with minimum step size. Reduction in harmonic is seen as compared to other lower multilevel devices. This inverter provides good output quality and minimum power loss as compared to other conventional inverter with the same Specification [2][7].

1.3 Concept of single phase 7 level (multilevel) inverter:

The part of Multilevel inverter that is seven layer inverter are used mainly used for a high voltage application and the result obtained by this inverter is much better than normal two level inverter due to minimum harmonic distortion, minimum electromagnetic interference, and high D.C. link voltages. It helps to generate the approximated sinusoidal waveform and Fundamental switching frequency [4][7]. The major problem of this of inverter is balancing of voltages and on the path of non-linear load it gives rise to the formation of spike in voltage level when the number of component increases.

1.4 Analysis of three phase inverter:

Three phase inverter it most commonly used in industry for the three phase AC device. Analysis of output is done on the basis of conduction at different triggering pulse of gate for different switch. There are various conduction mode like 180°, 120° and 150°. As compared to single phase it has less THD% at output of inverter [5]. If there is a requirement of AC the waveform should be shaped in pure sine wave format or approximated to the sin waveform. In order to achieve that we need to reduce the harmonic content, which possible using different types of PWM inverter [9]. Using Sin wave pulse width modulation [8][9] and a Space vector pulse width modulation [8][9] we can get the good fundamental as compare to basic conduction mode operation [6].

2. FLOW MODEL AND EXPERIMENT

The basic structure of the project is shown and explains with respect to the block diagram. Basically it consists of eight blocks out of which three blocks are used to perform closed loop control and other blocks are the main blocks of system where the main operation are used to perform. From supply block DC supply is used to forward towards positive and negative terminal of an inverter which is operated by the Sinusoidal Pulse width modulation technique. The Inverse Park transformation provide feedback signal to PWM generator. The current and voltages are supposed to be sensed by stage1 and stage 2 block. Filter block is used to smoothen and minimize the THVD percentage and THID percentage from the voltage and current waveform. The whole system is suitable for any type of output load i.e. linear load and non-linear load. Feedback mechanism tracks the record of distortion in current and voltage and tried to minimize it Pulse Width Modulation.

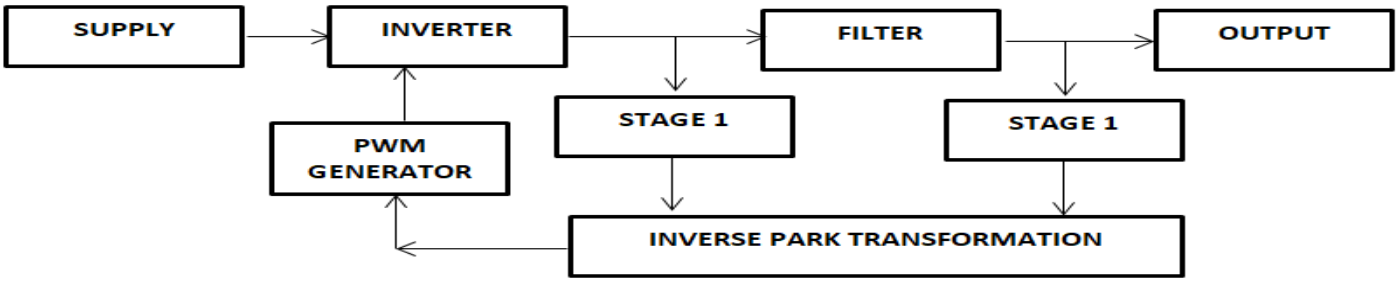


Fig -1: Flow model of inverter design

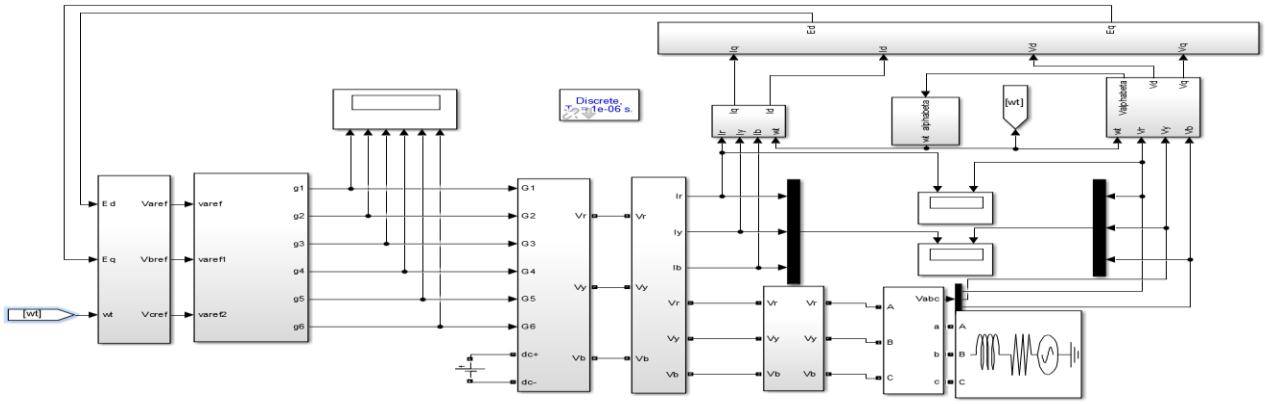


Fig -2: Simulation of inverter design

The first stage block helps to sense the current and plot those sensed current on d-q axis in two stages, first the signal get converted into α_β from ABC(i.e. three phase) and then α_β is converted into d-q. The conversion of ABC into α_β is defined by Clarke transformation and the conversion of α_β into d-q is defined by park transformation. Further the signal get tuned with the help of PI controller and after tuning the single are forwarded to inverse park transformation block to convert the d-q axis signal.

3. RESULT AND DISCUSSION:

As we focus on voltage distortion so we can observe that the result obtained in feedback SPWM is minimum as compare to other and same followed by the current distortion. In case of magnitude of fundamental voltage it remains almost same in all cases. And in case of fundamental current the feedback SPWM follow adaptive pattern.

SN.	Inverter type	THVD%	Voltage Magnitude	THID% (Without L)	THID% (Without L)	Current magnitude (without L)	Current magnitude (witht L)
1	Half wave inverter	48.03	127.3	48.03A	14.67	12.73	6.84
2	Full wave inverter	48.03	254.6	48.03	29.33	25.46	14.2
3	5- level inverter	35.55	202.3	35.55	26.10	20.33	8.656
4	7- level inverter	29.54	200.1	29.54	26.64	20.01	8.52

Table 1: comparison of parameter of single phase inverter

SN.	Parameter	180° conduction mode	120° conduction mode	THIPWM	SVPWM	*Feedback SPWM*
1	THVD%	0.04	0.02	0.09	0.07	*0.00*
2	THID%	97.65	47.87	587.24	33.53	*2.02*
3	Fundamental Voltage Magnitude	587.1	587.1	586.5	585.8	*586.5*
4	Fundamental current Magnitude	1.47	1.7	5.2	7.2	*250*

Table 2: comparison of parameter of three phase inverter

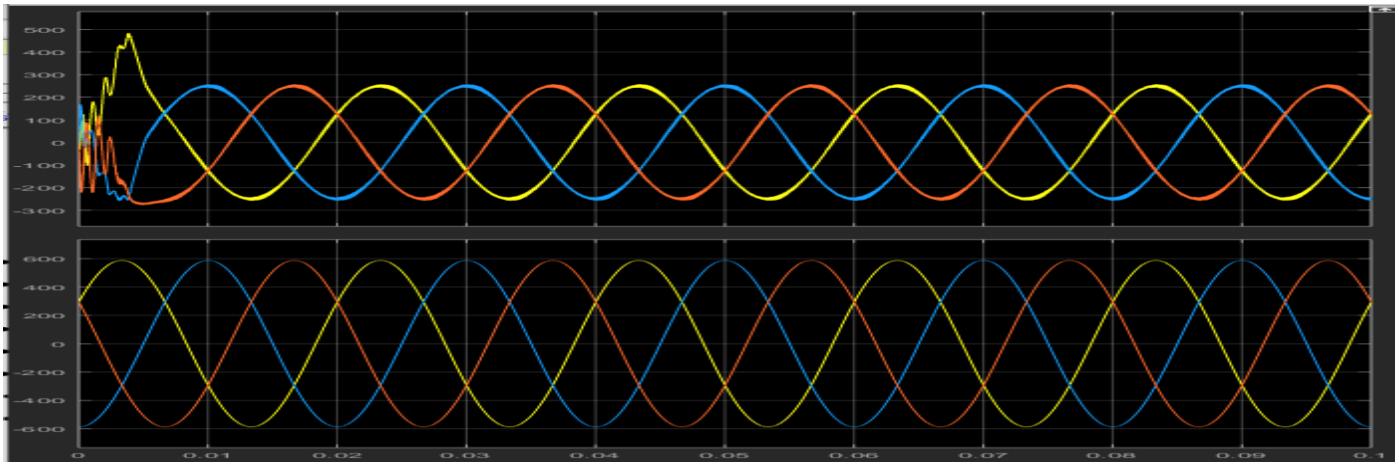
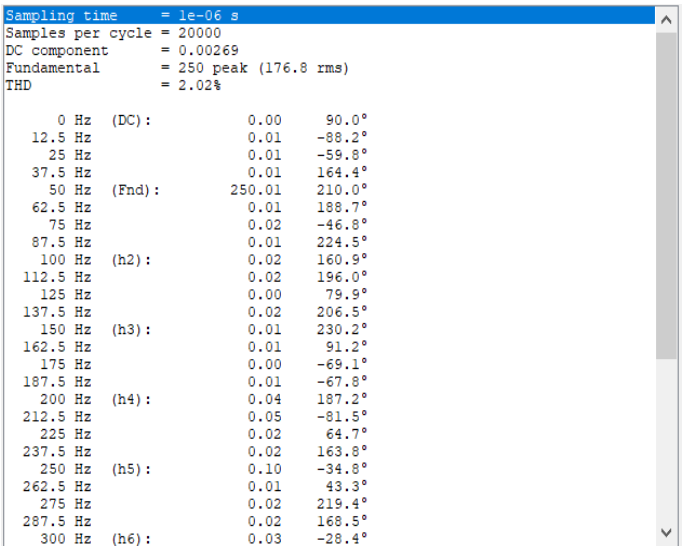


Fig -3: Current and Voltage waveform of three phase feedback SPWM inverter



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Sampling time     = 1e-06 s
Samples per cycle = 20000
DC component      = 0.00269
Fundamental       = 250 peak (176.8 rms)
THD               = 2.02%

     0 Hz   (DC):          0.00     90.0°
  12.5 Hz                  0.01    -88.2°
    25 Hz                  0.01    -59.8°
  37.5 Hz                  0.01    164.4°
    50 Hz   (Fnd):       250.01    210.0°
  62.5 Hz                  0.01    188.7°
    75 Hz                  0.02    -46.8°
  87.5 Hz                  0.01    224.5°
   100 Hz   (h2):          0.02    160.9°
 112.5 Hz                  0.02    196.0°
   125 Hz                  0.00     79.9°
 137.5 Hz                  0.02    206.5°
   150 Hz   (h3):          0.01    230.2°
 162.5 Hz                  0.01     91.2°
   175 Hz                  0.00    -69.1°
 187.5 Hz                  0.01    -67.8°
   200 Hz   (h4):          0.04    187.2°
 212.5 Hz                  0.05    -81.5°
   225 Hz                  0.02     64.7°
 237.5 Hz                  0.02    163.8°
   250 Hz   (h5):          0.10    -34.8°
 262.5 Hz                  0.01     43.3°
   275 Hz                  0.02    219.4°
 287.5 Hz                  0.02    168.5°
   300 Hz   (h6):          0.03    -28.4°
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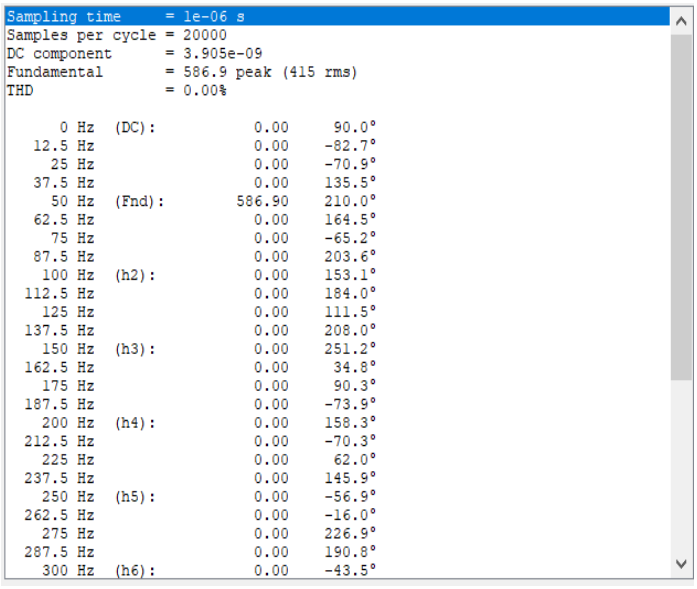
Fig -4: Total harmonic Current distortion



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Sampling time     = 1e-06 s
Samples per cycle = 20000
DC component      = 3.905e-09
Fundamental       = 586.9 peak (415 rms)
THD               = 0.00%

     0 Hz   (DC):          0.00     90.0°
  12.5 Hz                  0.00    -82.7°
    25 Hz                  0.00    -70.9°
  37.5 Hz                  0.00    135.5°
    50 Hz   (Fnd):       586.90    210.0°
  62.5 Hz                  0.00    164.5°
    75 Hz                  0.00    -65.2°
  87.5 Hz                  0.00    203.6°
   100 Hz   (h2):          0.00    153.1°
 112.5 Hz                  0.00    184.0°
   125 Hz                  0.00    111.5°
 137.5 Hz                  0.00    208.0°
   150 Hz   (h3):          0.00    251.2°
 162.5 Hz                  0.00     34.8°
   175 Hz                  0.00     90.3°
 187.5 Hz                  0.00    -73.9°
   200 Hz   (h4):          0.00    158.3°
 212.5 Hz                  0.00    -70.3°
   225 Hz                  0.00     62.0°
 237.5 Hz                  0.00    145.9°
   250 Hz   (h5):          0.00    -56.9°
 262.5 Hz                  0.00    -16.0°
   275 Hz                  0.00    226.9°
 287.5 Hz                  0.00    190.8°
   300 Hz   (h6):          0.00    -43.5°
```

Fig -5: Total harmonic voltage distortion

4. CONCLUSION

After cascading single phase full bridge inverter there is reduction in percent of Total Harmonic Voltage Distortion and Total Harmonic Current Distortion. Use of an inductive load give rise to reduction in Total Harmonic Distortion percent of current but at a same time the fundamental magnitude of current reduces. While cascading there is minor reduction in fundamental magnitude of current and voltage and also give rise to increment of zeroth harmonic order. As per IEEE standard THD should be less than 5% in the system. In d-q control circuit one can vary the current as per their need (but the THID% should not cross the margin of 14% during variation). No major distortion during the variation of voltage. During variation of main supply we can see the distortion in current.

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