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VOLTAGE HARMONIC REDUCTION USING OPEN LOOP CONTROLLED MULTILEVEL INVERTER FOR PHOTOVOLTAIC APPLICATION: A REVIEW

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Abstract: In this paper use of multilevel inverters are being discussed for the photovoltaic applications. A photovoltaic panel produces a Direct current (DC) output and the loads that are used are mostly AC by nature so by using inverters dc output is converted to ac but the output of inverters also have dc components which generates harmonics. In this paper it is discussed that by using multilevel inverters stepped waveform of the output from the PV panel is possible and with the increase of the level a voltage waveform voltage harmonic can be reduced tremendously and harmonic injection due to PV panel integration with the grid can be reduced

Keywords : - Renewable Energy Source, Multi Level Inverter, Photovoltaic Grid Integration, Harmonic Reduction

1 Introduction: In the past 5 to 10 years researches on renewable energy has increased to the large extent. Due to the increase in environmental issues like gas emission and green house effect the need to use renewable energy sources in place of conventional energy sources has also increased. Hydro energy, photo-voltaic (PV) and wind energy are the most extensive and modern technologies as they are having various advantages like reliability, reasonable installation, cost of energy production, environment friendly, and capabilities of supporting micro grids. Among hydro, wind and photovoltaic, the photovoltaic source PV source is considered the best in terms of modernity and considering environment issues. Due to these advantages PV systems are being frequently adopted worldwide as well as in India in past 5 years. The growth rate of PV system is largest among all he renewable energy systems.

The power generated by a solar photovoltaic panel is having DC nature. Thus it becomes very much necessary to convert the DC power of the PV panel into AC power using inverters. With the rapid increase in the electrical power demand in the industrial application the value of the switching current has also been increased. To improve the quality and performance of a PV panel installation it is always preferred to have increase in voltage level but the static and dynamic performance of the semiconductor device at high voltage level deteriorates.

A high power level means the high voltage or current level or both simultaneously. The growth to technical advancement is however slow as compared to the increasing industrial applications and also not availability of efficient high power converters the application of multilevel inverters comes into picture for joining power semiconductors as per the requirement.

The multilevel inverter provides the voltage distribution between the different switches thus decrease the voltage stress on different power converter switches. Many new technologies are being evolved in the field of multilevel inverters in the past few years. Some of the main technology include the flying capacitor type multilevel inverter, the neutral point clamped multilevel inverter as well as cascade H-bridge multilevel inverter.

In this paper all the topologies of a multilevel inverters are discussed along with their advantages and limitations.

2 Inverters

An electrical device which converts direct current to an alternating current is known as inverters. The ac power output of the inverter is used to drive the electrical loads like lights, radar, motor, radio and other electrical devices. It is also used in aircraft system to convert dc power to ac power.

2.1 Inverter Topology

Fig shows the schematic diagram of a single phase H-bridge inverter. It looks like an English letter H that is why it is called as a H- bridge inverter. This type of inverter contains four fully controlled power semi converter switches S_1-S_4.

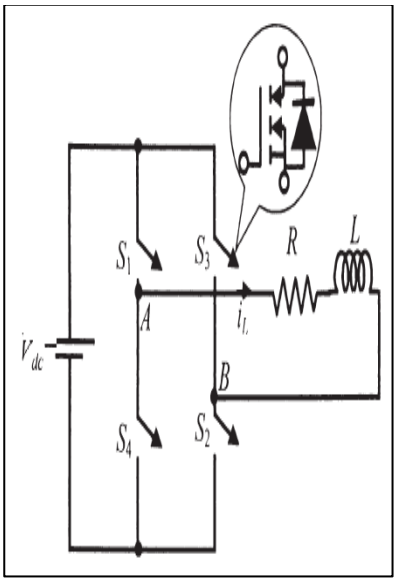

Fig 1 Schematic diagram of an H-bridge inverter

The power semiconductor devices can be MOSFET for low power device or an IGBT for high power application. The use of power semiconductor device as a switch depends upon the power rating and switching frequency of the device. For low power high switching frequency MOSFET are preferred and for very high power low switching frequency GTO are preferred. Generally IGBT's are preferred for mid power and mid frequency application.

A dc source voltage V_{dc} is connected at the input side of the inverter the load is assumed to be a R-L load which is connected between the two legs of the inverter. The switches present in each leg are complementary to each other which mean if one switch is on then another switch present in that leg must be off. The switches works in pair which means when S_1 and S_2 are on then S_3 and S_4 are off. Similarly when S_3 and S_4 are on then at that time S_1 and S_2 are off. Some time delay is provided to turn off each pair. This period is called blanking period. When S_1 and S_2 are on then output voltage is V_{dc} and when S_3 and S_4 are on then output voltage is $-V_{dc}$.

3. Multilevel inverter

The configuration shown in fig 1 is basically a two level inverter as the output can have two levels of voltage that is V_{dc} or $-V_{dc}$. The inverters that can have more than two levels of voltage are called multilevel inverters. A three level inverters can have Vdc, o and –Vdc as the level of voltages, similar to that a 4 level inverter, 5 level inverter and a 6 level inverter will have 4 levels, 5 levels and 6 levels of voltages respectively.

3.1 Diode clamped multilevel inverter

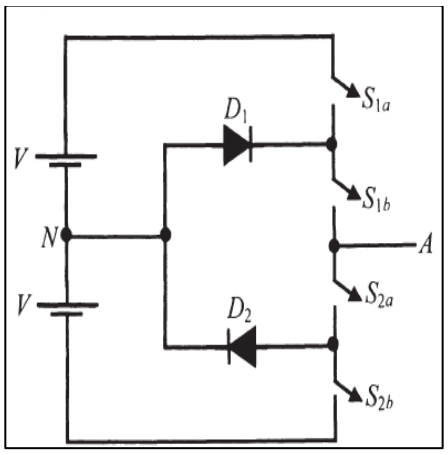

Fig 2 Schematic diagram of a 3-level inverter

Fig 2 gives a schematic diagram of one leg of the 3 level inverter. It contains four switches (S_{la}, S_{lh}, S_{2a} and S_{2b}) and two diodes (D_I and D_2)' each of these switches consists of a power semiconductor device and an anti-parallel diode. Each of the two dc sources supplying the inverter has a magnitude of *V.* The neutral point of these two sources is denoted by *N. A* three-phase inverter can be constructed by duplicating the leg. The output voltage V_{AN} is shown in table 1 for various switch combinations.

S_{1a}	S_{2b}	S_{2a}	S_{2b}	V_{AN}
OFF	OFF	ON	ON	-V
OFF	ON	ON	OFF	0
ON	ON	OFF	OFF	V

Table 1 Output voltage of a 3-level inverter

The schematic diagram of one leg of a four level inverter is as shown in fig 3

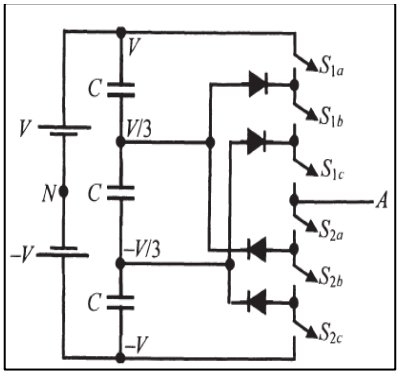

Fig 3 Schematic diagram of a 4-level inverter

This inverter requires the levels + *V/3* and *-V/3* in addition to the levels of + *V* and - *V.* Since the number of

levels is even, the level 0 is not achievable by this inverter. To achieve the above-mentioned dc levels, three capacitors of equal size are connected as shown in the figure. Table 2 lists the four voltage levels across *A* and *N* for various switch combinations.

S_{1a}	S_{1b}	S_{1c}	S_{2a}	S_{2b}	S_{2c}	V_{AN}
ON	ON	ON	OFF	OFF	OFF	V
OFF	ON	ON	ON	OFF	OFF	V/3
OFF	OFF	ON	ON	ON	OFF	-V/3
OFF	OFF	OFF	ON	ON	ON	-V

Table 2 Output voltage of a 4-level inverter

In a similar fashion we can construct five, six or higher level inverters.

3.2 Multilevel Capacitor Clamped/Flying Capacitor Inverter, CCMLI

A schematic diagram of Capacitor Clamped (CC), or Flying Capacitor, multilevel inverter topology is shown in figure 4. It uses capacitors instead of clamping diodes to hold the voltages to the desired values. On a shared DC-bus m-1 number of capacitors are required,

M is the no of levels of the multilevel inverter, and 2(m-1) switch in parallel with anti parallel diode pairs should be used.

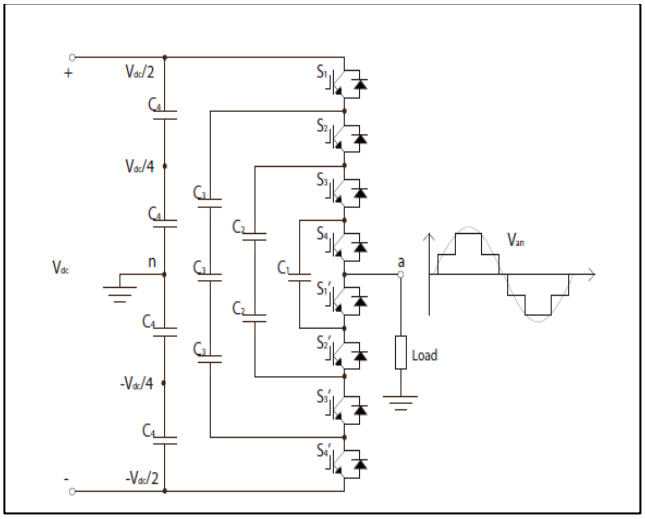

Fig -4 A Capacitor Clamped Multilevel Inverter with five voltage levels

3.3 Cascaded Multilevel Inverter, CMC

A five level cascaded multilevel inverter is shown in the fig 5. Full H- bridge inverters having different DC source are connected in cascade. This setup is done to create the stepped waveform. In Fig 5 one only one leg of a three phase five-level Cascaded Multilevel Inverter is shown. Each full-bridge can be regarded as a module and it is only these modules that build up the CMCI topology. One full-bridge module is in itself a three-level CMCI, and every module added in cascade to that extends the inverter with two voltage levels.

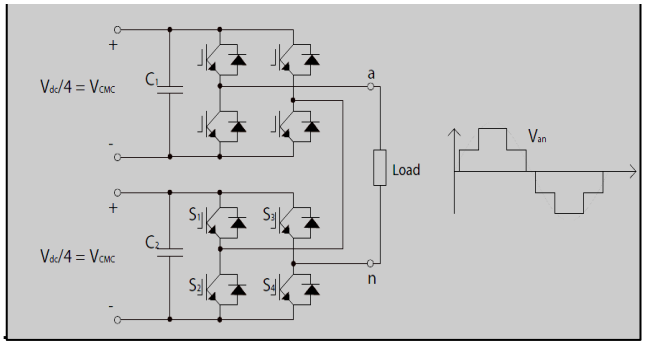

Fig-5 A five-level Cascaded Multilevel Inverter

4. Modulation methods of multilevel inverter

Modulation in a multilevel inverter can be categorized into two groups of method. In one group modulation is done with fundamental switching frequency and in another group modulation is done with a high switching frequency. Both group uses a PWM technique for modulation. With the modulation with both types of methods output waveform is a stepped wave. Also the space vector PWM method is also a choice to be used for the multilevel inverters.

4.1 PWM for two-level inverters

By comparing the reference wave with the triangular carrier wave PWM of the two level inverter is achieved. The desired output voltage wave is taken as a reference wave the amplitude of the carrier wave that is a triangular wave is same as the reference wave but it has higher frequency compared with the reference wave. The frequency of the triangular carrier wave must be on higher side at least more than double the frequency of the reference wave.

Carrier wave frequency is often in the range of KHz in electric power application. The change in switching states depends upon the frequency of the reference wave. Switching occurs every time the triangular wave crosses the reference wave. Fig 6 shows a plot of the ordinary two-level PWM reference, carrier wave and output voltage.

When the carrier wave crosses the reference wave its magnitude becomes higher than the reference wave the

top switch of the two level inverter turns off and bottom switch turns on so that $V_{dc}/2$ becomes the output. Again when the carrier wave crosses the reference, its magnitude getting lower than the reference wave , the switches change state and the output becomes $-V_{dc}/2$. When the reference is positive the output voltage signal will be $V_{dc}/2$ for the majority of the time resulting in a positive output AC signal following the reference. An straight forward example is if the reference wave is constant at zero voltage, the carrier wave would then cross it upwards and downwards with the same time between every crossing, making $V_{dc}/2$ and $-V_{dc}/2$ being the output for equal time, each cycle. This leads to that the average output voltage over one carrier wave period becomes zero.

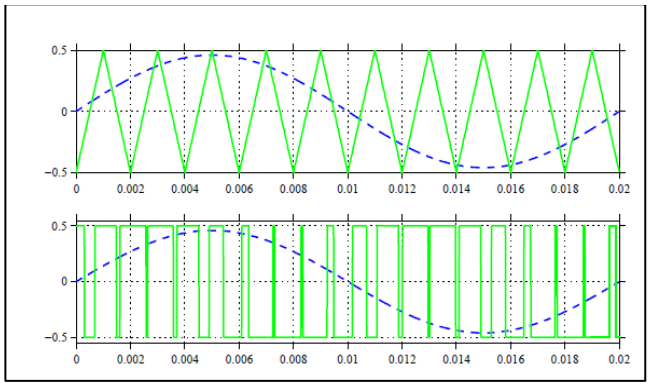

Fig 5- PWM reference (dashed) and triangular carrier (solid) wave in upper plot and output voltage (solid) eave in lower plot

4.2 PWM for multilevel inverters

Multilevel PWM methods uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave, much like in the two-level PWM case. To reduce harmonic distortions in the output signal phase-shifting techniques are used .There are several methods that change disposition of or shift multiple triangular carrier waves. The number of carrier waves used is dependent to the number of switches to be controlled in the inverter.

5. Selective Harmonic Elimination

Selective Harmonic Elimination (SHE) is a low switching frequency strategy that uses calculated switching angles to eliminate certain harmonics in the output voltage. With the help of Fourier series analysis the amplitude of any odd harmonic in the output signal can be calculated. Usually the switching angles are chosen so that the fundamental is set to the wanted output amplitude and the other harmonics to zero see Figure 3.7. The switching angles must however be lower than π/2 degrees and for a number of switching angles a harmonic components can be affected, where a-1 number of harmonics can be eliminated[16] (one angle to set the fundamental). If angles were to be larger than π/2 a correct output signal would not be achievable. For an inverter with m levels a = $\frac{m-1}{2}$. Higher harmonics can be filtered out with additional filters added between the inverter and the load if needed. For a five-level inverter a = 2, so there are two switching angles available and a - 1 = 1 angles can be used for harmonic component elimination.

6. Conclusions

It is concluded that by using a multilevel inverter we can reduce the harmonic injection by inverters to the grid in photovoltaic grid integration. Multilevel inverter topologies and its modulation and control techniques are studied and in future emphasis will be laid to model a multilevel inverter and do the optimal controlling so as to do the photovoltaic grid integration with minimal injection of harmonics.

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