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Low Power Phase Locked Loop Design Techniques

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Abstract - *Phase Locked Loop (PLL) is a closed loop, negative feedback system. This paper gives investigation carried out of study of various PLL architectures for low power and performance applications. Also, an attempt of understanding different technologies and reviewing the different methods of designing a low power PLL has been made. This paper proposes a low power PLL design with reduced phase noise and jitter. The proposed PLL can be utilized in applications up to 1GHz with low power consumption. For low power PLL it is proposed to use dynamic logic for PFD architecture and MTCMOS technique for the footer which will minimize the subthreshold leakage current by variation of Vth.*

Key Words: **Phase Locked Loop (PLL), Phase Frequency Detector (PFD), Charge Pump (CP), Low power techniques, Current Starved Voltage Controlled Oscillator (CSVCO).**

1. INTRODUCTION

In Communication Systems, PLL has wide applications like radio, telephone, mobile phone, PCs etc. PLLs are mainly used for clock synthesis, jitter reduction, frequency synthesis, bit synchronization and skew reduction etc. Phase Locking is also used in electronics and instrumentation applications which include memories, microprocessors, hard disk drive etc. PLL can be designed to operate both for analog and digital signal processing. Phase Locked Loop is a negative feedback control system which compares the phase and frequency of the input signal with the feedback signal and detects the error [1]. If there is no error, then the loop is locked. The basic block diagram of a PLL [1] is as shown in Fig 1. It consists of Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LPF), Voltage Controlled Oscillator (VCO) and Frequency Divider (FD).

The main block of a PLL is PFD which compares the phase and frequency of the input reference signal with feedback signal and detects an error- UP or DOWN signal. PFD consists of 2 resettable D flip flops which compares the rising edges of both input and feedback signal. If the rising edge of input signal leads the feedback signal, then 'UP' signal will go 'high' and 'down' signal goes 'low' and vice versa. The charge pump is a kind of DC to DC converter that uses capacitors for energetic charge storage to raise or lower voltage. It converts the pulse output of PFD into a current output. The Loop Filter removes the ripples in the Charge pump output, blocks the high frequency and allows only desired range of frequency. VCO is the most important component of PLL which generates the output frequency corresponding to control voltage. The Frequency divider is used to scale down the VCO output frequency by 'N' to match with the locking range of PLL.

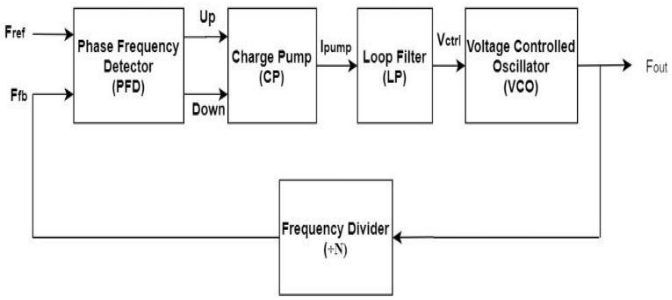

Fig -1: Block diagram of PLL

Section II describes the design methodology with various techniques used for low power PLL design. The proposed design is briefly explained in section III. Conclusion is drawn in section IV.

2. DESIGN METHODOLOGY

Many researchers have undertaken different techniques for designing PLL and its components. Most of the researchers have carried out the research work in the view of increasing frequency or reducing parameters such as area, power consumption, jitter, phase noise etc. Various researchers have presented papers on low power PLL design by modifying the design of various PLL components and parameters like supply voltage, threshold voltage, etc.

2.1 PLL design using less number of transistors:

Fig 2(a) shows the design of a conventional PFD that requires 54 transistors which increases area, power consumption and dead zone. In the paper [2] and [10], the modified PFD is designed by positive edge triggered D flip flops using dynamic TSPC logic as shown in Fig 2(b) utilizes only 19 transistors which is very less compared to a conventional PFD. In this PFD design, dead zone is limited to 0.01ns. Hence by reducing number of transistors, area and power consumption can be reduced. The design uses 0.8µm technology with 5V power supply.

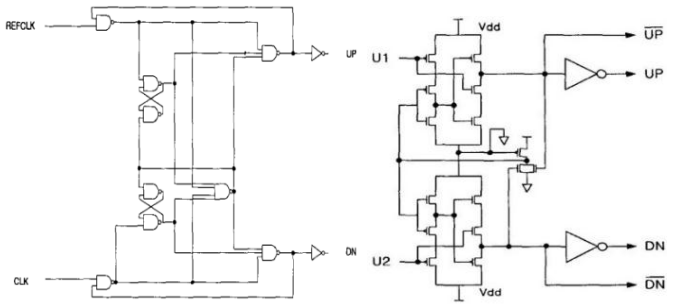

Fig -2(a): Conventional CMOS PFD Fig **-2(b)**: PFD using dynamic TSPC Logic

The switches in the conventional charge pump are replaced with transmission gates to reduce the clock feed through and current mismatch. The output impedance is improved by using cascode current sources. The design employs 2nd order loop filter and ring based CSVCO which produces an output frequency of the range 650MHz up to 1.4GHz and gain value is -592MHz/V. The measured phase errors and jitter are 12ps and 15ps at 1.27Ghz input reference.

2.2 PLL design using low power supply voltage:

In paper [3], the authors have developed a PLL with 0.18µm technology, using supply voltage of 0.7V in CMOS process. The PLL consists of a dynamic Phase Frequency Detector, modified CP with gate switches, third order Loop filter, VCO designed with bulk driven technique, FD with conventional static D flip flops. In addition to these blocks, the designers have also included a Delta Sigma modulator to enhance the output frequency resolution and a Calibration Circuit (CC) for automatic frequency tuning.

They have incorporated 2 switches in the charge pump to reduce the static power dissipation (from supply to the ground). Since the biomedical application requires small area, power consumption and minimum sensitivity to process variations, the authors have selected three stage fully differential ring based VCO rather than LCVCO. Fig 3 shows the design of VCO with bulk driven technique. Each delay cell has programmable capacitive load for tuning which is digitally controlled by 2 switches. The programmable Frequency Divider block consists of Pre-scalar circuit designed from DFFs (using E-TSPC logic to design divide-by-2/3 units) which reduces power consumption and increases speed.

A DSM (Delta Sigma Modulator) is incorporated which generates the data from FD output causing uniform distribution of quantization noise and randomizing spurious tones. Since higher order DSMs occupy more area, increases design difficulty and introduces extra poles and loses stability, 3 order DSM is chosen in this design.

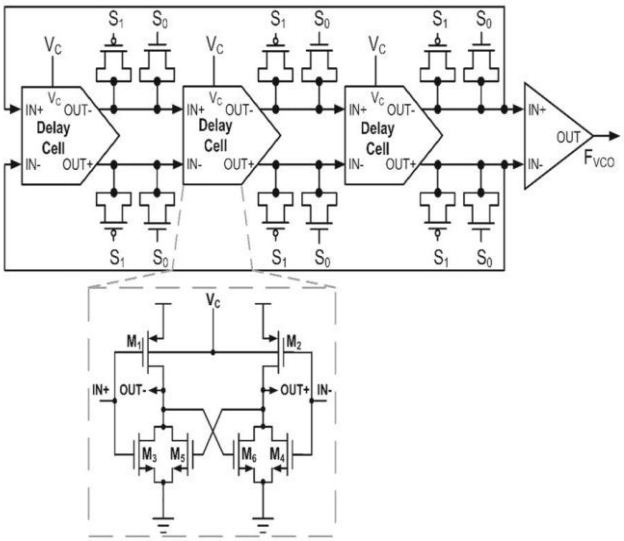

Fig -3: VCO design with bulk driven technique

In order to compensate for process variation, a Calibration Circuit (CC) is added to the design which takes control voltage information from the VCO (Vctrl) to decide whether to calibrate or not. The overall power consumption of the PLL is 0.425mW at a supply voltage of 0.7V with 405MHz operating frequency. The measured phase noise and reference spurs are -99.49dBc/Hz at 1MHz offset and -48.04dBc respectively.

2.3 PLL design using Bulk driven technique:

In paper [4], low power PLL is designed by utilizing a CMOS process of 0.18 m with 1.8 V power supply. The PFD design in this paper is a modified version of dynamic TSPC logic (8 transistors) where signals are applied through delay elements to nullify the dead zone. Operating frequency of PFD is calculated by the sum of rise and fall time. It can be observed that PFD design in this paper has low power performance of 0.3mW at 5GHz frequency. The design simulated in HSPICE.

Fig 4 shows the charge pump designed using modified Wilson current mirrors to improve the output swing and increase the output resistance. Wilson current mirror charge pumps reduces loop gain of the circuit since transistors are placed in cascaded form. This problem is solved using modified version of Wilson Current mirror. Bulk driven technique is used wherein bulk voltage (V_{SB}) of the substrate is reduced which in turn reduces the threshold voltage of the transistor. The designed charge pump provides high gain with faster switching.

The PLL employs two stage CSVCO and has wide locking range from 500MHz to 5GHz. The rms and peak-to-peak jitters measured are 0.671ps and 3.46ps respectively at 3GHz frequency. The reference spur is measured as -72 dBm and output phase noise is -117.6dBc/Hz with 1.85GHz and 1 MHz frequency offset.

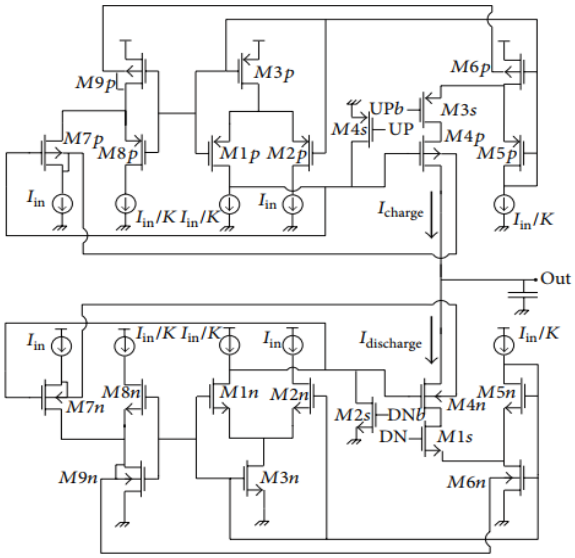

Fig -4: Charge pump using Wilson current mirror

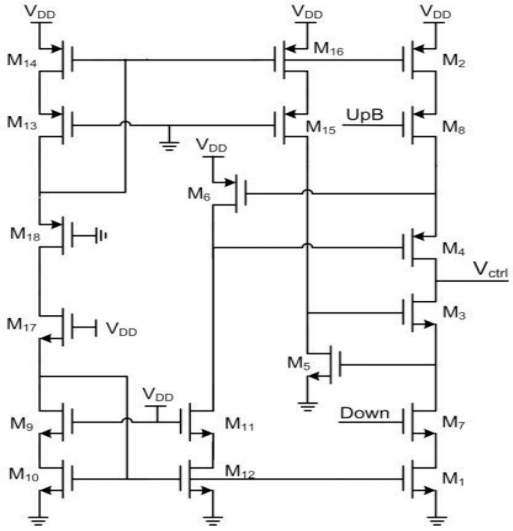

Fig -5: Gain boosting Charge pump

2.4 PLL design using gain boosting:

The PLL in paper [5] is designed with 0.18µm feature size, 1.8V power supply using Tanner 13 tool. The PFD block is designed by using modified D flip flops with TSPC logic and exhibits zero dead zone from 10MHz to 1GHz. Fig 5 shows a gain boosting charge pump with transistors M7 and M8 acts as controlled switches. The transistors M9 to M16 forms the lower cascode current mirror with biasing voltage of VDD and GND biasing voltage for PMOS switched mirror is chosen. The current generated by M17-M18 transistor pair reduces the power of charge pump. This charge pump improves the output swing of 0.1 to 1.6V and reduces current mismatching.

A third stage CSVCO is incorporated in the design to produce an output frequency up to 2.15GHz. Frequency Divider is designed by using 2 identical D flip flops in master slave configuration to perform ½ division. The PLL locks at 300ns and maximum power consumption is 3mW.

2.5 PLL design with Level Shifter:

In paper [6], the authors have designed a PLL for clock multiplication application in Low Voltage Differential Signaling (LVDS) transmitter. The PFD is designed with dynamic logic using TSPC D flip flops.

Two transistors are inserted to reduce the charge sharing effect in the charge pump. The VCO design in Fig 6 consisting 3 blocks: Voltage to Current converter which converts the input voltage into biasing current which is then fed to a Current Controlled Oscillator (CCO). The CCO generates the oscillations based on the biasing current. The 3rd block is a level shifter which converts the small voltage input into rail to rail output voltage. The design uses a second order LPF.

A low power consumption of 12mW is achieved with a 3.3V voltage supply. The lock range of PLL is in the range of 100 MHz – 560 MHz, hence the designers claim that it can be used for LVDS transmission.

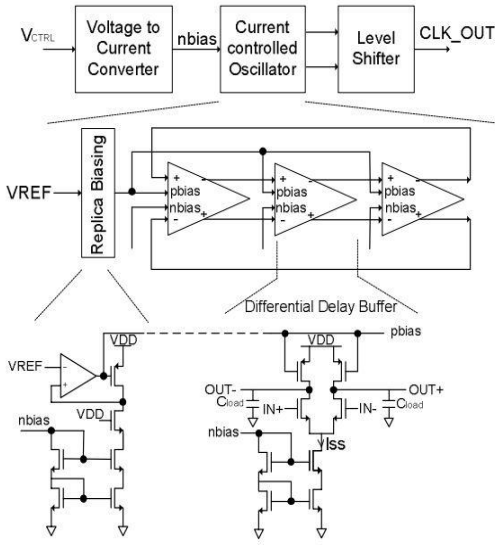

Fig -6: VCO design using Level Shifter

In paper [7], authors have designed a 3rd order PLL for low power application. The design comprises of a high speed, low power PFD in dynamic logic using TSPC D flip flops. The PFD design uses NAND gate in reset path. A single ended charge pump is designed with a gain of 3.18uA/rad in

350nm technology node to minimize non-idealities like charge sharing etc.

The designers have used 2nd order loop filter with loop bandwidth of 1.25MHz. The CSVCO design is similar as in [4] with 3 blocks in VCO design. The gain of VCO is measured to be 220MHz/V. The frequency divider (divide by 7 factor) is designed by using D flip flops, NAND and NOR gates from the standard library.

The low power PLL in this paper is designed in 350nm technology node and operates for a reference frequency in the range of 20MHz- 2GHz. The low power technique used in this PLL is the addition of decoupling capacitors in the power supply to reduce the noise (of the power supply) and thereby reducing the switching activity. The designers have also compared the PLL results with and without decoupling capacitors at several technology nodes. After analyzing the result, they have concluded that the power consumed by the PLL with decoupling capacitor is reduced to 37% at 350 MHz with 3V power supply. The measured RMS Value and average value are 1.7V and 1.3V respectively. The power consumption of PLL is reduced to 20% at 3V power supply without decoupling capacitor.

3. THE PROPOSED LOW POWER PLL

The study of various research papers and investigations shows that usage of minimum transistors, low power supply and other power optimization techniques [8] play a vital role in the design of low power PLL. The proposed low power PLL is being designed using 45nm CMOS technology with 1V supply and simulated using LTSpice XVII. The proposed 3rd order PLL consists of PFD using dynamic logic, charge pump with current mirror. Fig.7 is the proposed model of low power PLL with multi threshold technique where high current circuits will be connected to footer transistor. The circuits inside the PLL are represented by C1, C2, ……Cn

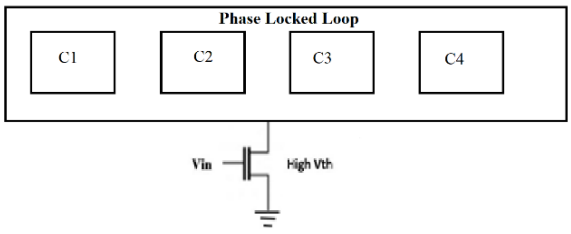

Fig -7: The proposed model of low power PLL

It is recommended to implement D flip flops designed by TSPC logic. A ring oscillator based current starved 5 stage VCO is being designed which can operate up to 1GHz with around 0.1GHz as Kvco (gain of VCO). Bode diagram to be plotted using MATLAB Simulink by designing specification like unity damping factor, phase margin value etc. After achieving suitable stability factor, the proposed PLL will be designed and simulated using LTSpice XVII.

4. CONCLUSIONS

It can be observed that modification in the conventional design have fetched good results in terms of area, power and speed in low power PLL design. Good immunity towards phase noise, low jitter, minimum (or zero) dead zone, low power consumption etc. has been achieved by designers using less number of transistors, low power supply voltage, bulk driven techniques, gain boosting methods and using level shifters. For low power PLL it is proposed to use dynamic logic for PFD architecture and MTCMOS technique for the footer which will minimize the subthreshold leakage current by using variation in V_{th} by selecting multi threshold library or by variation of W/L ratio[9].

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