International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 07 Issue: 10 | Oct 2020 www.irjet.net p-ISSN: 2395-0072

REVIEW: GHz Bandwidth Low Power Low Noise CMOS Amplifiers Using Different Topologies for Wireless Applications

Raj Kumar Tiwari[1], Shiksha Jain[2]

[1]Professor, Dept. of Physics and Electronics, Dr. R.L.A. University Ayodhya, U.P, India
[2]Assistant Professor, Dept. of ECE, I.E.T., Dr. R.L.A. University Ayodhya, U.P, India

---

Abstract - *This review paper represents the demand of low power low noise broadband CMOS amplifier from the last two decades using different topologies for wireless applications. The circuit designing of very high-performance CMOS amplifiers is a vigorous research area and is of major necessary part for modern wireless communication applications. Low power low noise GHz bandwidth CMOS amplifier's architectures can be designed using various types of topologies like: Current reused topology, Resistive feedback topology, Common source cascaded topology, Noise cancellation technique and active Inductor topology etc. In this review paper, we discuss the circuit designing, uses, issues and recent trends of broadband CMOS amplifier are revised to obtain high performance parameters of amplifiers using CMOS technology in last two decades.*

***Key Words*: CMOS Amplifier, High Bandwidth, Wireless Applications.**

1. INTRODUCTION

From the last two decades, the pressure to design the electronics circuit of CMOS amplifier with low power low noise high bandwidth for any wireless applications is growing day to day. It is very critical task for electronics industry and limited by radio frequency front-end. In the broadband communication system, high performance parameters likes: high speed, very low noise, high data rates, cheap, low power consumption with compact designs are in remarkable and in demand due to electronics industries competition. The broadband amplifiers play the major role to transfer the large data in wireless communication systems [1] [2]. The symbolic diagram of wireless communication system is shown in following fig.1. In this figure, low noise amplifier can be replaced by the high bandwidth CMOS amplifier with very low noise and low power consumption.

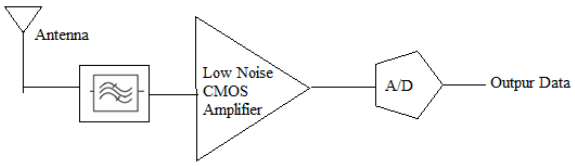

FIGURE 1: Wireless Communication System for Broadband Applications

In the case of heterodyne receiver for communication shown in fig.2, Low noise amplifier using CMOS technology is a major input part to amplify the weak signal with low noise and is usually preceded by a filter (reject the unwanted signal and accept the wanted necessary signal).

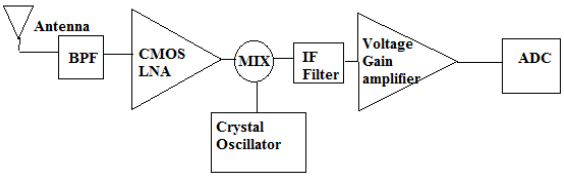

Figure-2: Heterodyne Receiver for Communication System

There is a growing requirement for the wireless communication to make nano devices use as a portable devices with high bandwidth wireless applications. It has many challenges like power consumption, high gain, low noise figure, high linearity [3][4]. Many authors have presented the ideas to design the low power low noise CMOS amplifier using various topologies for different purpose. These are seeing in following survey.

This review paper presents existing work done by various authors and researchers in the electronics communication field to design CMOS amplifiers. From the last two decades various topologies have used to achieve high performance of CMOS amplifier. These are follows:

1. Current reuse topology

2. Cascade common source amplifiers topology
3. Source degeneration topology
4. Resistive feedback topology
5. Cross coupled capacitor technique
6. Gm- boosted topology
7. Noise cancellation technique
8. CMOS Active inductor etc.

One of the most efficient recent techniques is CMOS Active inductor. This can be used in the place of inductor to increase the bandwidth of the amplifier with low noise and low power. Because during its survey, I found that CMOS transistors have required little electrical current comes from switching as capacitors are changing from one state to another state. Additionally, the complementary semiconductors work together to control the output voltage and current. This result provides low-power consumption based circuit design that generate off minimal heat. Due to this reason, CMOS transistors have mostly used in the implementation of modern low noise low power amplifier than previous designed transistors (such as MOS, FET, NMOS and CCDs in camera sensors) [5].

2. SURVEY OF EXISTING WORK FROM LAST TWO DECADES

We can't gain and update our knowledge about the low noise low power CMOS amplifiers without surveying earlier proposed research done by our researchers / scientists in respective field. The earlier topologies and design concepts given by researchers are very helpful in our research to obtain a required task for modern wireless communication systems. The following literatures from the last two decades are reviews with different topologies:

Year 2000

IEEE members: Brain M. Ball Weber, Ravi Gupta and David J. Allstot had presented a fully integrated 0.5 – 5.5 GHz CMOS distributed amplifier. This distributed amplifier is four stage distributed amplifier. A 0.6 µm three layer Al metal is used to fabricate using digital CMOS process. It is a complex method to implement the amplifier with a gain of 6.5 dB and power dissipation is 83.4 mW from a 3V supply. The worst-case return losses on the input and output of amplifier are -7dB and -10 dB, respectively. All types of differential amplifier using CMOS technology has gain stages which are connected such that their capacitances are separated, yet the output currents still combine in an additive fashion[6][7].

Year 2005

In 2005, CMOS low noise amplifier had proposed based on cross-coupled Gm-boosting by the authors W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio. This topology is capable to reduce the whole power consumption of system and improve the noise figure of a common gate LNA. The topology also enables a significant reduction in voltage and current consumption. This type of low noise amplifier consumes 3.6 mA from 1.8 V and attains a measured NF of 3.0 dB at 6.0 GHz. The proposed amplifier has major features due to cross-coupled Gm-boosting topology and makes attractive for low- power low noise high-frequency integrated designs.[8]

Year 2005

Chang-Wan Kim, Min Suk Kang, Phan Tuan Anh and Hoon-Tae Kim proposed the ultra wideband low noise amplifier with a resistive shunt feedback topology. This topology provides large band input matching with small noise figure. This was possibility to reducing the Q-factor of narrowband LNA input. This topology enables a large band of 3.1GHz to 5GHz in wireless systems with gain bandwidth of 2 to 4.6GHz. This amplifier was implemented by 0.18-/Splmu/m CMOS technology by consuming 12.6 mW powers [9][10].

Year 2006

Stanley B. T. Wang, Ali M. Niknejad, and Robert W. Brodersen presented a sub-mW fully differential CMOS low noise amplifier for ultra wide band applications. It was operating at less than 960 MHz for sensor network applications. They utilized MOS transistors (NMOS and PMOS) to boost the transconductance, coupling the input signals and combining the common-gate and shunt-feedback topologies. By using this process, we can achieves 13 dB of power gain, a 3.6 dB minimum noise figure with only 0.72 mW of power consumption from a 1.2 V supply.[11]

Year 2007

Senior member IEEE: Chih-Fan Liao and Shen-Iuan Liu presented the ultra wideband low noise amplifier for 3.1 to 10.6GHz ultra band using noise cancelling topology. Noise cancelling topology enables to suppressed noise from the matching device over the desired ultra wideband. Fabricated low noise amplifier using 0.18µm CMOS process, achieves a 9.7dB power gain over a -3dB bandwidth of 1.2 to 11.9GHz with 4.5-5.1dB noise figure. This was capable to consume minimum power of 20mW from a 1.8V input supply and cover only 0.59mm^2 area of an integrated chip[12].

Year 2007

IEEE members: Yueh-Hua Yu, Yi-Jan mery Chen and Deukhyoun Heo presented the designing of low power ultra wideband low noise amplifier using inductive degeneration topology. It was implemented using 0.18µm CMOS technology. The inductive degeneration is applied to the cascaded common source amplifier as a distributed amplifier to reduce the noise figure and improve the gain at high frequency. This designing was produce noise figure of 4.65 dB, gain of 10dB with low power consumption of 7mW. This was very helpful for broad band communications [13].

Year 2008

Kambiz Moez and M-1 Elmasry proposed a CMOS amplifier for ultra wide band application using differential topology. Kambiz Moez investigate and shows that resistive- inductive network can be used instead of terminating resistor of the gate transmission line and tolerate degraded input matching at low frequency for ultra wide band wireless applications. It was need to operate above 3 GHz. That designed distributed amplifier to obtain a flat gain of 12 dB with average noise figure of 3.3 dB at 30 mW power consumption [14]. Che -Cheng Huang, Zhe - Yang Huang and Yeh - Tai Hung are also presented a CMOS current reused low noise amplifier for wireless receiver by using two cascode common source amplifiers and output Buffer. This presented amplifier had a wide band 3.1 GHz - 12.2 GHz at very low power consumption (13.9 mW) with higher gain 13.1 dB [15].

Year 2009

Sanghoon Joo, Tae-Young Choi, and Byunghoo Jung presented a technique to achieve a low power low noise ultra wideband CMOS amplifier which consist of the advantage of g_m-boosting from inductively degenerated topology and input impedance matching from resistive feedback topology. The gain of the low power low noise CMOS amplifier increases by the quality factor of the series passive input network and its NF was reduced by a similar factor. By exploiting the g_m-boosting property, The proposed fully integrated CMOS low noise amplifier achieved a noise figure of 2.0 dB and consuming 2.6 mW from a 1.2 V supply [16].

Year 2010

Abisak Worapishet, Ittipat Roopkom and Wanlop Surakam Pontorn had introduced drain line impedance tapering technique to achieve simultaneous high gain and bandwidth. This technique was capable to given 3.2 GHz, 25.2 dB hybrids cascaded double stage distributed amplifier. This drain line impedance tapering technique was able to produce low power low noise distributed amplifier [17] [18]. Chuan Chen and Jeng – Rem Yang proposed 3-10 GHz CMOS distributed amplifier with low power low noise and high gain for UWB system and simulated on 0.18 um CMOS technology. This proposed amplifier is used current reused technique with a peaking inductor and achieved flat response at average NF of 3.4 + 0.36 dB with 14.8 mW power dissipation [19].

Year 2011

Meng Zhang and Zhiqun Li had presented a low power low noise differential amplifier for wireless sensor network in TSMC 0.18 m RF CMOS process. A two-stage cascade common gate topology and two external inductor choke coils were used to achieve input matching of LNA under low power consumption and a differential inductor has been designed as the load to achieve reasonable gain and reduce chip area simultaneously[20]

Year 2012

Muhammad Khurram and S. M. Rezaul Hasan proposed a new designing of amplifier that takes the advantage of the current- reuse technique by “stacking”

the active PMOS stage (that provides the inverting g_m-boosting gain between the source and the gate terminals of the input stage (Common Gate) on top of the input CG stage "piggyback g_m-boosting". The new proposed design reduced the power dissipation associated with the g_m-boosting, by implementing the "current-reused g_m-boosting", where the bias current is shared between the g_m-boosting common source stage and the common gate amplifier. They represented a low-power CG UWB LNA architecture which implements a novel "current- reused-boosting" technique. The topology also includes a front-end passive LC-band-pass filter for broadband input matching with sharp out-of-band roll-off. Proposed architecture represents a low-power CMOS transconductance "g_m" boosted ultra wideband LNA using common gate, operating in the 3–5 GHz range, employing current-reuse technique [20].

Year 2013

Jun Da Chen also proposed the new techniques based low power ultra wide band low noise amplifier using 0.18 um CMOS technology but this proposed amplifier achieved 3 to 7.5 GHz bandwidth with 4.6 – 5.3 dB noise figure by using source degeneration input matching technique. The performance of this amplifier was not better than the others but it was complex in designing [21]. While Shivani and Mr. Prashant Gupta also represented the extremely low power consumption (363 uW) high bandwidth (71.37MHz) amplifier with high phase margin (81^0) and simulated on Orcad cadence simulator at 1.2 V power supply. It was very useful to make a trade-off between low power consumption and high phase margin with high gain. [22].

Year 2014

On the other hand, Sana Arshad and Rashad Ramzan also proposed the ultra wideband low noise amplifier by using noise cancellation topology and simulated by CMOS technology. The main object of this designing is to achieve the very low noise at high frequency band in amplifier. It was widely used in the wireless communication system & found low power consumption 363µW [23].

Year 2015

While, in 2015, Xiao – Peng Yu and Wen Lin Xu had proposed the designing of 48-62 GHz ultra wideband low noise amplifier using 65 nm CMOS technology. This proposed amplifier includes two techniques like Current Reused Technique and Cascade Common Source Amplifier. First technique is used to increase the frequency band up to 10 GHz and second technique is used to change gain with Stagger tuning topology at 1.5V. This proposed amplifier included large value of inductor and consume large area chip [24].

Year 2016

Amir. Mahdavi and Fatemeh .Geran had presented the ultra wideband amplifier circuit using common gate and cascade topology. It was implemented using 0.18 µm based CMOS technology under TSMC. This proposed amplifier produced maximum gain of 22.1dB over a high bandwidth of 3.1GHz-10.6GHz with low power consumption 1.3mW. The wideband input impedance matching of LNA is obtained by employing a degenerating inductor (|S11|<-7.5 dB) [25].

Year 2017

Monsen Hayati and Sayad Cheraghali presented an ultra wide band LNA included four technique: Noise Cancellation Technique, Current Reused Technique, Source Degeneration and Resistive Feedback Technique. It operates between 3GHz-12GHz frequency band. In this presented amplifier, circuit is a combination of noise cancellation technique and current reused technique to achieved the enhance bandwidth with high gain at low noise figure with supply voltage 1.8 V. In addition, good input impedance matching can achieved with inductive source degeneration and resistive feedback techniques with 23.23mW power consumption and 1.721dB noise figure [26].

Year 2018

In recent year 2018, some authors like S.Manjula, M . Malleshwari, and M.Suganthy together presented a new designing of low power ultra wide band low noise amplifier using a CMOS active inductor. It is reliable for the wireless local area network receiver. Active inductor is

employed at the input stage of the amplifier for input impedance matching to reduce the chip size. The proposed amplifier produces the ultra wide band of frequency of 3.1 to 10.6 GHz with high gain 10.74+ 0.01 dB, 4.85dB noise figure and very low power consumption. It is simulated on 0.18µm CMOS technology [27].

Year 2019

In recent year 2019,Jiaqian Wu and Zhangfa Liu presented the designing of ultra wideband low noise amplifier. This designing is based on cascode configuration with resistive feedback. The main objective of this amplifier is wideband input impedance matching with high gain and low noise as compare to previous proposed designing of amplifier. It is simulated on SMIC 40nm CMOS process. The circuit simulation results represent the less than noise figure of 4.5dB with wide frequency range of 3.5-31-GHz [28].

All above research papers based on different topologies for wireless communication are comparing to each other. It is shown in following table-1.

3. CONCLUSION

According to the above survey of existing work, many topologies have been used to design ultra wideband low power low noise amplifier. After the survey of literature, we found that the cascade configuration with resistive feedback topology is more suitable to design the low power, low noise wideband CMOS amplifier for wireless application. It is depend on number of cascaded circuit. But I have analyzed that more research is necessary regarding circuit designing parameter measurements, modeling and simulation to achieve extremely low power consumption, wide frequency band, low noise figure with noise less CMOS amplifier for modern wireless communication applications.

REFERENCES

[1] Robert L. Boylested and Louis Nasnelsky Electronics devices and circuit theory Prentice Hall is an Imprint of Pearson, tenth edition, pp. 578-582 (2009).
[2] Intel UWB website: http://www.intel.com/technology/ultrawideband/
[3] B. Razavi, Design of Integrated Circuits for Optical Communications, McGraw-Hill, 1st ed, September 2002.
[4] G. R. Aiello, “Challenges for ultra-wideband (UWB) CMOS integration”, IEEE MTT-S International Microwave Symposium Digest, vol. 1, pp. 361 -364, 8-13 June 2003.
[5] Nell H.E. Weste and Kamran Eshraghian, “Principal of CMOS VLSI Design”, Reprinted with June1988.
[6] B. Ballweber, R. Gupta and D.J. Allstot, “Fully Integrated CMOS RF Amplifier,” in IEEE Dig. Tech.Papers, 1999, PP.72-73.
[7] Brain M. Ballweber, Ravi Gupta and David J. Allstot, Fellow IEEE, “A Fully Integrated 0.5 GHz - 5.5 GHz CMOS Distributed Amplifier”, IEEE Transactions on solid state circuits, vol.35, No.2, February 2000.
[8] Zhuo, W. Li, X. Shekhar, S. Embabi, S.H.K. Pineda de Gyvez, J. Allstot, D.J. and Sanchez-Sinencio, “A Capacitor Cross-Coupled Common-Gate Low-Noise Amplifier’ IEEE Transactions on Circuits and Systems-II: Express Briefs. 52:875-879 2005.
[9] Chag – Wam Kim, M.S. Jung, Sang Gug Lee, “Ultra wideband CMOS LNA”, article in Electron LETT, May 2005.
[10] C.P. Chang and H.R. Chuang, “0.18 µm 3-6 GHz CMOS broadband LNA for UWB radio”, article in Electronics Letters, July 2005.
[11] Wang, S.B.T. ; Niknejad, A.M. and Brodersen, R.W, “Design of a Sub-mW 960-MHz UWB CMOS LNA”, IEEE Journal of Solid-State Circuits. 41: 2449-2456 2006.
[12] Chin – Fan Liao, Shen – Iuan Liu, “A Broadband Noise Cancelling CMOS LNA for 3.1 - 10.6 Ghz UWB Receivers”, IEEE Journal Of Solid State Circuits, Vol. 42, No. 2, February 2007.
[13] Yuch - Hua Yu, Yi – Jan Emery Chen, Deuknyoun Heo, “A 0.6V Low Power UWB CMOS LNA”, Article in IEEE Microwave and Wireless Components Letters 17 (3) : 229 – 271 April 2007.
[14] Kambiz Moez and M. I. Elmasry, “ A Low Noise CMOS Distributed Amplifier for Ultra Wide Band Applications”, Article In Circuits And System II: Express Briefs; IEEE Transaction on 55 (2) : 126 –130, March 2008.
[15] Zhe – Yang Huang, Che – Cheng Huang, Yeh – Tai Hung, “A CMOS Current Reused Low Noise Amplifier for Ultra Wideband Wireless Receiver”, Microwave and Millimeter Wave Technology, IEEE Explore, ICMMT -2008, vol.3.
[16] Joo, S. ; Choi, T.Y. and Jung, B. 2009. ‘A 2.4-GHz Resistive Feedback LNA in 0.13-µm CMOS’ IEEE Journal of Solid-State Circuits. 44: 3019-3029.
[17] Apisak Worapishet, Ittipat Roopkom, “Theory And Bandwidth Enhancement Of Cascaded Double –Stage Distributed Amplifiers”, Article In Circuits And System 1 : Regular Papers IEEE Transaction on 57 (4) : 759 – 772, May 2010.

[18] Brecht Machiels, Patrick Reynaert and Michiel Steyaert, "Power Efficient Distributed Low Noise Amplifier in 90nm CMOS", Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE.
[19] I - Chuan Chen and Jeng -Rern Yang, "3 -10 GHz CMOS Distributed Amplifier Low Power Low Noise and High Gain Low Noise Amplifier for UWB Systems", Article in TENCON 2010.
[20] Khurram, M. and Hasan, S.M.R, "A 3–5 GHz Current-Reuse g_m-Boosted CG LNA for Ultra wideband in 130 nm CMOS", IEEE Transaction on Very Large Scale Integration (VLSI) Systems. 20: 400-409.
[21] Jun Da Chen, "A Low Power Ultra Wide Band LNA in 0.18 μm CMOS Technology", Article in Active and Passive Electronic Components 2013: 1 -10.
[22] Shivani, Mr. Prashant Gupta, "An Extremely Low Power Consumption Operational Amplifier with High Phase Margin and Gain in 130nm Technology", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Vol. 2, Issue 11, November 2013.
[23] Sana Arshad and Rashad Ramzan. "A Sub 10mW Noise Cancelling Wideband LNA for UWB Application", Article In International Journal of Electronics and Communication, Aug 2014.
[24] Xiao – Peng, Wen Lin Xy, and Chen Feng, "A 11.2mW, 48 - 62 GHz LNA in 60nm CMOS Technology", Article in Circuits System and Signal Processing, Aug. 2015.
[25] Amir. Mahdavi and Fatemeh .Geran, "A Low power UWB CMOS Low Noise Amplifier for 3.1-10.6 GHz in Receivers", 8th International Symposium on Telecommunications (IST'2016), PP.567-600.
[26] Monsen Hayati, Sayad Cheraghali, "Design of UWB LNA using Noise Cancelling and Current Reused Technique", ICCCNT, 2017.
[27] S.Manjula, M.Malleshwari, and M.Suganthy, "Design of Low Power UWB CMOS Low Noise Amplifier using Active Inductor for WLAN Receiver", International Journal of Engineering & Technology, 7 (2.24) 448-452, 2018.
[28] Jiaqian Wu and Zhangfa Liu, "A 40nm CMOS Ultra-Wideband Low Noise Amplifier Design", Advances in Computer Science Research, International Conference on Wireless Communication, Network and Multimedia Engineering (WCNME 2019), vol.89.

TABLE-1: Comparison Table of Above Literature Survey

S.No.	Year	Topology	Frequency Range	Gain	Noise figure	Power Consumption
1.	2005 [8]	Cross Coupled G_m Boosting Topology	Maximum 6GHz	-	3dB	30mA current consumption
2	2007 [12]	Noise Cancellation Topology	3.1-10.6GHz	9.7dB	4.5-5.1dB	20mW
3	2008 [14]	Resistive Inductive Topology	Maximum 3GHz	12dB	3.3dB	30mW
4	2008 [15]	Current Reused Topology	3.1-12.2GHz	13.1dB	-	13.9mW
5	2010 [19]	Current Reused Topology	3-10GHz	-	3.4+0.36dB 3.4-0.36dB	14.8mW
6	2013 [21]	Source Degeneration Topology	3 GHz -7.5GHz	-	4.6-5.3dB	-

7	2016 [25]	Common Gate Cascode Topology	3.1GHz-10.6GHz	**22.1dB**	-	**1.3mW**
8	2017 [26]	Noise Cancellation, Current Reused, Source Degeneration And Resistive Feedback	3 GHz-12 GHz	-	**1.721dB**	23.23mW
9	2018 [27]	CMOS Active Inductor Topology	3.1GHz-10.6GHz	10.74+ 0.01dB	4.85dB	-
10	2019 [28]	Cascade Configuration With Resistive Feedback	**3.5GHz-31GHz**	-	Less than 4.5dB	-