High Speed Area Efficient Various Bits of QSD Addition / Subtraction using Reversible Logic gate

Asia Hasan[1], Prof. Nishi Pandey[2], Prof. Meha Shrivastava[3]

[1]*M. Tech. Scholar, Dept. of Electronics and Communication, TRUBA, Bhopal, India*
[2]*Assistant Professor, Dept. of Electronics and Communication, TRUBA, Bhopal, India*
[3]*Head of Dept., Dept. of Electronics and Communication, TRUBA, Bhopal, India*

Abstract- *Arithmetic Logic Unit plays a vital role in the central processing unit of the computer system. Addition is considered to be a primary part in the ALU. Power and speed are the major parameters to be kept in mind for designing an added. Because of carry propagation, complexity and delay gets introduced in the adder circuit due to which addition, subtraction and multiplication obtains delay in the Arithmetic Logic unit. In order to reduce the delay, carry-free addition is introduced by QSD (Quaternary Signed Digit) Numbers. In this paper, a fast QSD Addition and Subtraction circuit is designed by use of DPG Reversible Logic Gates.*

1. INTRODUCTION

In digital electronics, computers, arithmetic operations and signal processors play an important and significant role. It means that as soon as the addition and subtraction take place, the speed of the whole system increases. Standard binary systems can produce carry which spreads from the least significant digit to the most significant digit. Thus, the length of the binary number determines the time that is needed for addition. We are introducing the high-speed QSD arithmetic logic unit, which is capable of adding without carry and subtracting without borrow. The QSD addition/subtraction operation uses a fixed number of min terms for any size. The Computation time is reduced because in QSD number system, carry propagation chain is eliminated so that the speed of the machine is enhanced. Carry free addition is possible because of the Quaternary signed digit number system. QSD Adder/QSD Subtractor circuits are logical circuits that are designed to carry out arithmetic operations at high speed. The first step is the generation of intermediate carry and intermediate sum between the augends and addend. In the second step the intermediate sum of the current digit is combined with the carry of the lower significant digit, which enhances the speed of the machine [1].

The advancement in VLSI designs, portable device technologies and increasingly high computation requirements, lead to the circuit design of faster, smaller and more complex electronic systems at the expense of lots of heat dissipation which would reduce the life of the circuit. Thus power consumption becomes an important issue in modern design [2]. The power dissipation that is tolerable in a given application context is always limited by some practical consideration, such as a requirement that a limited supply of available energy (such as in a battery) not be used up within a given time, or by the limited rate of heat removal in one's cooling system, or by a limited operating budget available for buying energy. Thus, improving system performance generally requires increasing the average energy efficiency of useful operations. It has been unmistakably shown by Frank [3] that reversible figuring is the main feasible alternative to beat the force dispersal [4]. The essential inspiration for reversible registering lies in the way that it gives the main way (that is, the main way that is sensibly steady with the most immovably settled standards of central material science) that execution on most applications inside practical force imperatives may at present keep expanding uncertainly. Reversible logic is also a core part of the quantum circuit model.

2. REVERSIBLE GATE

Reversible rationale is picking up significance in zones of CMOS configuration on account of its low power dissemination. The customary entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Thus, one piece is lost every time a calculation is completed Hence it is impractical to decide a remarkable information that brought about the yield zero. With a specific end goal to make an entryway reversible extra information and yield lines are added so that a coordinated mapping exists between the info and yield. This keeps the loss of data that is fundamental driver of force dispersal in irreversible circuits. The information that is added to a m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit. Those yields that are not utilized as a part of the circuit is called as junk yield (GO). The quantity of trash yield for a specific reversible door is not altered.

The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DPG gate produces the following logical output
calculations:

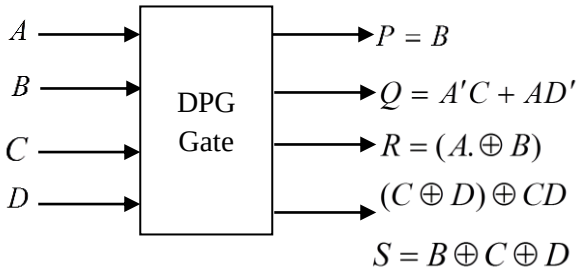


Figure 1: DKG Gate

$$P = B \quad (1)$$

$$Q = A'C + AD' \quad (2)$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \quad (3)$$

$$S = B \oplus C \oplus D \quad (4)$$

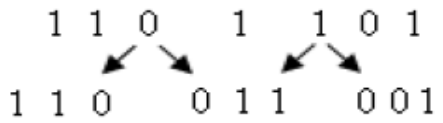
3. PROPOSED DESIGN

QSD NUMBER

1-digit QSD can be represented by one 3-bit binary equivalent as follows:

-3 = 101
-2 = 110
-1 = 111
0 = 000
1 = 001
2 = 010
3 = 011

So to convert *n*-bit binary data to its equivalent *q*-digit QSD data, we have to convert this *n*-bit binary data into *3q*-bit binary data. To achieve the target, we have to split the 3rd, 5th, 7th bit…. i.e. odd bit (from the LSB to MSB) into two portions. But we cannot split the MSB. If the odd bit is 1 then, it is split into 1 & 0 and if it is 0 then, it is split into 0 & 0. An example makes it clear, the splitting technique of a binary number $(1101101)_2$ are shown below:



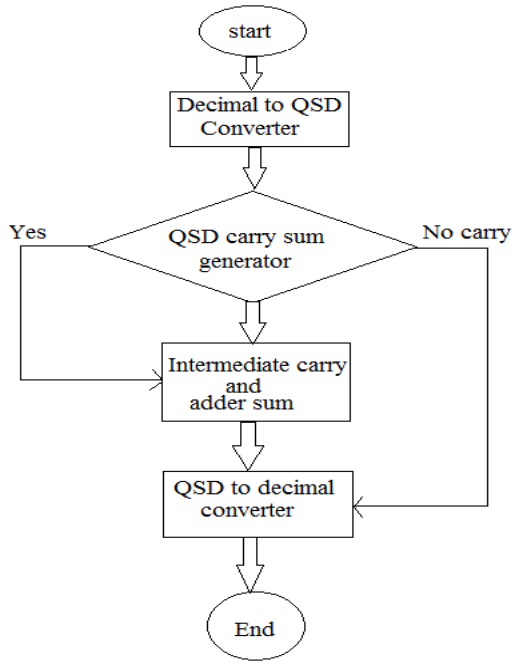


Figure 2: Flow Chart of Proposed Methodology

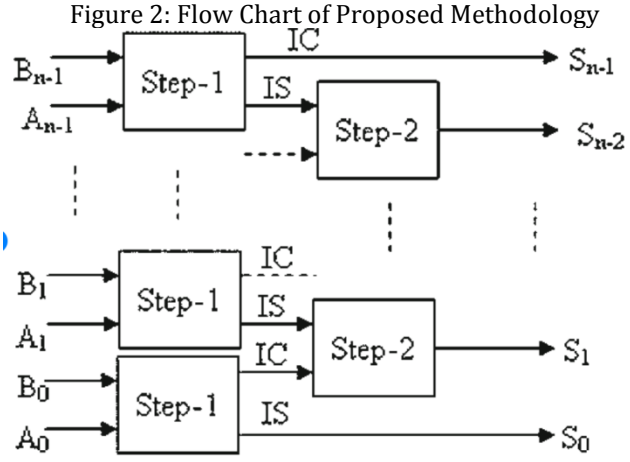


Figure 3: lock diagram of n-digit QSD carry free adder circuit

So we have to split the binary data (1)$q-$ times (as example, for conversion of 2-bit quaternary number, the splitting is 1 time; for converting 3-digit quaternary number the split is 2-times and so on). In each such splitting one extra bit is generated. So, the required binary bits for conversion to its QSD equivalent (n) = (Total numbers of bits generated after divisions) – (extra bit generated due to splitting).

Table 1: Binary representation of Quaternary signed digit numbers

Serial Number	Quaternary signed digit	Binary Representation
1	-3	101
2	-2	110
3	-1	111
4	0	000
5	+1	001
6	+2	010
7	+3	011

4. EVALUTION PARAMETERS

Garbage Output
Unused output or extra output is not used to circuit is called garbage output.
Constant Input
The constant inputs either '0' or '1' defined in the input are known as ancilla input or constant input.
Number 4-input LUTs
LUT stands for look up table that reduces the complex mathematics calculations and provide the reduced processing time.
Number of Slices
How many areas are used in this circuit is called number of slices.
Number of IOBs
All input output port used in this circuit are combined called number of input output buffer switch.
Maximum Combinational Path Delay
Maximum delay for signal propagation is called the maximum combinational path delay.

5. SIMULATION RESULT

More specifically, we have developed new garbage-free circuits for addition and are working towards a general multiplication circuit. We have also combined multiple operations together to implement a reversible arithmetic logic unit. With these and other garbage-free arithmetic circuits it is possible to design larger reversible computing systems. As an example, we have implemented discrete lossless transforms by redesigning these with a lifting scheme. We have also shown the design of a reversible computing architecture and implemented this using only reversible logic gates. While, these are still small systems, with further development it should be possible to use similar strategies to implement even larger systems.

Table 2: Comparative Results of Existing Algorithm and Proposed Algorithm in 4-bit Adder/ Sub-tractor

Parameter	Existing Adder/ Sub-tractor [1]	Proposed Reversible Adder/ Sub-tractor
No. of Gates	44	40
Garbage Output (GO)	8	8
Quantum Cost	28	24

Figure 4: Bar Graph of the Previous and Proposed Reversible Full Adder

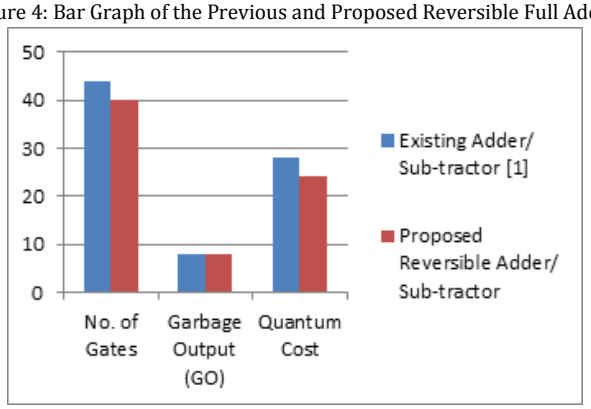


Table 3: Comparative Results of Existing Algorithm and Proposed Algorithm in 8-bit Adder Sub-tractor

Parameter	Existing Adder/ Sub-tractor [1]	Proposed Reversible Adder/ Sub-tractor
No. of Gates	88	80
Garbage Output (GO)	16	16
Quantum Cost	56	48

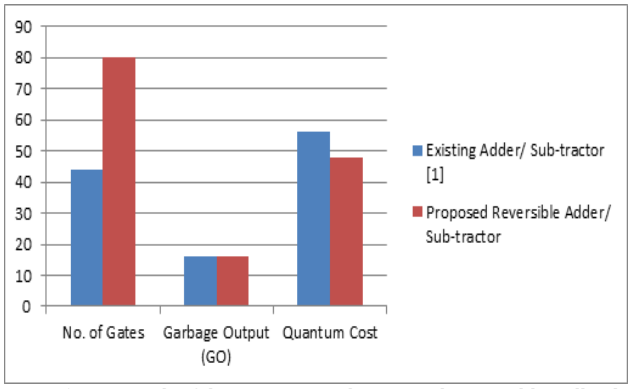


Figure 5: Bar Graph of the Previous and Proposed Reversible Full Sub-tractor

Table 4: Comparative Results for higher bits

Parameters	No. of Gates	GO	QC
16-bit	160	32	96
32-bit	320	64	192
64-bit	640	128	384
128-bit	1280	256	768

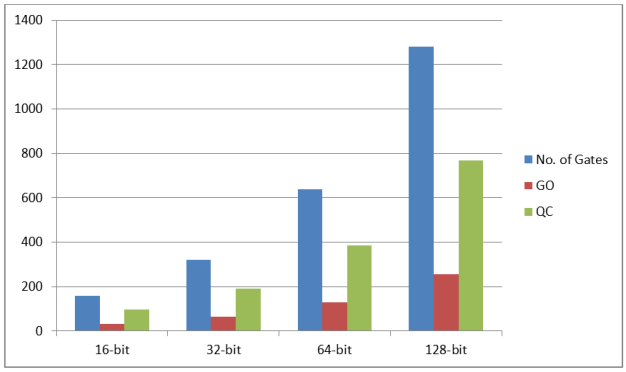


Figure 6: Bar Graph of the Proposed Reversible Full adder and Full Subtractor

6. CONCLUSION

Reversible logic may be a promising computing design paradigm that presents a technique for constructing computers that produce no heat dissipation. Reversible computing emerged as results of the applying of quantum physics principles towards the event of a universal computing device [1]. Specifically, the basics of reversible computing area unit supported the link between entropy, heat transfer between molecules in an exceedingly system, the chance of a quantum particle occupying a specific state at any given time, and the quantum electrodynamics between electrons once they are in close proximity. The basic principle of reversible computing is that a bijective device with an identical number of input and output lines can produce a computing setting wherever the electrodynamics of the system provide calculation of all future states based on best-known past states, and also the system reaches each attainable state, leading to no heat dissipation [2].

REFERENCES

[1] Simranjeet Singh Sudan and Manish Singhal, "MIG and COG Reversible Logic gate Based QSD Addition / Subtraction", International Conference on Computing, Communication and Automation (ICCCA2017).

[2] Radhika Thakur, Shruti Jain and Meenakshi Sood, FPGA Implementation of Unsiged Multiplier Circuit based on Quaternary Signed Digit Number System", IEEE Conference on Signal Processing, Computing and Control, IEEE 2017.

[3] Purva Agarwal and Pawan Whig, "Low Delay Based 4 Bit QSD Adder / Subtraction Number System by Reversible Logic Gate", 2016 8th International Conference on Computational Intelligence and Communication Networks.

[4] Ameya N. Bankar, Shweta Hajare, "Design of Arithmetic Circuit Using Quaternary Signed Digit Number System", International Conference on Communication and Signal Processing, April 3-5, 2014, India.

[5] Tanay Chattopadhyay and Tamal Sarkar, "Logical Design of Quaternary Signed Digit Conversion Circuit and its Effectuation using Operational Amplifier", Bonfring International Journal of Power Systems and Integrated Circuits, Vol. 2, No. 3, December 2012.

[6] Krishna Murthy, Gayatri G, Manoj Kumar "Design of Efficient Adder Circuits Using Proposed Parity Preserving Gate" VLSICS Vol.3, No.3, June 2012.

[7] M. D. Saiful Islam and Z. Begum, Reversible Logic Synthesis Of Fault Tolerant Carry Skip BCD Adder, Journal of Bangladesh Academy of Sciences, Vol. 32, No. 2, 193-200, 2008.

[8] M. K. Thomsen, R. Gluck, H. B. Axelsen, 2010, Reversible arithmetic logic unit for quantum arithmetic, Journal of physics A: Mathematical and Theoretical, 43 (2010) 382002 (10pp), doi: 10.1088/1751- 8113/43/38/382002.

[9] M. Haghparast, K. Navi, 2008: A Novel Fault Tolerant Reversible Gate For Nanotechnology Based Systems, Am. J. Applied Sci., 5(5), 519-523.

[10] B. Parhami, Fault Tolerant Reversible Circuits, Proc. Asilomar Conf. Signals, Systems, and Computers, Pacific Grove, CA,Oct.2006.

[11] Haghparast, M. and K. Navi, " A novel fault tolerant reversible gate for nanotechnology based systems". Am. J. Appl. Sci., 5(5).2008.

[12] Jayashree H V and Ashwin S, "Berger Check and Fault Tolerant Reversible Arithmetic Component Design", 978-1- 4799 - 8364-3/ 15/ $31.00 @ 2015 IEEE.

.