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Network on Chip with Tunable Datarate

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Abstract – *A Network on chip is the best interconnect solution for today's and future System-on-chip, as it reduces the complexity involved in designing the wires and also provides a well-controlled structure. The NOC interconnect provides a standardized way to add or replace various processing elements to the SOC design. Also, in complex SoC's, it may be desired to establish individual clock frequencies for the interconnection which aims to optimize power dissipation. In this paper, the proposed system contains a fifo module, decoder module, kogge stone adder module, analog-to-digital converter module and digital phase lock loop module which act as an applications in each node and the modules are interconnected using priority algorithm, also the architecture provides tunable frequency for different configurations. The software used to perform the simulations is Xilinx ISE.*

Key Words: Network-on-chip, Fpga, Xilinx ISE, Fifo, Dpll, Adc, Kogge stone adder, System on chip.

1. INTRODUCTION

Network on Chip provides communication between operating modules located on the same chip. The goal is to combine computing cores of varying purposes like for example device controllers, ROM and RAM modules, stand-alone devices, sensors, dsp and much more that can be placed on a single chip. This interconnect technology is used to implement the communication features of large-scale to very large-scale integration systems. For high-end system-on-chip designs, network on chip is preferred as it reduces the complexity involved in designing the wires and also provides a well controlled structure capable of better power, speed and reliability due to these advantages it is considered to be the best integrated solution. It can also be seen in a way which can integrate high number of computational and storage blocks in one single chip. As there is a demand to increase the density design of very large scale integration circuits this gives rise to the complexity of each component in a system which in turn results in increasing transistor density, higher frequencies and shorter time-to-market pressure. Recently, there is a greater need for Multiprocessor system on chip (MPSoC) and chip multiprocessor (CMP) architectures but these uses bus structures for on-chip communication and integrate complex heterogeneous functional elements on a single chip. With the increasing number of processing elements the soc designer's face a lot of challenges to design on chip interconnection. The disadvantage of traditional bus-based communication is the lack for scalability, predictability and they are not capable to keep up with the increasing requirements of the present and future SoC's in terms of power, performance, timing closure, and scalability. Thus, to meet the requirements of the challenges of next-generation system designs a network on chip has been developed recently to mitigate the complex on-chip communication problem. Since more number of processors and cores are integrated in Mp-soc and CMP architectures which demands for low latency, high throughput and reliable global communications. These demands cannot be met by current dedicated bus based on-chip communication infrastructure. The problems faced while trying to achieve such latest process technology designs with a bus structure results in number of issues including timing closure, performance degradation and scalability. There is a delay in the global interconnection speed specially when the feature size of modern silicon devices shrinks below 55 nanometers. Network on chip is a new methodology that has been developed to solve these issues by introducing a structured and scalable communication architecture.

2. RELATED WORK

The proposed NoC architecture named RingNet stands out with communication through a central memory and traffic load controlled by the recipient. Optimal utilization of FPGA resources is one of the goals of RingNet development. Especially, buffers are implemented in distributed RAM available in FPGAs, and the virtual cut-through is used as an efficient switching technique for FPGA [1]. To improve energy-efficiency and fault tolerance capability of NoC router by leveraging channel slicing. The proposed system is designed to realistically estimate a design's peak power consumption, which directly impacts other salient system attributes, such as performance, implementation costs, battery life, and reliability. Therefore, introducing a fully automated high-level methodology to generate appropriate traffic and data patterns that cause peak power consumption within the NoC [2]. As technology scales, energy-efficiency and fault-tolerance have become two key concerns for NoC design. The proposed router has three identical router slices connected with internal sharing path. This method can diagnose and repair both control and datapath faults without suspending normal operations [3]. On-chip interconnects used in NoC applications must deliver high bandwidth with low communication latency and high power efficiency. Because of the bursty traffic, the utilization of these on-chip interconnects varies with application. Therefore, it is paramount to maintain excellent power efficiency across all utilization levels. However, the power efficiency of

conventional interconnects severely degrades at low utilization levels, because they consume large power even when they are idle. Thus the presented techniques implements power efficient transceivers for on-chip interconnects that can eliminate idle power almost entirely, thus achieving energy proportional operation [4]. A routing algorithm tailored to partially connected 3D-NoCs is proposed. Compared to the previous work, simulations show that the proposed algorithm provides lower latency, higher saturation point and better temperature distribution under a variety of traffic patterns and TSV configurations [5]. The proposed system is based on comb switches. TAONoC adopts a regular torus topology to accommodate the layout of a tile-based chip multicore processor. Depending on the unique designs of the three function modules, TAONoC can support contention-free communication without the need for arbitration [6]. An integrated run-time solution for both security and fault tolerance of field-programmable gate arrays (FPGA)-based SoCs through digital signatures, live monitoring, adaptive routing, and partial 6 reconfiguration supported by an in-house-developed network on chip, X-Network. The proposed X-Network reduces the ratio of required routers versus processing elements with better performance, and more importantly, offers more flexibility than conventional networks to facilitate fault tolerance and security designs [7]. For design space exploration and finding the best NoC solution for each specific application, a fast and flexible NoC simulator is necessary, especially for large design spaces. The proposed system contains an FPGA-based NoC co-simulator, which is able to be configured via software. It implements a two-layer configurable global interconnection in the proposed architecture [8].

3. PROPOSED SYSTEM

This paper work aims to provide a interconnect technology which connects the modules on a system-on-chip using priority algorithm and also improve the performance of processing elements when deal with multiple clock for inter domain translations. Consider a SoC, in which there are many components for examples say, dac, adc, fft etc these components are represented as individual modules and these modules are interconnected using a network based communication. Also, the proposed system enables the frequency for different configuration to be tuned according to the user's requirement. Figure 1 illustrates the overall block diagram of how the network on chip with tunable datarate works. The design consists of submodules which are later integrated to form one system. These submodules are clock tree synthesis, lut configuration, node configuration. The architecture consists of five nodes to be interconnected they are analog-to-digital converter, kogge stone adder, digital phase lock loop, decoder, first-in, first-out. The clock tree synthesis diagram is shown in figure 2. This module generates a range of clocks from a global clock. By designing clock synthesis the frequency can be tuned for the different configuration. It consists of a synchronous counter which increments the clock and a clock divider which divides the clock into multiple clocks. The gate decoder is used to stop or reset the clock. Here, d-latch is used which holds or release the clock and it is given to a trigger pulse and the process continues till multiple clocks are obtained from a reference clock. The Look up table configuration provides a predefined data of conditions to control the nodes and clocks. It is used to initialize the setting of nodes and clocks. In this the processing elements are packed in such a way it can encapsulate all the information in one data packet under configuration settings. The node configuration consists of N number of nodes which acts as a separate digital modules and the connection of each node depends on the priority based algorithm. To add a node or to replace a node depends on their priority value. The priority value represents the values given to the node based on their priority of requirement. The priority based algorithm is as follows

ALGORITHM:
STEP 1: Consider the value of priority
STEP 2: Check if priority value is high
STEP 3: Then connect to the load with high priority
STEP 4: Create node name and transfer data
STEP 5: Display the node

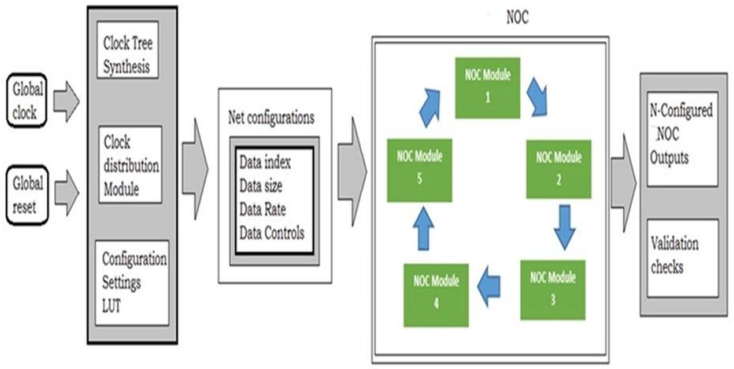

Fig -1: Block diagram of NOC with tunable datarate

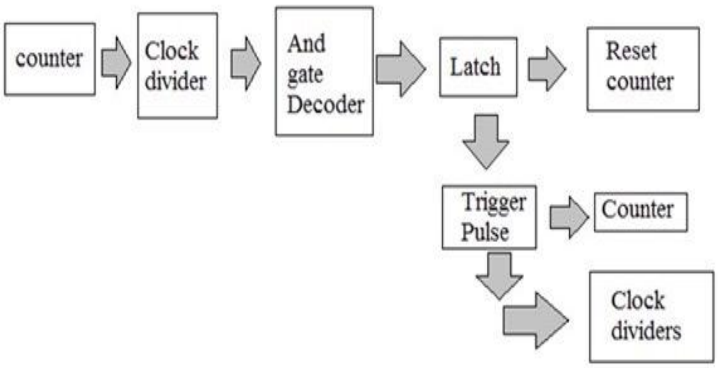

Fig -2: Clock tree synthesis

The integration is the final step in which all the sub modules are integrated as one under a configuration setting. It acts as

a finite state machine model which connects all the submodules in the design and maintain the synchronization and avoids unwanted clock jitters which disturb the flow.

4. EXPERIMENTAL RESULTS

The network on chip with tunable datarate architecture consists of five digital modules to be connected. These modules can be added or replaced depending on their priority values. These five modules are kogge stone adder, analog-to-digital converter, digital phase lock loop, seven segment decoder, fifo. The simulation results in figure 3 represents kogge stone adder. It is one of the fastest adder in which propagate and generate bit is produced in each vertical stage. Using the below formula the output sum is obtained.

Gi = Ai and Bi;
Pi = Ai xor Bi;
Si = Pi xor Ci-1;

In the figure 4 the simulation result represented is a 4-bit analog-to-digital converter, which represents a analog signal, sampled signal, quantized signal and digital code. Thus, it converts a analog signal to a digital signal. The figure 5 represents digital phase lock loop which shows the input clock is synchronized with the reference clock. It consists of a phase detector, loop filter and digital control oscillator. The phase detector compares the reference frequency and input frequency and detects error. The loop filter is used to remove noise here, low pass filter is used. The digital control oscillator adjusts the frequency that is it increments or decrements the frequency to get the synchronized output. The simulation results in the figure 6 represents seven segment decoder in which the seven segment display is represented by its equivalent binary values. The simulation result in the figure 7 represents FIFO where the data is written and read using the signals fifo full, read enable, write full, read data etc. It acts as a memory buffer. It is a synchronous fifo because it uses the same clock to write and read the data. The figure 8 represents the network-on-chip with tunable datarate architecture, with the integration of the five modules, clock tree synthesis, node configuration, look up table configuration. It represents the overall output of the architecture and how the nodes are connected in a SoC. The simulation also shows how the frequency can be tuned for different configuration setting. For each configuration say 0001, 0010.....1111 there are different ranges of clocks representing different frequency for each configuration and also for each configuration the priority values are given. If the priority value is high then the next node will be connected if not it will be disconnected. The clock divided for each configuration is based on two's multiple like 2, 4, 8..etc. In this way communication between operating modules are provided and the processing elements can be added or replaced and also the frequency is tunable according to user's requirement. The programming language used to implement this architecture is vhdl. This architecture helps to optimize the power dissipation by tuning the frequency.

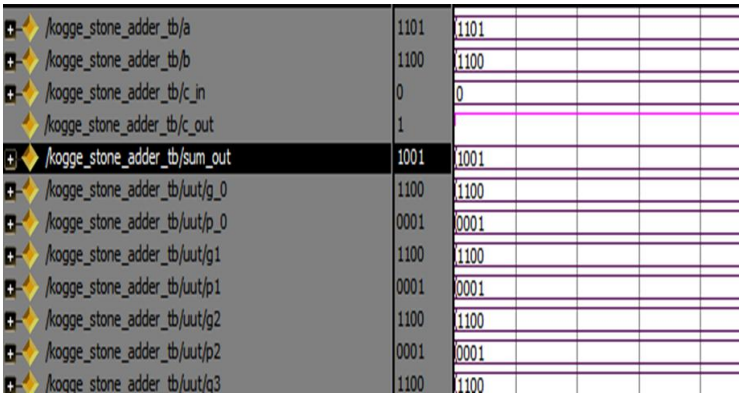

Fig -3: Simulation result of Kogge stone adder

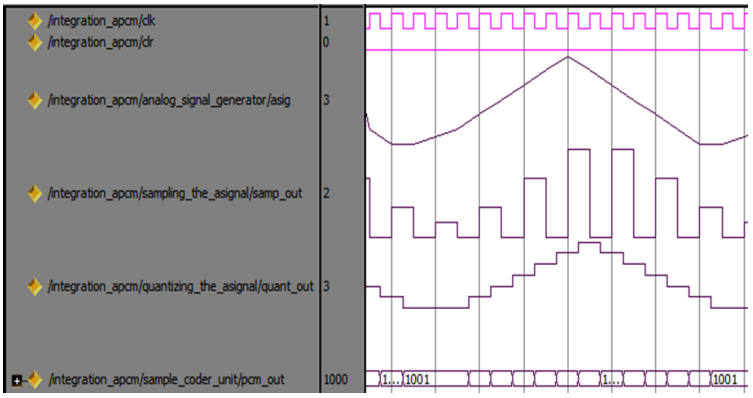

Fig -4: Simulation result of analog to digital converter

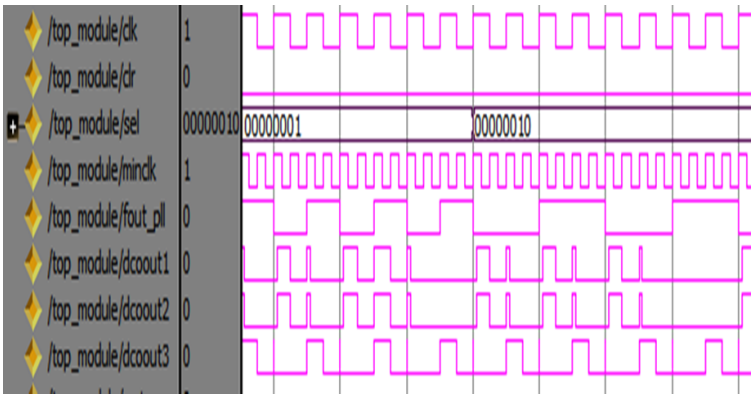

Fig -5: Simulation result of digital phase lock loop

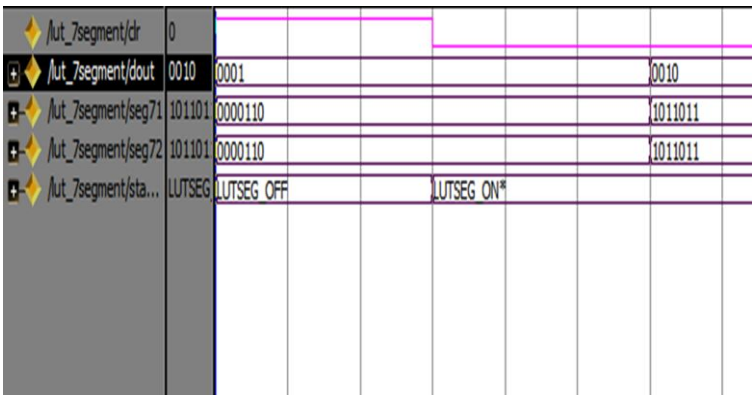

Fig -6: Simulation result of seven segment decoder

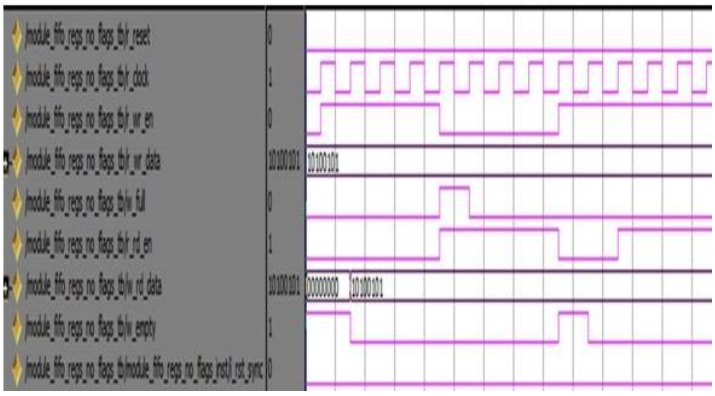

Fig -7: Simulation result of fifo

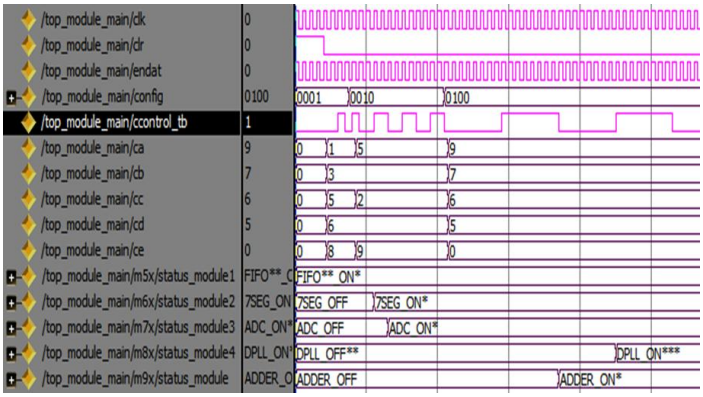

Fig -8: Simulation result of noc with tunable datarate

5. CONCLUSIONS

In complex SOC's, it is desired to use tunable frequency for the different configuration. The NoC with tunable datarate is used to improve the performance of processing elements when deal with multiple clock for inter domain translations. The frequency for different configurations can be tuned according to the user's requirement. The simulation result shows that the modules are interconnected and the clock frequency is tunable which aims to optimize power. Thus, Network on chip interconnect reduces the wire routing congestion on chip and it is a standardized way to add or replace various processing elements to the SOC design. The extension of the work will focus on developing the architecture into a MpSoc platform and can be implemented in a Xilinx FPGA for further validation.

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