Design and Implementation of CMOS and CNT based 2:1 Multiplexer at 32nm Technology

Anjum Aara[1], Sushant Jain[2]

[1]PG scholar, Department of Electronics & Communication Engineering, ITM Gwalior

[2]Assistant Professor, Department of Electronics & Communication Engineering, ITM Gwalior

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Abstract- *Carbon nano tube transistor is a narrative nanotechnology that pledge extra low-power, immensely murky and high speed composition for formation of logical design at a nano-scale. Multiplexer is a convenient module for the design of several dominant circuits. This article proposes a narrative and efficient module of 2:1 multiplexer. Comparison of these outcomes to be illustrates in significant enhancements in our module as compared to traditional technology. So, in this article we analysis the outcomes of CNT & CMOS based 2:1 multiplexer. After comparison we found that CNT have many advantages over CMOS. So, we prefer CNT over CMOS for further research and will apply more technique on CNT based Schmitt trigger to analysis the improvements. This simulation is complete on SPICE tool, which is widely worn in VLSI field.*

Keywords: CNT, multiplexer 2:1, CMOS, power consumption, SPICE.

1. Introduction

In the recent years, carbon nano tubes have been seeking the attention of the researchers as it exhibits efficient implementation potential in several current and emerging technologies, the dimensions of the CNT are also small as well as the morphologies are also unique. The structure of CNT is formed via graphite. There are three forms in which the graphite can be formed in a nano scale they are: Carbon nano balls, Carbon nano coil and carbon nano tubes. The carbon nano balls are also familiar as the bulky balls embracing of the atoms consisting 60 carbon molecules which are exhibited in the mould of soccer ball. Then the second form is they are found in the form of carbon nano tubes, these are narrow strips of tiny sheets which are made up of graphite which are discovered in further two forms first is the multi wall CNT comprising of various hollow carbon atom cylinders which are entwined with each other, second is a single walled CNT which is just made up of a single carbon atoms layer and the third form is the coil form of CNT. CNT is a graphite sheet which is cylindrical in nature, geometrically it is found in two different forms, they are Straight CNT and Twisted CNT. The CNT which is formed straight are further rolled into the tubular forms as they are cut straightly and the twisted CNT, they are cut at a particular angle from the sheet of graphite and then further rolled into the tubes [1-4].

This CNTFET is considered as one of the strong and emerging technologies which are capable of replacing the existing CMOS technology. The prime concept leading to the article of CNT was Moore's law stating "that as the per device transistor numbers are expanding and are getting double each year, their size is diminishing". To function according to the existing Moore's law, the CMOS automation undergone the diminishing in size with the propagation delay cost getting raised and the consumption of power enhanced depicting the more merged power delay product form. The propagation delay of CNTFET was found to be excessively low as compared to CMOS. The dissipation of the power was also found to be low as well as the power delay products also reduced as this was directly affected by power dissipation. They exhibited more benefits because of the reduced sizes [5].

Multiplexers are those devices converting 2n number of inputs into one single output, which means that the inputs are multiple but the output is single. In the aforementioned 2n, n stands for the select pin which determines and decides that which pin will input first and which pin will input later. The meaning of the 2:1 multiplexer is that they are designed in such a way, so that they acknowledge and decide amongst the two pins which input pin will reach the output first. Demultiplexers are those appliances which have one input and the output of such are 2n, here also the n posture for prefer pin numbers governing that amid which of the output lines the transmittance of the input will be forgotten first. The task of the magnitude comparators is contrasting the two magnitudes of two binary numbers. In this a 2 bit magnitude comparators were depict which give outcomes in three different kind of outputs which are based on equal, greater than and less than comparisons [5].

Multiplexer is sometime known as data selector. A multiplexer is a connective structure that prefers binary information from one to several input lines and manages it to a single output line. The 2:1 multiplexer module has one output, two inputs and one selection input. The selection of specific input line is managed through a group of selection lines. The selection line resolute which of the input bit is transmitted to the output [2].
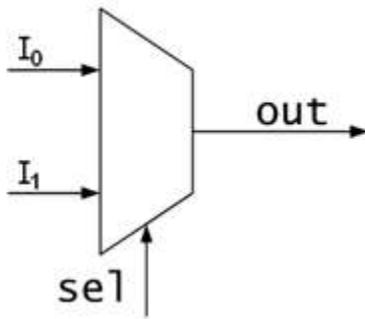
Figure1: 2:1 multiplexer

2. Literature review

Mishra et.al in 2014 stated various analysis which were performed and established mainly on the basis of the arithmetic circuits mainly dependent over the MUX design. The power is optimized and explored using the multiplexer. The new 4:1 MUX is construct to operate the CMOS transmission gate logic (TGL) diminihing the complexity of the module as compared to the conventional CMOS which is based on the construct of the multiplexer. The decreased or the degraded output was removed which was based on the TGL. Further, for obtaining strong output level the PMOS and NMOS were mixed together gaining the area, this gain in the area was accomplished using the results of this proposed MUX. This model was designed to operate 45 nm technology with the power consumption of 1.88nW suing the power supply of 0.7V. They indicated that the till the 200 Gb/s, MUX could be easily operated [6].

Zean et.al in 2017 stated the recent researches of CNTFET which is based on the digital circuits whose performance results obtained were better as a replacement for current which was possible for the existing circuits of CMOS digital logic. The authors used CNTFET 32nm and were performed using the H SPICE model. This model is based on the custom 4:1 Multiplexer and 1:4 Demultiplexer along with the designing of the 2 bit enormity comparators were analyzed with PTM CMOS 32 nm through HSPICE model which was designed with full custom 4:1 multiplexer, 1:4 demultiplexer and 2 magnitude comparators regarding the product of the power delay. From the results and analysis simulations, the results obtained by the author were 92%, 82% and 93% respectively with the CNTFET based on 4:1 Multiplexer and 1:4 Demultiplexers along with the designing of the 2 bit enormity comparators. The values and the percentages obtained exhibited less PDP when compared to PTM; CMOS based 4:1 Multiplexer and 1:4 Demultiplexers along with the designing of the 2 bit magnitude comparators respectively [5].

3. Circuit description

A multiplexer is a connective model which collect binary inputs from one to 2N input lines and it manages these inputs to single outputs. The selection of a specific input data line to the output is manifest by a group of selection inputs. The multiplexer or MUX is sometimes known as data selector, because it prefers one of the numerous input data lines and steers the binary information to the output of multiplexer.
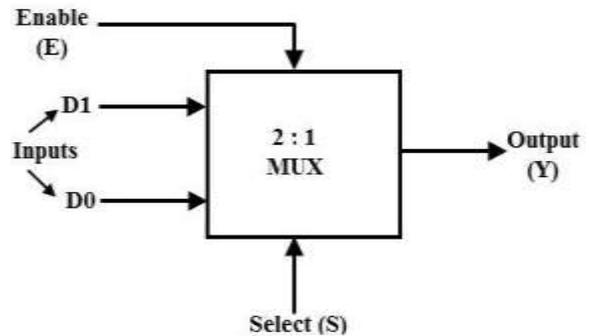

Figure 2: Block Diagram of Multiplexer

A 2x1 multiplexer having two inputs i.e. D1 and D0, one selection input S, one enable clock pulse E and one output line Y. As we can see there does one prefer inputs therefore, they can have only two achievable combination starting from 0 and 1. When selection input is 0 then input line 'D1' is preferred and is directed to the output. Similarly, when selection input is 1 then input line 'D0' is preferred and is directed to the output Y for their combination of these selections input. Its block diagram, truth table and circuit diagram is illustrative below. The output equation of the 2x1 multiplexer is given

$$Y = D1\bar{S} + D0S$$

The expression and truth table of a 2x1 multiplexer is as given

$$Y = D1\bar{S} + D0S$$

Selection line	Output
S	$Y = D1\bar{S} + D0S$
0	D1
1	D0

Truth Table of 2x1 Multiplexer

3.1 CMOS based 2*1 Multiplexer

2x1 Multiplexer can be build by CMOS as illustrate in figure 2. CMOS based 2x1 Multiplexer build up of two section first one is pull up lattice and other one is pull down lattice. Pull up lattice mainly known as PMOS and

pull down is NMOS. In this model PMOS device is connected to the supply voltage (VDD) and NMOS appliances is also connected with ground (GND) to the circuit.
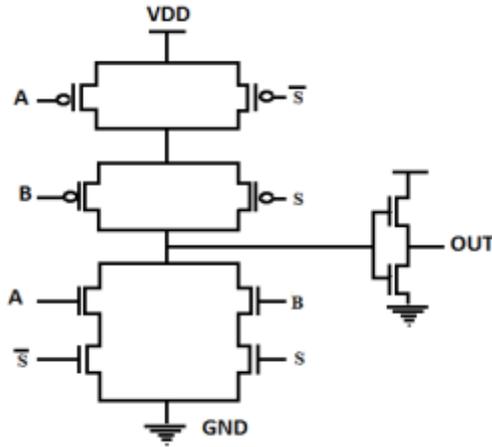

Figure 3: CMOS based 2x1 Multiplexer

3.2 Circuit Description of CNT based 2x1 multiplexer

There is lot of drawback in CMOS based transistor to overcome these drawbacks through CNT transistor in this paper. This type of transistor is cylindrical form whose length (L) and width (W) dimension is 32nm. Working concept of both MOSFET and CNTFET technology can operate in 32nm. The schematic design of 2x1 multiplexer using CNT based transistor as shown in figure 3.
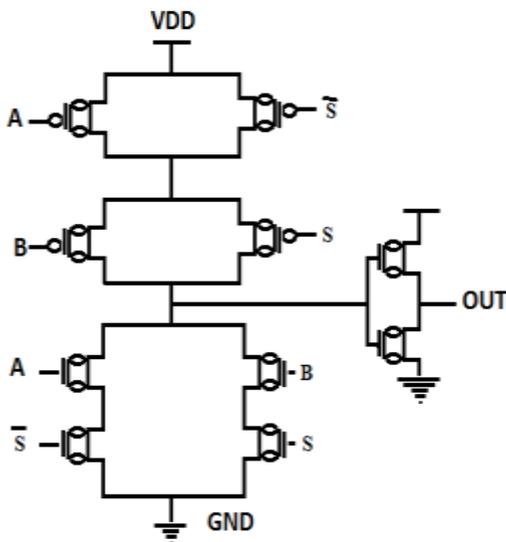

Figure 4: CNT based 2x1 Multiplexer

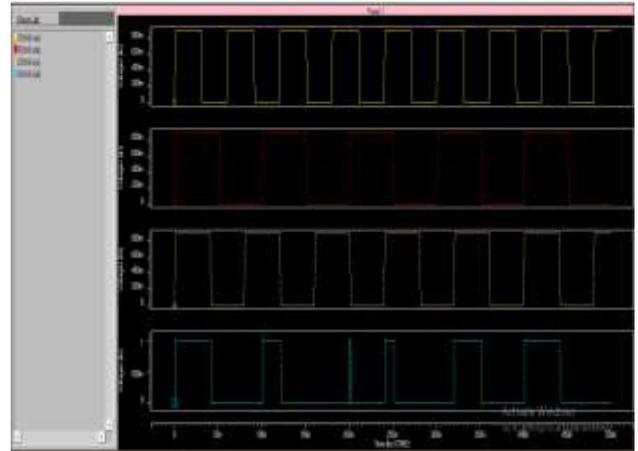## 4. Simulation Results and Discussions

Figure 5: Waveform of CMOS based 2x1 Multiplexer

The waveform of 2x1 Multiplexer in CMOS and CNT based transistor to operate in 32nm technology. Both CMOS and CNT based multiplexer to be simulated by SPICE simulation tool. The simulated waveform of CMOS based 2x1 multiplexer as illustrate in figure 4.

Simulated waveform of 2x1 Multiplexer is operate through CNTFET technology to provide noise immunity of signal is improved and power dissipation loss to be diminished in contrast of CMOS technology as clearly seen in figure 5.
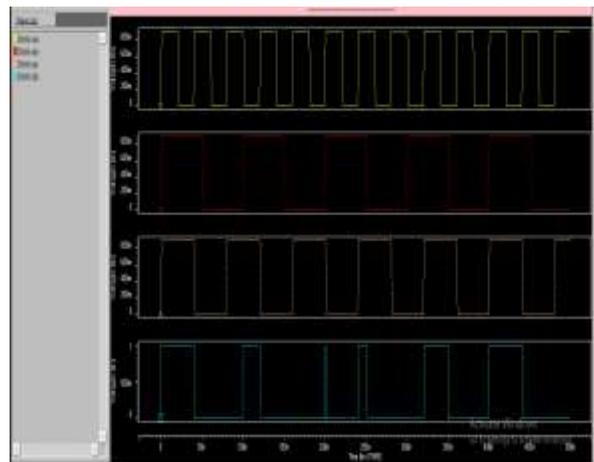

Figure 6: Waveform of 2x1 Multiplexer is operate CNTFET technology

Power dissipation: Power dissipation mechanism is classified into two classes:

     A. Static power dissipation and Dynamic power dissipation

When circuit is in active state Dynamic power consumption occurs, i.e. some work perform on data.

- due to load capacitances charging and discharging
- When both PMOS and NMOS are moderately on

B. Static power consumption occurs when the model is in off state or in a power-down mode.
- Sub threshold transmission through down mode transistors.
- Tunneling current passes gate oxide
- Leakage current in reverse-biased diodes

$P_{total} = P_{static} + P_{dynamic}$ .... (1)

$P_{dynamic} = 1/2 \ (CL*VDD2 *fc)$........(2)

$P_{static} = Ioff* VDD$.....................(3)

Where,

CL= load capacitance

VDD=Power supply

fc= Clock frequency

Ioff =leakage current drawn by each switch in off state

The following table displays the comparative study between CMOS based multiplexer design and the CNT based multiplexer design.

Performance parameters	Multiplexer based CMOS	Multiplexer based CNT
Technology	32nm	32nm
Supply voltage	1v	1v
Average power	6.83nW	6.40nW
Leakage power	504.218pW	319.20pW
Leakage current	504.218pA	319.20pA
Delay	40.86ns	40.84ns

Table 1 illustrates the simulation outcomes of 2x1 Multiplexer. In CMOS based 2x1 multiplexer leakage power is 504.218pW and delay is 40.86nS is to be determined with the help of SPICE simulation tools. CNTFET based 2x1 multiplexer leakage power was diminished to 319.20pW and delay is reduced to 40.84nS at 1V power Supply. Graphical representation of all Parameter was determined in both CMOS and CNTFET as illustrate in Figure.
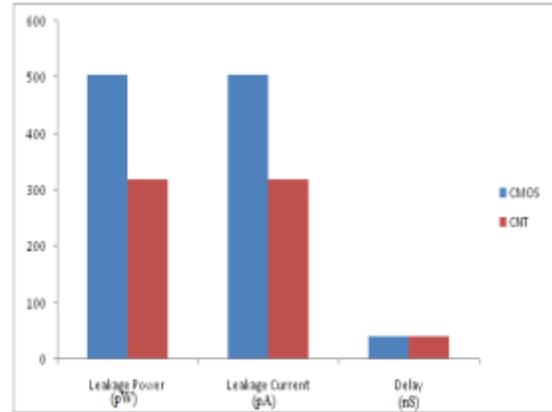

Figure 7: Graphical Representation of Various Parameter of 2:1 Multiplexer

5. Conclusion

In this paper to compare both CMOS and CNT transistors at 32nm technology in 2x1 Multiplexer design for performance parameters like the power consumption, delay, leakage current etc. The complete circuit work of 2x1 Multiplexer is performed on the SPICE Tool for both CMOS and CNT transistors. The results of CNTFET based 2x1 Multiplexer reduces the power consumption is 57.99 % over CMOS based technology. From the inferences made the idea of the research have been integrated through the CNT based transistors concept gives more efficiency than the CMOS based transistors technology because the planned Latch are designed victimization 2x1 Multiplexer arrangement such the physical phenomenon property is used to induce higher performance against clanging input signals.

6. References

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