Broadcasting Test Patterns to Integrated Circuit via Single Bidirectional Data Line

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Abstract - *During the last few years, engineers made efforts to improve testing methods of the integrated circuits (ICs). Classical testing methods encounter a significant increase in testing cost because of the complexity of testers design. Moreover, diagnosing ICs usually result in long test time. In this paper, we present a new approach testing design based on a single bidirectional data line instead of multi data lines. The test patterns will be broadcasted serially through a single data line and the corresponding response patterns will use the same line. The proposed technique reduces the number of test pins to one. Shift registers and switching circuits are to be placed and incorporated into the device under test (DUT). It will be used to distribute the test patterns parallel to test pins. Also, the embedded circuits are utilized to control the data flow over the single data line. The main advantage of using single data line is lower complexity and higher functionality. The proposed method is simulated using National Instruments Multisim Simulator.*

Key Words: Integrated circuit testing, bidirectional data line, higher functionality, test access port

1. INTRODUCTION

The incredible shrinking of printed circuit boards and system on chips (SOCs) lead to miniaturization resulting in loss of test access. Also, the ever-expanding chip and the increasing integration at chip level complicate controllability[1]. Moreover, cost will increase by a factor of ten as fault finding moves from one level of complexity to the next. This cause a reduced profit margins, delayed product introduction and dissatisfied customers [2]. The conventional methods of test such as Functional Test (Edge-Connector Test) were imposed by hard-wired copper interconnects which encounter limitations and impede the advance of future testers[3, 4]. It is based on board function, rather than structure. In the traditional testing methods, the test generation was manual and the test access is limited to primary I/O only. In-Circuit Test (ICT) (Bed-of-Nails Test) which is based on board structure also limited by chip complexity[5]. It requires expensive testers and fixtures. Also the test access limited by fine pitch packages, double-sided boards, conformal coating and multi chip modules (MCMs). In such tests chip function can be ignored for shorts testing and must be considered for continuity test. Test generation though automated and requires ICT models [6, 7]. The performance of testers depends basically on the device properties. To enhance the tester performance, the efforts should be focused on improving the tester speed through decreasing the interconnections between the tester and the device under test. The complexity of the interconnections between DUT and the tester become one of the major showstoppers in evaluating the health of DUT [8]. Embedding memory and microcontroller units inside testers encounters fundamental constraints in tester design. It increases cost, size and complexity of the tester[9]. Also it limits the tester capability of testing. Decreasing memory size leads to a proportional decrease in the number of devices that can be diagnosed by the tester[10]. Versatile and multi-faceted testers can be made, but the cost will be very expensive. The rapid growth in the complexity of circuits requires a parallel and continuous development in the tester microcontrollers and that makes a difficult challenge [11-13]. To surpass these constraints, we introduce a star test topology (STT) that provides a means to arbitrarily observe test results and source test stimulus. The model requires minimal on chip/board resources (pins/nets). Also, it is not limited by chip function or complexity. Moreover, test access is not limited by the board physical factors and the test generation is highly automated[14]. Single trace is used to send and receive test data to/from test access port (TAP) or device under test. The proposed architecture is expected to reduced the yield loss due to the proven contact problems. Moreover, it is possible to achieve high cost reduction for complex SOC designs with negligible design and test overheads. The main objective is a development of the test access port and design for testability (DFT) chip architecture to reduce the complexity of testing nets, resources and pins connection. The proposed STT can efficiently utilize one test trace between TAP and each device under test DUT. Hence, one test access pin is required for each DUT. The advantages of STT are as follows

a) High test cost reduction can be achieved since the connection and bandwidth required for the interface between the TAP and one DUT is dramatically reduced to one data trace.

b) Negligible design and test overheads for complex SOC designs since it is compatible with IEEE 1149.1.

c) Each DUT is tested separately without depending on other DUTs.

d) Unlike 1149.1 SOC, there is no need to embed any instruction, identification or bypass registers in the SOC.

2. Star Test Topology (STT)

In STT, each DUT is connected to the central test access port TAP with a point-to-point connection. The TAP acts as the hub and the DUTs are the clients. The connection does not necessarily have to resemble a star to be classified as a star topology, but all of the DUTs test access pins on the printed circuit board must be connected to the TAP only. All traffic that traverses the network passes through the TAP. The TAP selects the targeted DUT to be tested, pass the test pattern and pass back the corresponding response pattern. The star topology is an easier topology to design and implement. The most important advantage of STT is its response to a node failure. When an error occurs, only one DUT will be affected rather than the entire network. Due to this feature, troubleshooting using a single point for an error connection is quite easy. In STT, the computer broadcasts the test input data to several DUTs via TAP, and the computer can easily identify a failed DUT. It is very easy to manage STT using connected DUTs because of its simplicity in testability. Since failures can be logically and easily located in STT, they are easily diagnosed.

3. STT Architect

In STT, TAP acts as the main hub and the DUTs performing like nodes. All test pins on DUTs use one line to interface TAP. Therefore test signals are directly transferred from TAP to the DUT without passing through other devices. A direct addressable method for preventing drive conflicts among the DUTs, is handled by TAP controller located in the PCB. The proposed architecture is depicted in Figure 1. When a data packet test data input (TDI) comes in TAP input pin, TAP reads the address information in the packet to determine its ultimate destination. Then, using serial to parallel shift registers and demultiplexer circuits, it directs the TDI packet to the next DUT on its journey. TAP perform the "data traffic directing" functions on the circuit. TAP forwards data packets TDI between incoming and outgoing interface connections. It routes them to the correct DUT using information that the packet header contains. And it captures the test data output TDO from DUTs forwarding them to PC. Test reset pin (TRST) is used to restart the test and forward the input data to new different DUT. Each DUT has its own test hub (TH). It is a circuit for interfacing multiple I/O pins and making them act as a single network segment. A signal introduced at the input of TH appears at the outputs of TH. It is a logical circuit that forwards data packets between TAP and DUT pins and vice versa.
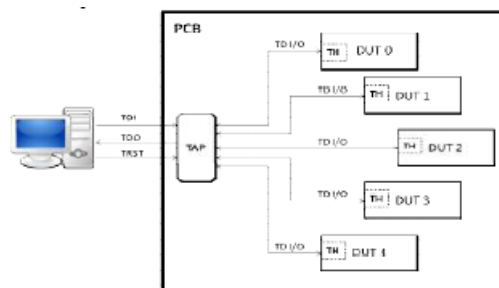

Figure 1: STT structure

TAP is utilized to communicate between the PC and each DUT. A TH controller is used to enable the PC to test DUT. According to IEEE 1149.1 standard, TAP must control all activities pertaining to the test and handles the DUT selection process, and TAP is used to interface the PC with DUT. Only one output pin, the test data output (TDO), is used to report results. The TDO of a single DUT is activated when the data is measured after the test, but the others. TH connects the channel of the TAP with the test input pins of the embedded cores according to the IEEE Standard 1500 compliance protocol. However, TH is composed of only one I/O pin. The ID and bypass registers are removed from the boundary circuit in order to reduce the built in circuits inside SOC.

TAP selects a DUT to be tested. To select the DUT, TAP controls the activation of the enable port of the TDO pad. If the DUT is selected, then the TDO enable port is activated, and the TDO pin drives the input value of the TDO to the PC. Otherwise, the TDO enable port will be inactive in order to produce high impedance values on the TDO pin to prevent the TDO bus contention.

4. Input Data Recognition

Generally, printed circuit board includes many integrated circuits in single board, each of which is separately designed and verified before use. Multiple test patterns may be applied to a single chip to test its functionality in accordance with IEEE Standard 1149.1, which states that three or four test input pins and one test output pin may be used for testing and debugging

of the SOC cores. TAP reads the input data to select which route should be used to forward a data packet, and through which physical interface connection. Routing is achieved by using internal pre-configured directive. Then, TAP forwards data packets between incoming and outgoing interface connections. It routes them to the correct DUT using information that data packet contains. TAP receives a serial data from USB, the first two digits of data is to apply a rising edge to start the TAP circuit, the following data bits is utilized by a counting register which controls the test/response data transmission and reception over the single trace. Then, addressing data is broadcasted to identify the destination of the data packet. Finally, the intended TDI is transmitted. As shown in Figure 2 the test data length is 7 bits (111) 2, the response data code length is 5 bits (101) 2, the DUT address is data is 1001 which is DUT 9. The remaining data represents the test pattern. Hence, TAP manages the flow of data across the circuit by only transmitting the received message to the DUT 9 for which the message was intended. A physical connection will be created to rout the data to DUT 9. Because of this, the proposed TAP is often considered more "intelligent" than the conventional TAP. Traditional TAPs doesn't provide identification of connected devices. This means that data packets have to be transmitted out to all devices under test, greatly degrading the efficiency of the connection.
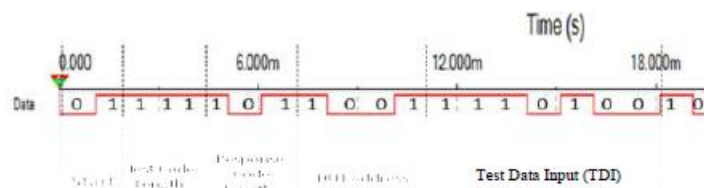

Figure 2: TAP input data

5. Test Data Routing

A routing circuit based on demultiplexer routes the test data input signal to one of several different data outputs. That is, one of its outputs is identical to the data input signal, while the other output signals are 0. The output that matches the input signal is determined by address data signal on the output of shift register. The routing circuit can in principle have any number of data outputs. The address data has as many bits as needed for the selection. N address bits suffice for 2 N data outputs. The routing circuit plays an important role in transmitting and also receiving test data and response data with DUT. By doing so, the routing circuit determines which DUT gets data written to it. Figure 3 describes the input data is distributed by input data decoder unit. The data router unit opens a port to the intended device under test by creating a physical connection.
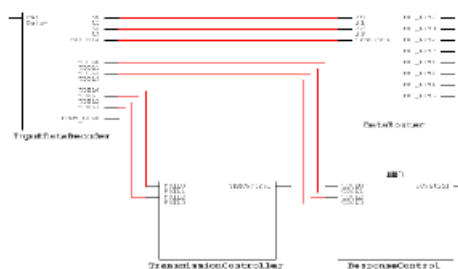

Figure 3: TAP input data distribution

6. Transmission and Response Time Controlling

Opening the transmission port is synchronized with transmission control unit operation. The unit starts counting down to close the transmission port as all test data transmitted. The countdown period depends on the value provided by the PC (TDIL0 TDIL1 TDIL2 TDIL3). Immediately after the transmission control unit finishes countdown, the transmission port closed and the response control unit open the port but on the opposite direction to receive the response pattern. The response control unit starts its own countdown according to the values provided by PC (TDOL0, TDOL1, TDOL2, TDOL3). The period must be enough to allow all response pattern bits to be captured. Figure 4 shows the test/response crossing control by TDI Control and TDO Control units. It 's seen clearly that TDI traffic starts at the rising edge of the TDI Control, while TDO traffic starts at the rising edge of TDO Control.
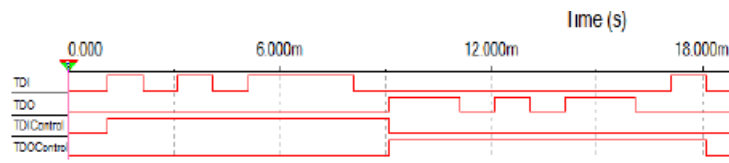
Figure 4: Test/Response data passage and crossing control

TDIControl and TDOControl play an importance rule in turning out the single interfacing trace between TAP and DUT to bidirectional trace.

7. DUT Test Boundary Circuit Architecture

The DUT receives test data serially from TAP, hence, there is a need for a shift register to broadcast the test pattern synchronously to the test pins. Also, the response pattern exits synchronously on the response pins and loaded serially by a serial-parallel shift register as shown in Figure 5.
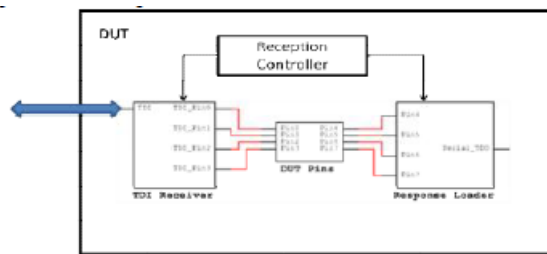

Figure 5: Test boundary circuit of DUT

A reception control unit is embedded inside DUT to indicate to the end of loading response pattern. This indication is exploited to control data traffic from/to the DUT. The reception control unit operation must be ultimately compatible with transmission/response control units in TAP.

8. Bidirectional Data Traffic

Units embedded inside test access port identifies the status of TAP, it has two modes; receiver or transmitter. Also, the reception unit inside DUT has the same function. Figure 6 shows how the control units turn the traffic direction over the single test trace. Diode 1N3613GP is used to avoid any signal contention over the trace. It has ignorable low forward voltage drop, ignorable leakage current, reverse current I R less than 0.1 μ A and high forward surge capability [15].

9. Conclusions

Star test topology using single bidirectional data line is one of the best means of reducing overall test costs. The proposed technique which is compatible with IEEE test Standards 1149.1 and 1500, does not require any additional test ports and the modification of embedded cores. In addition, a new seamless management method is proposed that can handle the multiple embedded cores. The proposed method can test multiple DUTs and cores and reduce the test cost drastically. The test cost reduction ratio over the previous works is very high with relatively small overheads. Therefore it is a practical solution for multi-site testing with high test cost reduction.
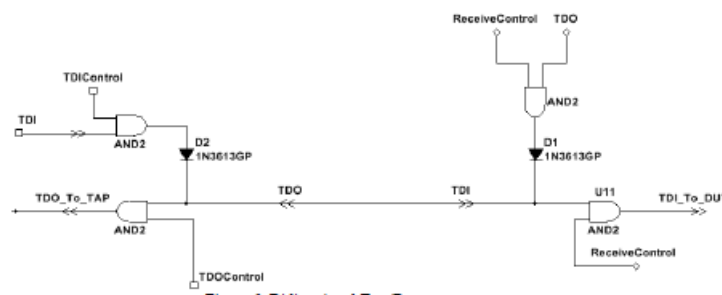

Figure 6: Bidirectional Test/Respone pattern trace

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