International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 08 | Aug 2019 www.irjet.net p-ISSN: 2395-0072

An Inductor based dc/dc Converter for Energy Harvesting Application with Low Input Voltage

Sri. Arun Raj S.R[1]

[1]*Assistant Professor, Dept. of Electronics & Communication Engineering, UBDT College, Davangere, Karnataka, India.*

Abstract - *To operate portable devices in low input supply voltages dc-dc converter are very useful and this type of devices are useful in energy harvesting application. In this paper is to boost low voltage dc-dc converter with inductor is used to produce high voltage supply voltage. In this paper input supply voltage is 500mV and it produce output voltage of 1.2 v. and by delivering a output current of 5.018μA and efficiency of about 34.44%. It is designed in 45nm CMOS technology by using Cadence Virtuoso software tool in this paper only single stage is used to produce output voltage of 1.2v and inductor were sized in 40μH to boost input voltage. Output power is 6.0216μW.*

Key Words: Converters, dc/dc power conversion, integrated circuit (IC) design.

1. INTRODUCTION

Energy harvesting or power harvesting or energy scavenging is method in which energy is derived from external source like solar power, thermal energy, salinity gradients, kinetic energy and wind energy are captured and stored for small wireless autonomous devices, and these are used in wireless sensor networks and wearable electronics. Energy harvesting has the low quality like low voltages, low currents or both and it is often unsuitable for standard integrated devices for supplying. For example when thermopile is exposed to low temperature gradients it give the output high currents at low input voltages. A energy harvesting takes the energy from environment and converts that energy into electrical energy and gives the output or an unregulated source voltage. Energy harvesting are used in application like portable, handheld and implementable electronics.

A dc/dc converter is a type of device like electronic circuit or electromechanical device, it converts from one voltage level to another voltage level of direct current (dc) and it is also type of power converter that convert power level range from very low that is small batteries to very high that is high voltage power transmission.

The dc/dc converter increase voltage of circuit without using more batteries of portable devices for to increase power. To increase the ultralow voltage dc/dc converter uses inductive based circuit, with the use of inductor it increases the voltage level and these are widely used in power electronics. An inductor is driven by almost lossless devices, ideal clock signals and large currents. In dc/dc converter it uses boost converter to step up voltage. The boost converter is used to increase the input voltage level from supply to high output voltage level to load. The boost converter is a class of switched mode power supply with containing two semiconductors that is diode and transistor and containing one storage element that is capacitor or inductor or both. In dc/dc converter output voltage is greater than source voltage. The boost converter is also called as step up converter and here p=vi, the output current is lower than source current.

In dc/dc converter there are three stages they are Boosting stage, Timing circuit and Regulator part. In order to convert ultralow voltage to high voltage that is 300m to 1.2v, boosting stage requires two cascaded step up converter that is stepup1 and stepup2. In this paper the voltage is step up by using inductor. In this design input voltage is increased by inductor. In boosting stage transistor is used as a switch. Boost stage performs in two operations, that are when switch is open and switch is closed. The clock generator second stage is to generate 75% duty cycle, combining D-flip/flop these are used to generate 50% duty cycle.

2. RELATED WORK

2.1. Boosting Stage:

In boosting stage to achieve output voltage of 1.2v there is two boosting stage is required so that first stage produced of about 450m-700mv and from this output is given to input supply voltage of second stage from this overall circuit produces of 1.2v. Here MOSFET M1 is act as a switch and MOSFET M2 act as a diode which is shown in below figure 2.1.

First stage is drive second stage is with use of first buffer stage. So to achieve high voltage duty cycle was set to 50% with comparison between boosting of voltage and consumption of power. Size of inductors are depending on various factors like capacitor, resistor and conductivity of switch also load and so many factors are consider for sizing of inductor. Depending on these factor only inductors L1 is chosen with help of discontinuous conduction mode also. So inductor L1 is sized at 40μH. In boosting stage design MOS switch M1 should be more in size, because more current flow in inductor causes more magnetic field and more voltage spikes are appeared. So that MOS size is mm in width and length. Here inductor current and voltage is given by

$$VL = L\left(\frac{di}{dt}\right)$$

Ripple current in inductor is shown below

$$\Delta I = \left(\frac{Vs}{L}\right)T1$$

There are two modes of operation. In first mode that is mode1 operation is given by, in this mode time duration is (0≤t≤DT) so that t is ends with DT so current in inductor and switch is given by

$$Vs = L\left(\frac{di}{dt}\right)i1$$

Solution of above equation is

$$i1(t) = \left(\frac{Vs}{L}\right)t + I1$$

In above equation I1is initial current and this current is end at mode1 that is t=DT to I2 that is i1 (t=DT) = I2 for this above equation can be written as

$$I2 = \left(\frac{Vs}{L}\right)DT + I1$$

In mode 2 operation inductor current is to be

$$Vs = Ri2 + L\left(\frac{di2}{dt}\right) + E$$

Similarly I2 is initially current. So that above equation can be written as

$$i2(t) = ((Vs - E)/L)\left(1 - \left(e\hat{}\left(\frac{R}{L}\right)t\right) + I2\ e\hat{}\left(\frac{R}{L}\right)t\right.$$

Here current end at mode 2 is similar to I1

$$i2(t = (1 - D)t) = I2 = \left(Vs - \frac{E}{L}\right)(1 - e\hat{} - (1 - D)z) + I2\ e\hat{} - (1 - D)z$$

Here $z = \frac{TR}{L}$

So ripple current is given by

$$\Delta I = I2 - I1 = \left(\frac{Vs}{L}\right)DT$$

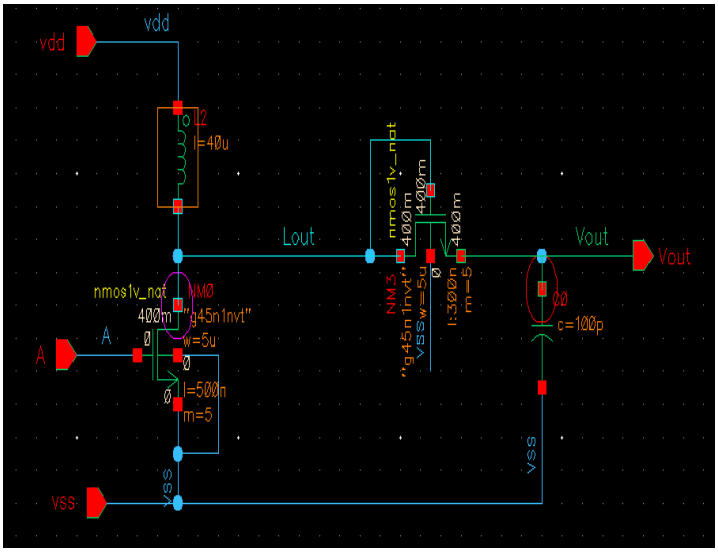

Fig 2.1: Single stage step up converter.

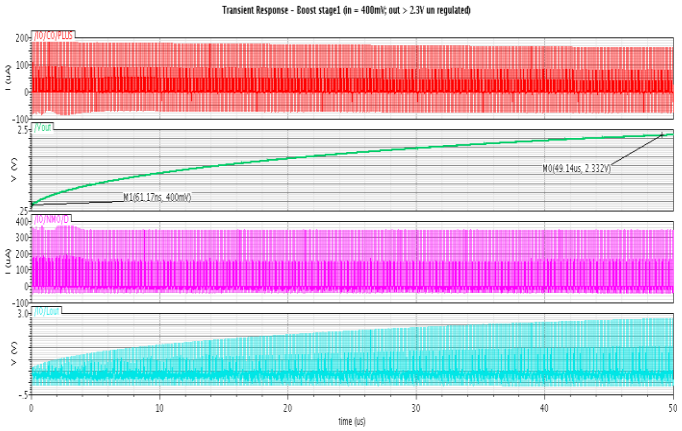

Fig 2.2: Output waveform for single stage step up converter.

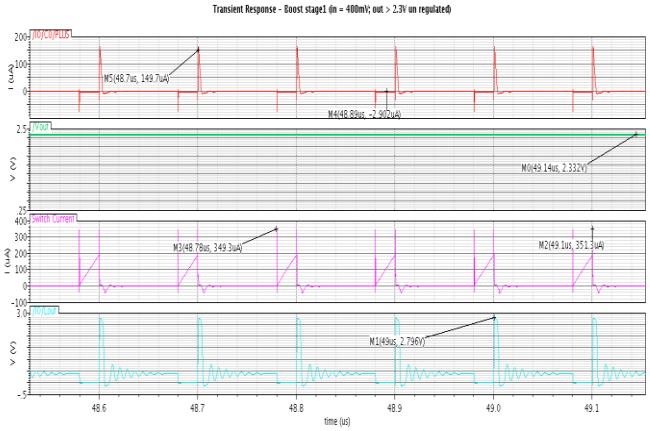

Fig 2.3: Un- regulated output for single step up converter.

2.2. Clock Generator: Clock generators are used to give the input voltage signal to dc/dc converter. Clock generator consists of oscillator and d flip flop. Oscillator gives oscillation signals to circuit. D flip flop produce duty cycle to circuit. Clock generator is first stage of converter and it is self-generated input signal without using any external voltage it give self-input to circuit. Clock generator is nothing but oscillator it give timing signal to converter in order to maintain synchronization operation of the circuit. Clock signals may be analog or discrete signal it provide both analog signal and discrete signal.

2.3. Oscillator: Oscillator is a simple ring chain oscillator. The inverter back to back connection is formed by oscillator, number of inverter stages is connected back to back and number should be odd number. From supply voltage it will work on its own input supply voltage this means without need of external input supply voltage it will work with supply voltage. Oscillator amplify noise signal and produce output signal. In our project after 10µs only oscillator get oscillate input signal before that 10µs there is no oscillation process after 10µs only oscillator give signal. As the number of oscillator stages increases frequency also increases and delay is decreases. Delay and frequency both inversely proportional to each other and formulae for delay is given by

T = 1/ (2nf) or f = 1/ (2nT)

To achieve higher frequency one number of stages should be more or delay should be less and operating frequency is 1MHz to 5MHz and 1MHz is sufficient to operate circuit. The circuit is to operate in low input voltage, so inverter stage of NMOS and PMOS should have low threshold voltages. This low threshold voltage causes leakage current. In inverter NMOS and PMOS is taken as low threshold voltages in order to reach low input power supply. Oscillator is nothing but electronic device it produces electric signal in a periodic manner so signals like square wave or sine wave and it is used to convert direct current to alternating current with use of supply voltage.

2.4. D Flip Flop: D flip flop are used to produce 50% of duty cycle. D flip flop architecture is based on pass transistor. D flip flop produce Q and Q^- as output these produce 50% duty cycle. Output of oscillator give input of this D flip flop so overall produce clock signal with 50% duty cycle. D flip flop architecture with use of pass transistor is mainly because of low power supply, with use of low input voltage it should work. One more advantage of pass transistors are used to design D flip flop because it requires less area and count of transistor and also to reduce power consumption.

2.5. Regulator: Regulator is a device which is used to control circuit like temperature and speed of circuit. Regulator gives enable signal to clock generator to first stage of step up converter. It consist of mainly voltage reference and level shifter these two output are connected to input of comparator, it compares two input signals that is Vref and level shifter and give output zero and ones. In regulator it fixes output voltage means it fixed at a certain voltage. In this paper regulator output is fixed at 1.2V. Current is appear at load it changes dramatically so regulator is used. Power supply of regulator has output of converter and regulator takes power consumption.

2.6. Voltage Reference: In voltage reference there are three stages: first stage is start up stage, second stage is current generator and last stage is acts as a active load. So from current generator stage it fixes constant output voltage. Voltage reference can operate minimum voltage that is 0.9v to 4v. In active load stage all transistor should be saturation region and it is given by equation as

$$Vref = Vth + \left(\frac{\sqrt{2I}}{k}\right)$$

Where I is current at active load stage, in output of voltage reference temperature is depends on various factor those are threshold voltage, mobility and bias current. So above equation states that output of voltage reference is depend on mobility that is k and threshold voltage Vth and I is bias current. So in voltage reference bias current should be fixed so current generator are used to produce fixed output voltage. The generator current consists of simply NMOS and PMOS back to back connection totally current in all MOSFET's should be same. So that generator current can achieve. In current generator M1 and M3 transistors are in sub threshold region and M2 and M4 transistors are in saturation region. In active load stage three transistors are used and those are diode connected and these transistors are mainly used to compensate temperature of voltage reference. In band gap there is a resistors are used for voltage reference, so area is more for resistor but in this architecture there is use of resistance only MOSFET's are used so area is also less.

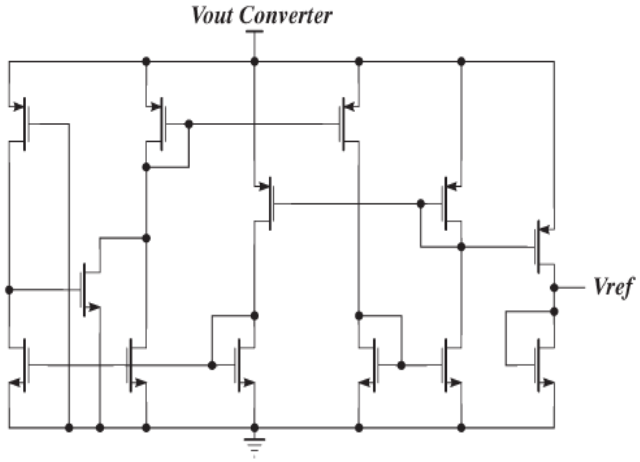

Fig 2.4: Schematic diagram for Voltage Reference.

2.7. Level Shifter: Level shifter is a digital device and it is used to produce one voltage to another domain. So it also converts one logic level to another logic level. It produces output voltage below supply voltage. If there is no level shifter voltage levels are cross signals and correctly not sampled. It fully converts one voltage level to a different voltage level. In level shifter there is diode connected, So Vds is equal Vgs and supply voltage is distributed to both Vds1 and Vds2.

So that

Vds1=Vdd – Vds2.

In M2 Vds < Vth1 so, Vgs2 ≤ Vth1 ≥ Vds2 so Vds ≤ Vth1.

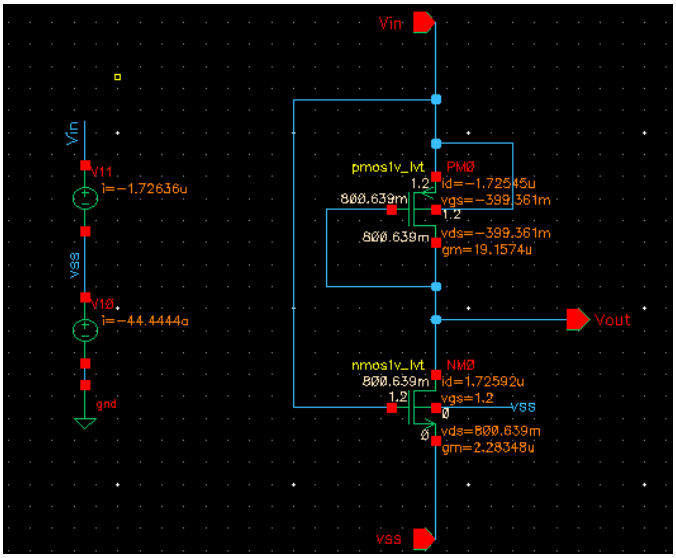

Fig 2.5: Schematic diagram for level shifter.

2.8. Comparator: Comparator is used as a regulator to fix output voltage in comparator it compares two input voltage and produce output signal in high or low voltages or one and zero signal. Output of comparator is one means it produce whatever in supply voltage it will produce and zero means it produce zero voltage. In comparator output is digital form because it produces one or zero. Output voltage works on condition like v+ and v- there are two input signal if v+ is greater than v- it will produce high supply voltage that is 1 and one more condition if v+ is less than v- it will produce zero voltage or 0. Here v- is reference voltage is used as v- and level shifter is used as a v+ and it produce output in 1 or 0. Comparator is simply operational amplifier comparator voltage and op-amp have differential input it contains three stages one is differential amplifier and second stage is common source amplifier if one more inverter is added to that common source amplifier that it becomes comparator so both differential and common source amplifier should be in saturation region.

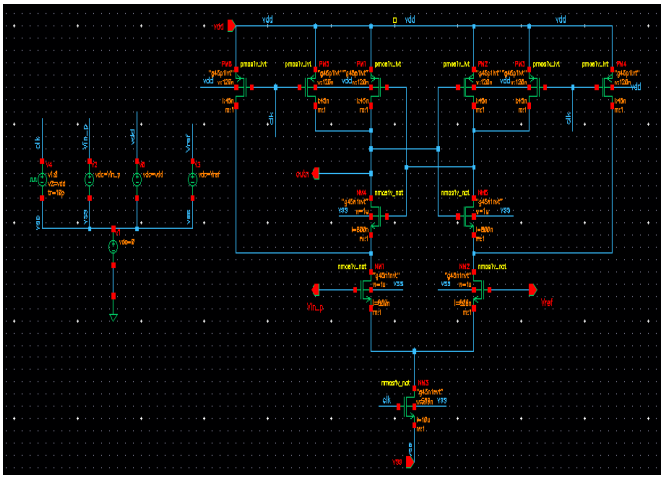

Fig 2.6: Schematic diagram for latched

Figure 2.6 shows schematic diagram for latched comparator, there are two differential input in circuit and produces output in form of zero and one.

Figure 2.7 shows output waveform for comparator, input is level shifter and voltage reference

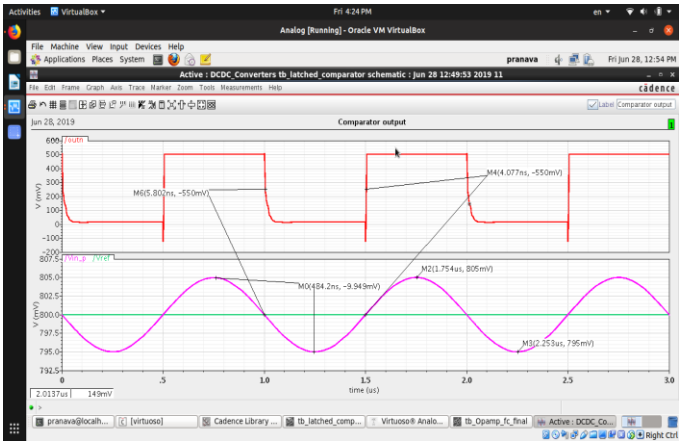

Fig 2.7: Output waveform for Comparator.

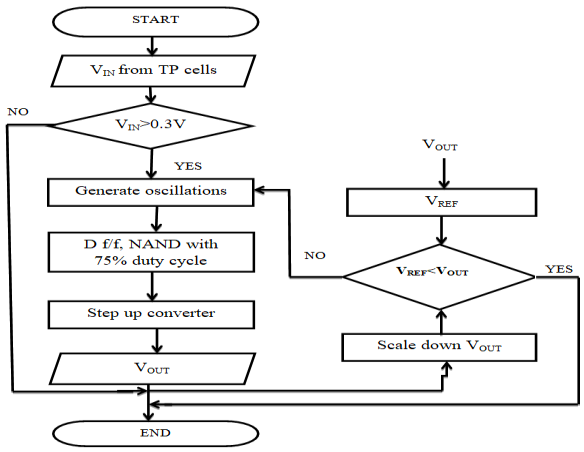

Fig 2.8: Flow chat for Circuit Diagram.

3. EXPERIMENTAL RESULTS

Output waveform for overall dc/dc converter is 1.2v. For regulated output, it produces 1.2v. But in unregulated output, it can produce more than 2.5v. The output waveform is as given below in figure 3.1 & 3.2.

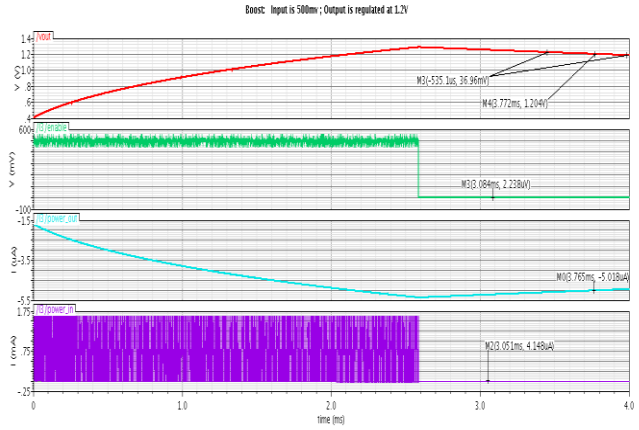

Fig 3.1: Output waveform for regulated output voltage.

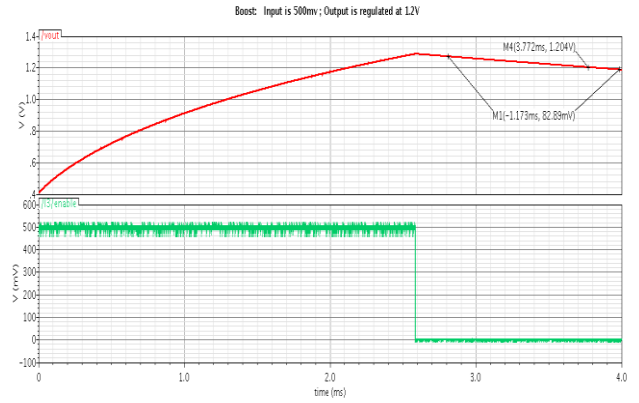

Fig 3.2: Outputs for Vout and Vin.

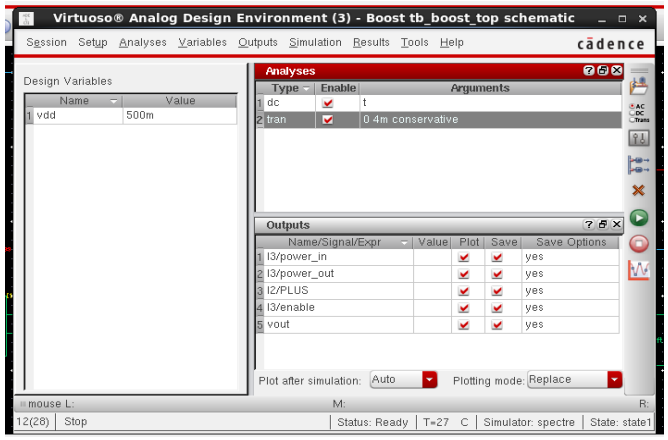

Fig 3.3: Transient time for converter.

Figure 3.3 shows transient execution window in cadence virtuoso software, so time is set as 4m conservative and it is checked for both dc and transient response. All enable, input voltage output voltage and power in, out all are shown in above window.

Discussion:

Comparison between previous work and with this paper is given below in the comparison table. And working of circuit diagram is shown in flow chat. In this paper, Input is 500mv supply voltage and produce 1.2v output voltage and efficiency of about 34.44%.

Table -1: Performance summary and comparison table between designed converter and previous work.

Parameter	[5]	[6]	[7]	[8]	[9]	[11]	In this Paper
CMOS Technology	180-nm	90-nm	35-nm	130-nm	350-nm	180-nm	45-nm
Extra masks	Low Threshold	With Tripple Well	Not Mentioned	Not Mentioned	Not Mentioned	Low Threshold	Vth
Input Supply Voltage	200mv	300mv	600mv	20mv	35mv	120mv	500mv
Output Supply Voltage	1.2v	1v	2v	1v	1.8v	1.2v	1.2v
External Supply Voltage	NO	NO	2v	0.65v	NO	NO	NO
External Required Component	2 Inductor	None	2v Buffer Capacitor	1 Inductor 1 Capacitor	1 Inductor 1 Switch	2 Inductors	1 Inductor
Efficiency Obtained	36%	Not Provided	70% (Just Boost Converter)	52%	58%	30%	34.44%

4. CONCLUSION

In this paper dc/dc converter is to operate with input voltage supply of 500mv. And this converter can produce an output voltage of 1.2v, by delivering output current of about 5.018μA and overall efficiency produce 34.44%. And the circuit is used for energy harvesting application. The technology is 45-nm with 500mv input supply voltage and it produces 1.2v output voltage.

REFERENCES

[1] L. Mensi, L. Colalongo, A. Richelli, and Z-M. Koacs-Vajna, "A new integrated charge pump architecture using dynamic biasing of pass transistors," in Proc. ESSCIRC, Sep. 2005, pp. 85-88.

[2] M.D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump with consideration of gate-oxide reability in low-voltage CMOS processes," IEEE J. Solid-State Circuits, vol. 41, no. 5, pp. 1100-1107, May 2006.

[3] G. Palumbo, D. Pappalardo, and M. Gaibotti, "A CMOS charge pump circuits: Power consumption optimization," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 49, no. 11, pp. 1535-1542, Nov. 2002.

[4] A. Richelli, L. Colalongo, M. Quarantelli, M. Carmina, and Z. M. Kovacs-Vajna, "A fully-integrated inductor based 1.8 V-6 V step-up converter," IEEE J. Solid-State Circuits, vol. 39, no. 1,pp.242-245, Jan. 2004.

[5] A. Richelli, L. Colalongo, S. Tonoli, and Z. M. Kovacs-Vajna, "A 0.2 V-1.2 V dc/dc boost converter for power harvesting applications," IEEE Trans. Power Electron.,vol.24,no.6,pp. 1541-1546, Jun. 2009.

[6] T. K. Halvorsen, H. A. Hjortland, and T. S. Lande, "Power harvesting circuits in 90 nm CMOS," in Proc. NORCHIP, Nov. 2008,pp. 154-157.

[7] I. Doms, P. Merken, R. Mertens, and C. Van Hoof."Integrated capacitive power-management citcuit for thermal harvesters with output power 10 to 1000µW," in Proc. ISSCC, Feb.2009,pp.300-301.

[8] E. Carlson, K. Strunz, and B. Oits, "20mV input boost converter for thermoelectric energy harvesting," in VLSI Symp. Tech. Dig., Jun. 2009,pp. 162-163.

[9] Y. K. Ramadass and A. P. Chandrakasan, "A batteryless thermoelectric energy-harvesting interface circuit with 35mV startup voltage," in Proc. ISSCC, Feb.2010,pp.486-487.

[10] G. De Vita and G. Iannaccone, "A sub-1 V, 10ppm/C, nanopower reference generator," IEEE J. Solid-State Circuits, vol.42, no. ,pp. 1536-1542, Jul.2007.

[11] Anna Richelli, Simone Comensoli, and Zsolt M. Kovacs-Vajna," A DC/DC Boosting Technique and Power Management for Ultralow-Voltage Energy Harvesting Applications," IEEE. Industrial Electronics, vol.5,No.6,June.2012.