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High Efficient Asymmetric DC Source Configured SCMLI

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Abstract – *This paper is going to describe the Switched Capacitor Multi-Level Inverter (SCMLI) topology with triangular multicarrier SPWM. This developed SCMLI having the asymmetric DC source configuration to obtain several levels of an output voltage. The detailed principle of operation, power loss analysis is included. The applications of this developed topology are mainly in industrial and renewable energy sources because of its high output voltages. The simulation analysis of this developed SCMLI structure is witness of the effectivity of a SCMLI over other topologies.*

Key words:* Boosting, Modulation Index (MI), Total Harmonic Distortion, Voltage balancing, Triangular Multicarrier SPWM (TMC SPWM), Switched capacitor and RECS.

I. INTRODUCTION

At present, the inverters are having a vital role in industrialized and in household applications. Multilevel inverters are became workable DC-to-AC converting of power used for altered applications, like electrical drives, RECS applications, electric utilities, and filters [1]. For multiple application purposes a new SCMLI is developed. For reliable working of inverters PWM techniques are preferable. Comparing with normal two level inverters, the Multilevel Inverters shows many advantages, like producing synthesized output voltage, higher power production ability, low losses with high efficiency, less voltage strain across switching devices [10] those contains IGBTs, MOSFETs, power diodes, DC sources and capacitors. These sources be the main for synthesized outputs. In general, three usual MLI topologies are present, namely, flying capacitor (FC), diode clamped (D-C) and cascaded H-bridge (CHB). Another main drawback of conventional MLI is that they require extra supplementary circuit to maintain voltage as balanced at capacitors; this circuit amplify its dimension, price and difficultness of converter [4].

The latest Multi level inverter arrangement by way of more no. of steps linked by way of a small amount of power switching devices suggested [7]. The latest switched capacitor-diode structure is presented [3]. It needs more capacitors in addition to as diodes on the way to generate heights levels of voltage at outputs. On the way to defeat these problem supplementary circuits and composite controlling strategy has presented. The resonant Switched Capacitor converter developed in [6] Even though these topologies minimize the capacitor voltage unbalance issue, the solution method amplify system as bulky, pricey and difficulty lacking the remaining advantage of self voltage boost ability.

On the way to attain self voltage boost capacity and ease the unbalanced capacitor voltage issue exclusive of taking supplementary circuit, SCMLI was presented. Here capacitors role is to be as alternative DC voltage sources. SCMLI can produce multiple levels of output voltage with minimized number of sources and power switches. In count, the SCMLI also enhance its source voltage up to required level of load voltage with alternating switching of those capacitors. Another main benefit of SCMLI is obtaining of capacitor voltage balance with the help of switching sequence tactic.

The remaining part of this paper was structured like. The developed 21-level SCMLI structure, its thorough operation of working is shown in Section II modulation technique is explained in Section III. Section IV gives power loss analysis and SC selection and comparison is presented. Section V will give those simulation results of developed SCMLI. Section VI is going to conclude this work.

II. DEVELOPED SCMLI

Fig.1 shown that the developed SCMLI construction. It consisting of 2 asymmetric DC voltage sources (*Vi* & 4*Vi*), 14 unidirectional switching devices either IGBTs or MOSFETs (*Si1*, *Si1*', *Si2*, *Si2*', *Si3*, *Si3*', *Si4*, *Si4*',*Si5*, *Si5*', *Si6*, *Si6*', *Si7* and *Si7*'), and 4 Switched capacitors (*Ci1*, *Ci1*', *Ci2* and *Ci2*'). This arrangement can make 21 voltage levels across the load terminals *xi* and *yi*.

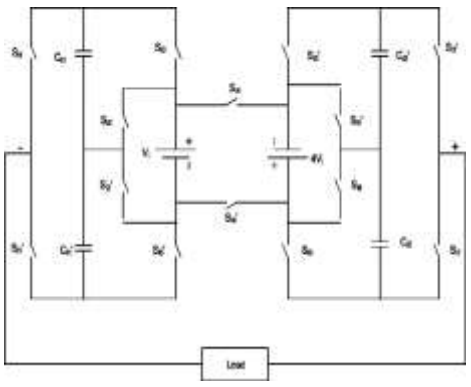

Fig.1. Developed SCMLI

In this developed topology, the capacitors *Ci1* and *Ci1*' can charge up to *Vi*, where as capacitors *Ci2* and *Ci2*' can charge up to 4*Vi* with suitable switching actions. This indicates that developed topology able to change the state of capacitors from charge and discharge simultaneously, that helpful to maintain voltage of capacitor at desired levels with lesser amount of voltage ripples.

1. Generation of zero voltage level

The Zero level output voltage was generated with turning ON the switches S_{i1}', S_{i3}', S_{i4}', S_{i5}, and S_{i7}, the zero output voltage appears across the load terminals. in this circuit condition the capacitors C_{i1}' and C_{i2} kept in charge condition by making turned ON of power switches $S_{i2,}$ S_{i6}' in that order. whereas capacitors C_{i1} and C_{i2}' are disconnected mode, as shown in Fig. 2.

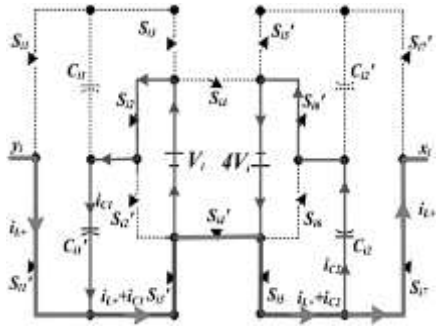

Fig.2. equivalent circuit of zero level voltage

2. Generation of ±2V$_i$ Voltage Level

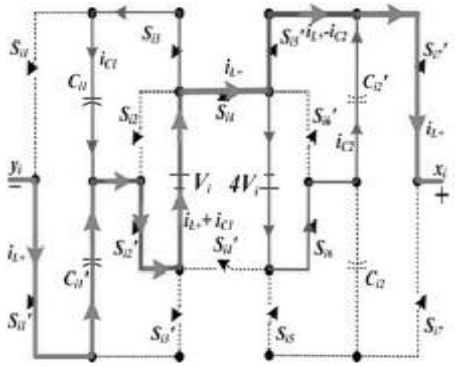

Fig.3. Equivalent circuit of +2 voltage level

When switches S_{i1}', S_{i2}', S_{i4}, S_{i5}', and S_{i7}' are turned ON, capacitor C_{i1}' was associated into series to V_i. Hence, that voltage across capacitor C_{i1}', was auditioned with V_i and capacitor C_{i1}' is in discharging mode, like showed inside Fig.3. Then load terminal output voltage nearly equal to 2V_i. In these switching, capacitors are in charge condition by means of making turn on of switches S_{i3} and S_{i6}, respectively. Similarly, −2V_i can be developed at the output terminals by adding voltage across capacitor C_{i1} with the input voltage V_i.

3. Generation of ±8V$_i$ Voltage Level

A +8V_i voltage level will formed at load by addition of supply voltage 4V_i with the capacitor voltage vC_{i2}. Therefore, capacitor C_{i2} is in discharging manner. This situation can be obtained by turning on switches S_{i1}, S_{i3}, S_{i4}, S_{i6}, and S_{i7}.

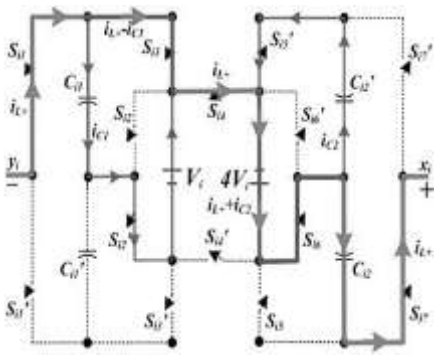

Fig.4. Equivalent circuit of +8 voltage level

In this mode that capacitors C_{i1} and C_{i2}' are in charging condition by turned ON of power switches S_{i2}' and S_{i5}', correspondingly.

4. Generation of ±10V$_i$ Voltage Level

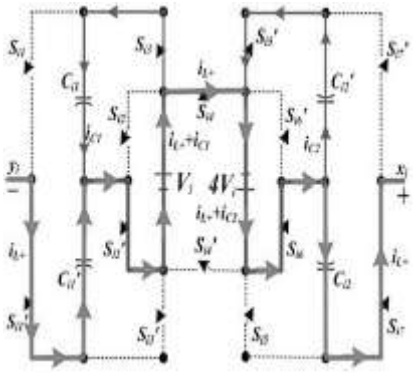

Fig.5. Equivalent circuit for +10 voltage level

There Fig.5 is the equivalent circuit for +10V. When switches S_{i1}', S_{i2}', S_{i4}, S_{i6}, S_{i7}, S_{i3}, and S_{i5}' are turned ON, capacitors C_{i1}' and C_{i2} are connected in series to both supply voltages,

whereas capacitors C_{i1} and C_{i2}' are connected in parallel to V_i and 4V_i, correspondingly therefore, In this mode, the output load voltage is summing up with supply voltages, those are almost +10V_i. Similarly, −10V_i can be created by making turned ON the opposite switches.

Similarly the remaining voltage levels also having various switching patterns. According to that only the SCMLI will operate and produce 21 level output voltage across the load.

III. MODULATION TECHNIQUE

These Pulse Width Modulation (PWM) techniques developed on the way to decrease the THD value of that load terminal voltage. Every variation on sinusoidal wave output load voltage are cause harmonic at load and this harmonic produce EMI, losses and pulsating torque occurs in electrical drives. Rising of switching frequency in PWM causes reduction of lower order harmonics by affecting the carrier switching frequency [2].

The reference have maximum magnitude Ar and as well as frequency fr. The operating principle of multi carrier SPWM is that comparing of triangular carrier signal with sinusoidal reference wave. When carrier signal is more compared to reference then relevant switch is ON and when reference signal is more compared to carrier then relevant switch is OFF. Here multilevel inverters, the amplitude modulating index, Ma and modulating frequency ratio Mf were shown in equation (i) and (ii),

$$M_a = \frac{A_r}{(m-1)A_c} \quad \text{(i)}$$

$$M_f = \frac{f_c}{f_r} \quad \text{(ii)}$$

Here Ar and Ac are amplitude of reference and carrier wave in that order. Found fr and fc are frequencies of reference and as well as carrier wave correspondingly. Now modulation index taken as 0.98 for SCMLI for 14 power switches with different carrier signals.

1. Triangular Multicarrier SPWM (TMC SPWM)

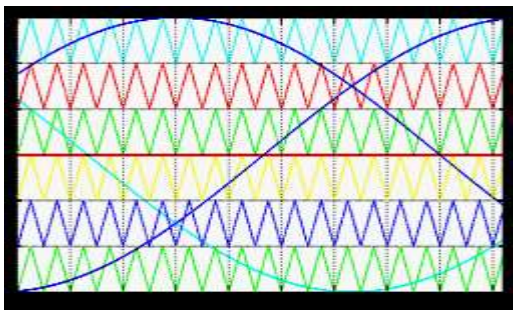

Fig.6 PD of TMC SPWM with Ma=1

The multicarrier modulation technique used for multilevel inverter. Multilevel inverters completed with the usage of some triangular waves as a carrier signal and single sine wave as a reference wave for each and every phase.

Carrier implemented sub-harmonic PWM (SH-PWM) that followed m no. of level inverter, m-1 no. of carriers of similar frequency fc, identical magnitude Ac are liable such bands engage contiguously. That shows by usage of regular triangular carrier waves produce fewer harmonic distortions where output side of inverter. Now IPD technique is used. This IPD technique has better results than the other techniques.

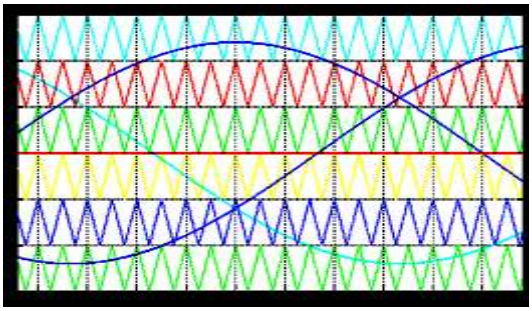

Fig.7 IPD of TMC SPWM with Ma=0.8

IV. POWER LOSS ANALYSIS

1. Efficiency

The losses in the developed SCMLI structure is mostly intense on three main power losses, specifically losses during switching (P_{sw}), losses during conduction (P_{con}), and losses with capacitor ripples (P_{ripple}). Then overall power loss (P_{loss}) of SCMLI is

$$P_{loss} = P_{sw} + P_{con} + P_{ripple} \quad (1)$$

The efficiency (η) of the developed inverter can be given by (2)

$$\eta = \frac{P_{out}}{P_{out}+P_{loss}} \quad (2)$$

Where P_{out} is the output power of inverter.

2. Switching Losses

This is the most common loss in a power switch take place when the switch is in transition state. When the switch state is changed from OFF to ON or from ON to OFF. When the linear approximation among the switch current and the switch voltage throughout the transition period t_{on} and t_{off} is measured, the energy losses that happen in the i^{th} power switch is

$$E_{i,on} = \int_0^{t_{on}} V_{swi}\left(1-\frac{t}{t_{on}}\right) I_i\left(\frac{t}{t_{on}}\right) dt$$

$$= \tfrac{1}{6} V_{swi} I_i t_{on} \quad (3)$$

$$E_{i,off} = \int_0^{t_{off}} I_i'\left(1-\frac{t}{t_{off}}\right) V_{swi}\left(\frac{t}{t_{off}}\right) dt$$

$$= \tfrac{1}{6} V_{swi} I_i' t_{off} \quad (4)$$

Where f_{sw} is the switching frequency; and I_i and I_i' present the switch current after ON and before OFF conditions correspondingly. To discover the energy losses per fundamental cycle of the i^{th} switch, the number of ON

transitions ($N_{on,i}$) and OFF transitions ($N_{off,i}$) over a cycle should be evaluated. Then, the energy losses per cycle for the i^{th} switch is

$$E_{i,sw} = (N_{on,i} \times E_{i,on}) + (N_{off,i} \times E_{i,off}) \quad (5)$$

The switching power losses of the i^{th} switch over a cycle are

$$P_{i,sw} = \frac{(N_{on,i} \times E_{i,on}) + (N_{off,i} \times E_{i,off})}{T}$$

$$= \frac{1}{6T} V_{swi} I_i (N_{on,i} t_{on} + N_{off,i} t_{off}) \quad (6)$$

Where T is the time for a fundamental cycle.
The overall switching losses of the 21-level SCMLI inverter is

$$P_{sw} = \sum_{i=1}^{14} P_{i,sw}$$

$$= \sum_{i=1}^{14} (N_{on,i} \times P_{i,on}) + (N_{off,i} \times P_{i,off}) \quad (7)$$

3. Conduction Losses

To find commonly obtain losses of the developed inverter arrangement, the internal resistance of each and every element must considered. From this investigation of the equivalent circuit the average power loss in conduction period in positive and as well as negative half cycles are same. The average power losses of conduction period for one full cycle are evaluated.

Now taking into consideration of First positive voltage level. The period of the first positive voltage level is $(t_2 - t_1)$ s in T (one full cycle). Therefore, the average loss of power during conduction for both first levels of load voltage given as

$$P_{ave1} = \frac{2(t_2 - t_1)}{T} (p_{1+} + p_{1-}) = \frac{4(t_2 - t_1)}{T} p_{1+} \quad (8)$$

correspondingly average power loss of that conduction period for remaining voltage levels are to be calculated based on equation (8). Thus, the average conduction losses for a cycle is

$$P_{con} = \sum_{j=1}^{10} P_{avej} \quad (9)$$

Where j=1, 2, 3,…., 1

4. Capacitor Ripple Losses

These are arise because of voltage variation among that capacitor and its relevant feeding source. Considering capacitor C_k is associated with discharging operation on behalf of a greatest time period $(t_{j+1} - t_j)$, subsequently highest voltage ripple of that consequent C_k is shown as

$$\Delta v_{ck} = \frac{1}{c_k} \int_{t_j}^{t_{j+1}} i_{ck}(t) dt \quad (10)$$

$i_{Ck}(t)$ is capacitor's current during dis-charging. these currents are naturally similar that of output terminal currents. Then capacitor ripple losses per one full cycle of capacitor C_k evaluated with

$$P_{ripck} = \frac{1}{2T} C_k (\Delta v_{Ck})^2 \quad (11)$$

Correspondingly, the ripple losses for each and every capacitors C_{i1}, C_{i1}', C_{i2}, and C_{i2}' for a full cycle determined by equation(11). Then entire capacitor ripple losses for one full cycle are given as

$$P_{ripple} = P_{ripCi1} + P_{ripCi1'} + P_{ripCi2} + P_{ripCi2'} \quad (12)$$

V. MATLAB SIMULATION RESULTS

The Switched Capacitor Multilevel Inverter (SCMLI) model with triangular multi carrier SPWM is simulated in MATLAB software to demonstrate achievability of SPWM technique.

Fig.9 shown simulated model of developed SCMLI and that designed and simulated using MATLAB software. This simulation model considered IGBTs as power switches devices, then simulation results of SCMLI are obtained when 50ohms resistive load is connected.

In these cases, the magnitudes of the DC power supplies are set as 100V and 400V. With these DC sources, the developed topology can produce a maximum output voltage of 1000V. The load across the SCMLI is 50ohms corresponding to that the output current of SCMLI is 45.4A. The output power of developed SCMLI is obtained 127.66W. For ease, all the capacitors are set as 560 µF when the primary switching method is implemented; switching losses are noticeably a smaller amount. With calculating the losses and obtained switching losses as 0.527W, capacitor ripple losses as 0.0799W and Conduction losses as 4.69W. Then overall losses in developed SCMLI are 5.296W.

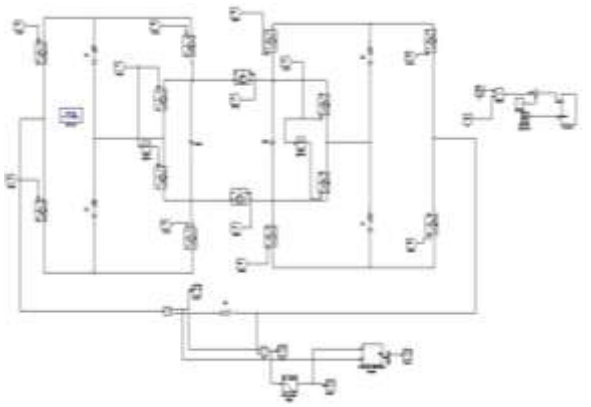

Fig.8 Simulation model of SCMLI

By the observation capacitor ripple loss and switching losses are smaller than conduction losses. With the output power and losses the efficiency can be calculated

using equation (2). And this developed SCMLI also having less THD of nearly 0.61% of Output Voltage for fundamental frequency and it is shown in Fig.13.

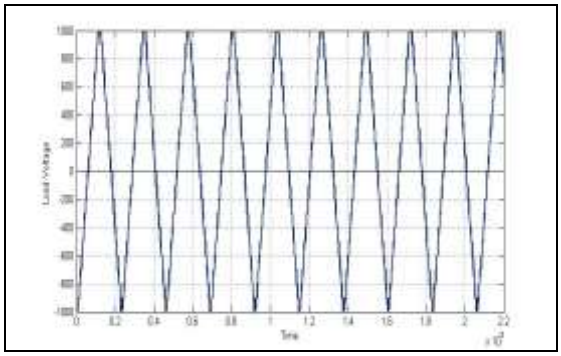

Fig.9 voltage at load terminals without filter

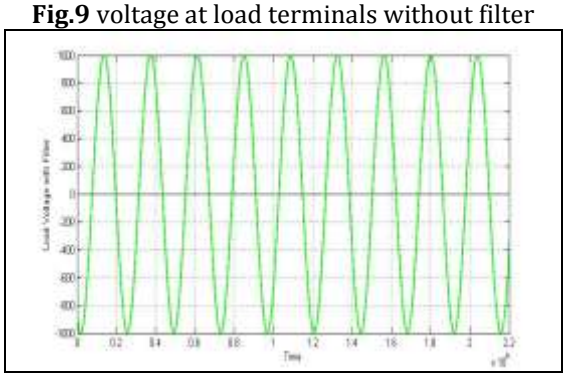

Fig.10 voltage at load terminals without filter

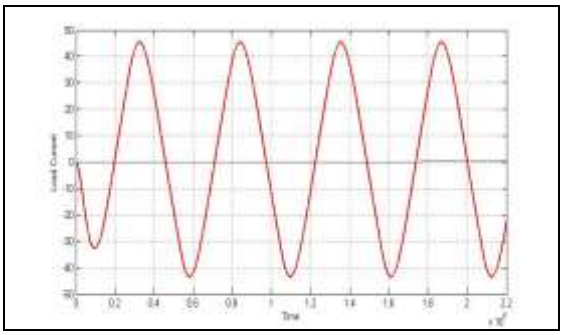

Fig.11 Load Current waveform

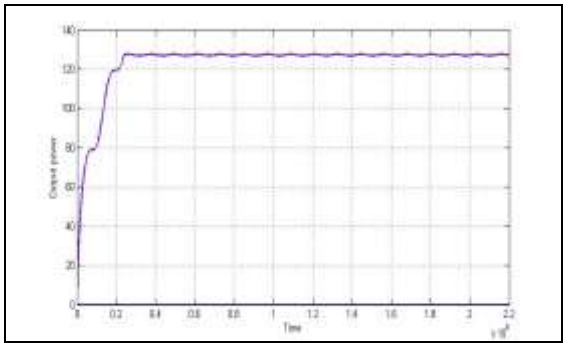

Fig.12 Output power

The Output 21-level voltage waveform at load terminals be shown inside the Fig.9. And filtered output load terminal voltage be shown inside the Fig.10. The Load current and output power of developed SCMLI is shown inside the Fig.11 and inside the Fig.12 correspondingly.

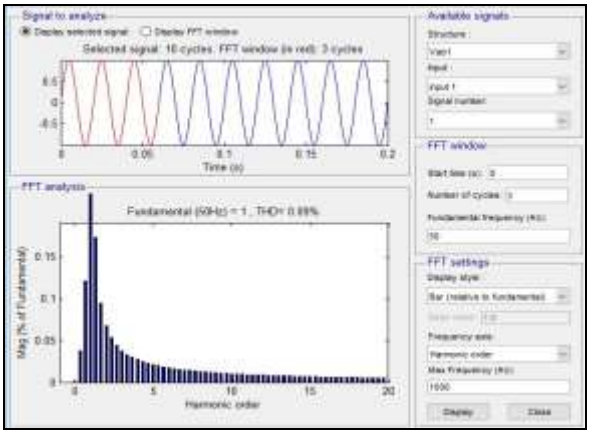

Fig.13 FFT analysis of a filtered output voltage

VI. CONCLUSION

A TMCSPWM SCMLI structure developed in this paper. That introduced topology shows the potential to boosting of its source voltage. Additionally, the developed topology provides considerably lesser losses than remaining topologies. For that reason the introduced topology got efficiency of 96.02%. This introduced topology also applicable for high-voltage applications like industries as well as domestic purposes and RECS. The results are obtained by doing simulation for a 50ohms load, percentage THD of the voltage is also less. Therefore it clearly justifies the developed SCMLI topology with Triangular Multi Carrier SPWM technique is Efficient. And it also has wide range of high voltage applications such as compensating devices in transmission, driving of electrical drives in industries and etc.

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