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DESIGN AND ANALYSIS OF SINGLE-STAGE BRIDGELESS BOOST- FLYBACK PFC CONVERTER WITH SNUBBER CIRCUIT

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Abstract - *Single stage bridgeless boost-Flyback PFC converter with the Snubber circuit is designed for output of 54V and 80W. The circuit is operated at the switching frequency of 60 KHz. This circuit is compared with the conventional Bridgeless Boost-Flyback PFC Converter by simulation results. The power factor is still improved by operating the input boost inductor in the Discontinuous mode. A single dc-link Capacitor is divided into two among which one is used as the Snubber Capacitor and the other is used as the dc-link Capacitor hence the voltage rating of the dc-link capacitor used in the circuit reduces. The Snubber circuit is employed to clamp the voltage spike of the switches which also improves the power transfer efficiency by utilizing the Leakage inductor energy.*

Key Words: **Bridgeless boost PFC Converter, Flyback converter, Snubber circuit.**

1. INTRODUCTION

The AC-DC converters have been widely used in the low power applications like notebooks, workstations, desktop computers, SMPS devices and servers etc. In context of these major requirements the need to develop AC-DC converters with high power factor, low switching losses, low conduction losses, low harmonic distortions and high power efficiency have increased. Hence the bridgeless rectifier circuits have been employed thereby reducing the conduction losses.

The fig 1(a) shows the circuit diagram of the conventional two stage bridgeless boost-Flyback PFC converter. The two stage Converter has the bridgeless boost rectifier as first stage the dc output of this rectifier is fed to the Flyback converter circuit through the large dc-link Capacitor $C_{sn.}$. To reduce the voltage spikes of the switches the passive Snubber Circuit is employed. The major concern in the AC-DC conversion is to maintain the unity power factor, with low distortion and achieve high power transfer efficiency.

Several Bridgeless boost PFC rectifiers were proposed which have achieved nearly unity power factor. The converter in the paper [1] uses the magnetic integration technique in order to reduce the number of components in the boost PFC and Flyback model thus achieving higher efficiency.

Various other converters have been proposed for this AC-DC conversion like in the paper [2] a bridgeless Sepic converter is employed as the PFC converter. The rectifier which is bridgeless-boost is used along with the half-bridge asymmetrical PWM dc–dc converter is proposed in paper [3]. The turning-on of the switches at Zero Voltage or near Zero Voltage is termed as Valley switching which is achieved in this converter due to the resonance that occur between the parasitic capacitor of the switches and input boost inductor.

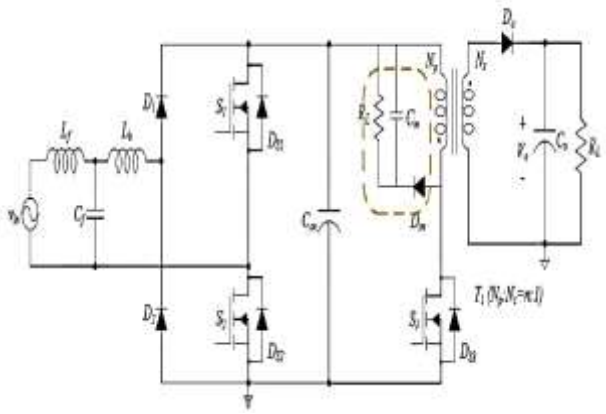

Fig 1 The two stage bridgeless boost integrated with Flyback PFC Converter

2. SINGLE STAGE BRIDGELESS-BOOST FLYBACK PFC CONVERTER

2.1 Topology

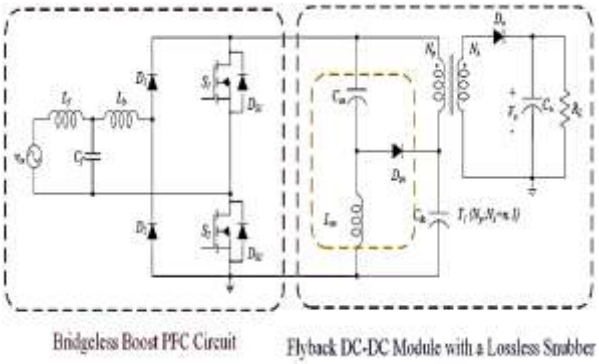

Fig 2(a) Bridgeless boost-Flyback PFC Converter with Snubber circuit

To achieve high power factor the input boost inductor L_b is operated in Discontinuous Conduction mode. And the coupled inductor of Flyback stage provide the input to output electrical isolation. The RMS current and switching loss during the turn on process are reduced by using valley switching. To reduce the high voltage spikes of the switches a lossless LCD Snubber circuit (L_{sn}, C_{sn} and D_{sn}) is used and another major advantage is the energy loss due to leakage inductor is reused by the Flyback circuit. Flyback circuit consist of coupled inductor T_1, output diode D_o and output capacitor C_o. The inductor's average voltage must be zero at the steady state, hence the voltage across the capacitors C_{sn} and C_{dc} is equal to V_{dc} as per the voltage -second balance law. The bulky dc-link capacitor is divided into two, one of which acts as Snubber capacitor and the other acts as dc-link Capacitor. In addition some input power is directly transferred to load without being stored in the dc-link Capacitor and the dc-capacitor stores the remaining power. Therefore capacitors with the low voltage rating can be used as dc-link capacitor thereby power transfer efficiency is improved and also the power factor is improved.

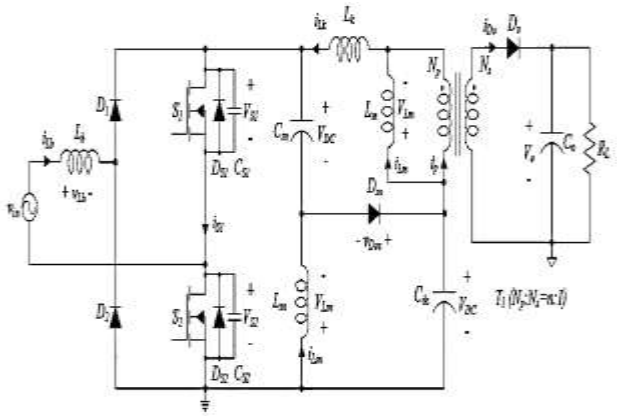

Fig 3(b) Equivalent Circuit of bridgeless boost-Flyback PFC Converter with Snubber circuit [5]

The fig 2(b) represents the equivalent circuit of the bridgeless boost-PFC Converter by considering the parasitic capacitors (C_{s1}, C_{s2}) of switches S_1 and S_2 respectively.

2.2 Operation of Converter

In this bridgeless boost-PFC Converter with Snubber circuit the same gating signal is used for both the switches S_1 and S_2. Due to the symmetry, the converter waveforms is shown for only one switching period i.e., during the positive half cycle of the input voltage. Fig 3(a) and fig 4 shows the theoretical operating modes and waveforms of the converter during the positive cycle of the input voltage and for one switching period T_s. The converter operation is divided into five modes. Before t_0, the current i_{Lb}, i_{Lm}, and i_{Lsn} are zero.

Mode 1 ($t_0 < t < t_1$): At t_0, both the switches S_1 and S_2 are turned on at same time. This instance is called zero voltage switching. Therefore there is a reduction in the turn-on switching losses. As the input boost inductor voltage V_{Lb} is equal to the supply voltage V_{in} and hence the boost inductor current i_{Lb} increases linearly.

$$iLb(t) = \frac{Vin}{Lb}(t - to).$$

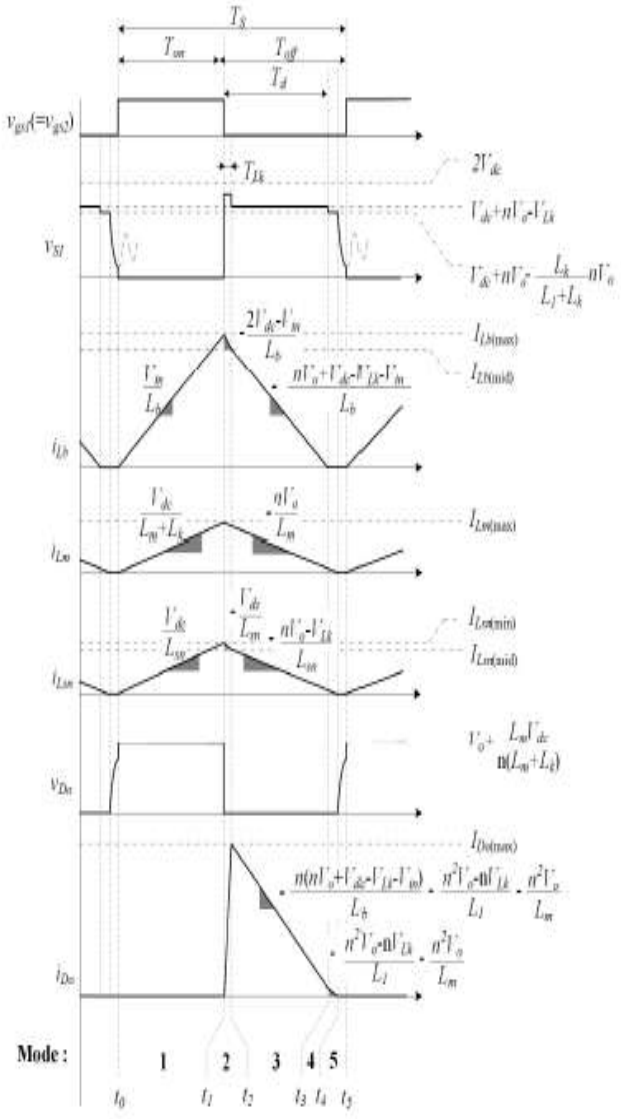

Fig 3(a) Waveforms of the bridgeless boost-Flyback PFC Converter [5]

Total voltage across both L_m and L_k is V_{dc}. Hence i_{Lm} increases linearly.

$$iLm(t) = \frac{Vdc}{Lm + Lk}(t - to).$$

The voltage across Snubber inductor $V_{Lsn}=V_{dc}$. Hence i_{Lsn} increases linearly.

$$iLsn(t) = \frac{Vdc}{Lsn}(t - to).$$

At the end of mode 1, the i_{Lb}, i_{Lm}, and i_{Lsn} reach the maximum value, these currents are as follows:

$$iLb(\max) = \frac{Vin}{Lb} Ton.$$

$$iLm(max) = \frac{Vdc}{Lm + Lk} Ton.$$

$$iLsn(max) = \frac{Vdc}{Lsn} Ton.$$

Where T_{on} turn-on time, it is the time between t_0 and t_1.

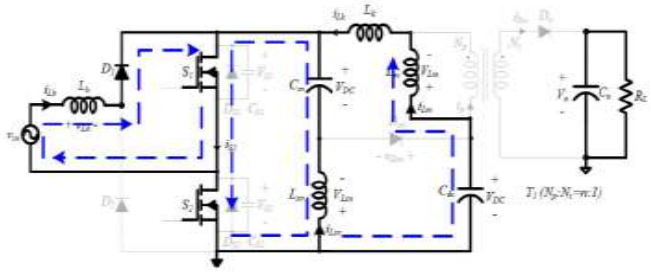

Fig 4(a) equivalent circuit for mode 1

Mode 2 ($t_1 < t < t_2$): At t_1, both switches S_1 and S_2 are turned off and the parasitic capacitor C_{S1} of the switch 1 begins to charge. Since parasitic capacitor C_{S1} is small, the time taken to charge is very less. The Snubber capacitor C_{sn} stores the leakage inductor energy through the Snubber diode D_{sn} during this mode. Hence, the voltage across the switch V_{S1} is equal to $2V_{dc}$. Since the boost inductor's voltage V_{Lb} is equal to – ($2V_{dc}$–V_{in}), the boost inductor's current i_{Lb} linearly decreases.

$$iLb(t) = iLb(\max) + \frac{-(2Vdc - Vin)}{Lb}(t - t1).$$

As the voltage across the magnetizing inductor V_{Lm} is -nV_o, the i_{Lm} decreases linearly.

$$iLm(t) = iLm(\max) + \frac{-nVo}{Lm}(t - t1).$$

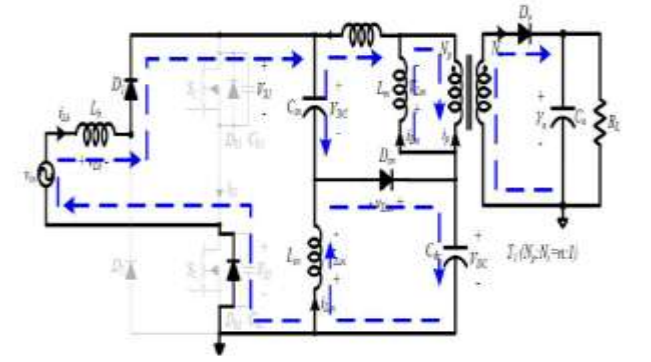

Fig 4(b) equivalent circuit for mode 2

During this mode, as the voltage across the Snubber inductor V_{Lsn} is –V_{dc}, the current in the Snubber inductor i_{Lsn} linearly decreases.

$$iLsn(t) = iLsn(\max) + \frac{-Vdc}{Lsn}(t - t1).$$

At the end of this mode the currents i_{Lb} and i_{Lsn} reach the middle or the minimum value.

$$iLb(mid) = iLb(\max) + \frac{-(2Vdc - Vin)}{Lb}(TLk).$$

$$iLm(mid) = iLm(\max) + \frac{-nVo}{Lm}(TLk).$$

Where T_{Lk} is the discharging time of the leakage inductor between t_1 and t_2.

During this mode the output diode Do is turned on, the current i_{Do} reaches the maximum value which is given by the below expression.

$$iDo(max) = n[\frac{-nVo}{Lm}TLk + \frac{(Vdc - nVd)}{Lk}TLk].$$

Mode 3 ($t_2 < t < t_3$): This mode begins when Dsn is turned off. In this mode, the voltages VLb, VLsn and VLk are given as:

$$VLb = -n(Vo + Vdc - VLk - Vin)$$

$$VLsn = nVo - VLk$$

$$VLk = Ls[\frac{nVoLb - (Vin - nVo - Vdc)Lsn}{Lb * Lsn}]$$

Where $\frac{1}{Ls} = \frac{1}{Lk} + \frac{1}{Lsn} + \frac{1}{Lb}$

The currents i_{Lb}, i_{Lm}, i_{Lsn} flows through the coupled inductor T_1 to the load side as the forward biased output diode D_o provide the path for the current flow.

$$iLb(t) = iLb(\text{mid}) + \frac{-n(Vo + Vdc - VLk - Vin)}{Lb}(t - t2)$$

$$iLsn(t) = iLsn(\text{mid}) + \frac{nVo - VLk}{Lsn}(t - t2).$$

The output diode current i_{Do} is given as:

$$iDo(t) = IDo(\max)+\text{n}$$
$$\{\frac{-n(Vo+Vdc-VLk-Vin)}{Lb} + \frac{nVo-VLk}{Lsn} + \frac{-nVo}{Lm}\}(t - t2)$$

The above equation shows that the the output diode D_o - current i_{Do} contains the boost inductor current i_{Lb} which flows through the coupled inductor T1 to the secondary side. Therefore, during this mode a part of input power is directly transferred to the load side.

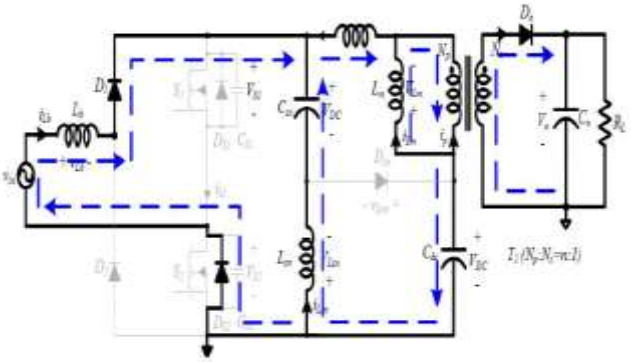

Fig 4(c) equivalent circuit for mode 3

Mode 4 ($t_3 < t < t_4$): At t3, the boost inductor current i_{Lb} reaches zero. The voltage across both the inductors L_{sn} and L_k is nV_o. The current i_{Lsn} is given as:

$$iLsn(t) = iLsn(t2) + \frac{nVo}{Lsn + Lk}(t - t3)$$

As the current i_{Lb} reached zero, the current in the output diode i_{Do} decreases linearly.

$$iDo(t) = IDo(t3) + n\{\frac{-(nVo - VLk)}{Lsn} + \frac{-nVo}{Lm}\}(t - t3)$$

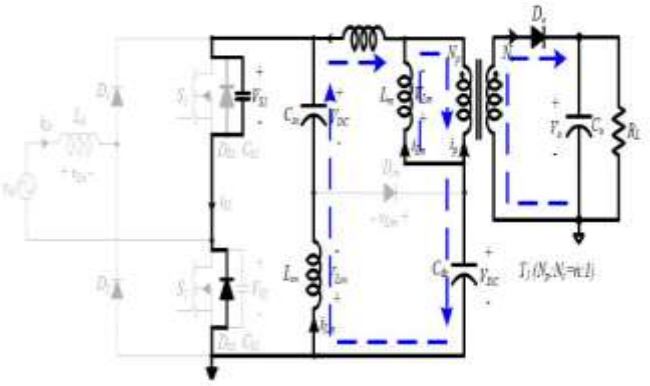

Fig 4(d) equivalent circuit for mode 4

Mode 5 ($t_4 < t < t_5$): This mode starts when output diode current i_{Do} reaches zero. Hence output diode is turned off under zero current switching (ZCS) condition. V_{s1} nonlinearly decreases and oscillates between C_{S1} and $(L_m+L_k)//L_{sn}$.

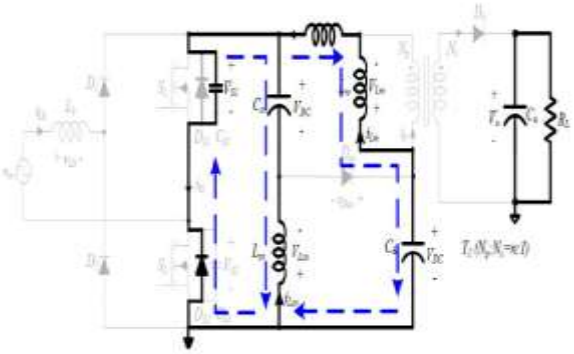

Figure 4(e) equivalent circuit for mode 5

2.3 Design Consideration [5]

i. Input Current and Power Factor

The input voltage is sinusoidal hence represented as $V_{in}(wt)=V_{in.\,pk}\sin(2\pi f_L.t)$

Where f_L is the line frequency. $V_{in.\,pk}$ is the peak input voltage.

Time taken by the boost inductor to discharge is the discharging time T_d is given as $Td=\frac{Vin(wt)}{nVo+Vdc-Vin(wt)}DTs$

Duty cycle, $D=\frac{Ton}{Ts}=\frac{nV0}{nV0+Vdc}$

The maximum magnetizing inductor current is $I_{Lm(max)} = \frac{Vdc}{Lm}T_{on} = \frac{nVo}{Lm}T_{off}$

The average of the input inductor current is the input current given as:

$$I_{in}(wt)=I_{Lb.avg}(wt)= I_{Lb.on(avg)} + I_{Lb.off(avg)}$$

$$= \frac{ILb.pk(wt)}{2} * \frac{Ton+Td}{Ts}$$

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} v_{in}(\omega t) i_{in}(\omega t)\,dt$$

$$\alpha = \frac{nV0}{nV0+Vdc}$$

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_{in}^2(\omega t)\,dt}$$

$$= \frac{nV_oD}{2L_bf_s}\sqrt{\left\{1+\frac{2\alpha}{\pi(1-\alpha^2)}+\frac{2\alpha(2\alpha^2-1)}{\pi(1-\alpha^2)\sqrt{1-\alpha^2}}\left[\frac{\pi}{2}-\tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}}\right)\right]\right\}}$$

$$PF = \frac{P_{in}}{V_{rms}I_{rms}}$$

Where V_{rms} and I_{rms} are the input RMS voltage and RMS current respectively.

ii. Voltage of the DC-bus and Output current

$$I_o = i_{Do(avg)}(t)$$

$$= \frac{1}{\pi}\int_0^{\pi} n(i_{Lb.d(avg)} + i_{Lsn.off(avg)} + i_{Lm.off(avg)})dt$$

$$= \frac{n^2 V_o D}{L_b f_s}\left\{\frac{\alpha}{\pi}-\frac{1}{2}+\frac{1}{\pi\sqrt{1-\alpha^2}}\left[\frac{\pi}{2}-\tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}}\right)\right]\right\}$$

$$+\frac{n^2 V_o L_e}{2}(1-D)^2 T_s$$

$$V_{dc} = \frac{2V_{in.pk}L_e}{L_b}\left\{\frac{2}{\pi}-\frac{1}{\alpha}+\frac{2}{\pi\alpha\sqrt{1-\alpha^2}}\left[\frac{\pi}{2}-\tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}}\right)\right]\right\}.$$

Where $\frac{1}{Le} = \frac{1}{Lsn} + \frac{1}{Lm}$

iii. Design of inductors L_b, L_m and L_{sn}

$$L_b = \frac{V_{in.pk}{}^2 D^2}{2\pi P_o f_s}\int_0^{\pi}\frac{\sin^2(\omega t)}{1-\alpha\left|\sin(\omega t)\right|}dt$$

$$L_e = \frac{L_b V_{dc}}{V_{in.pk}\left\{\frac{4}{\pi}-\frac{2}{\alpha}+\frac{4}{\pi\alpha\sqrt{1-\alpha^2}}\left[\frac{\pi}{2}-\tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}}\right)\right]\right\}}$$

iv. Output power and directly transferred input power

$$P_{out} = V_o I_o$$

$$= \frac{n^3 V_o{}^2 \alpha}{L_b f_s}\left\{\frac{\alpha}{\pi}-\frac{1}{2}+\frac{1}{\pi\sqrt{1-\alpha^2}}\left[\frac{\pi}{2}-\tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}}\right)\right]\right\}+\frac{L_e V_{dc}{}^2}{4}D^2 T_s.$$

$$P_{direct} = P_{out} - \frac{L_e V_{dc}{}^2}{4}D^2 T_s.$$

v. Voltage stress of devices

In the proposed converter, the maximum voltage of S1, S2, D1 and D2 is clamped by 2Vdc. In addition, the voltage stress of Snubber diode Dsn is 2Vdc. In addition, the voltage stress of Snubber diode D_{sn} is 2Vdc. The voltage stress of output diode Do is Vo+ V_{dc}/n.

3. STATE SPACE ANALYSIS

The state space analysis is the method of modelling the physical system mathematically. It relates the input, output and the state space variables using the differential equations. These differential and algebraic equations are written down in the form of the matrix.

The general form of the state space equations is represented as shown below:

$$\dot{\mathbf{x}}(t) = A(t)\mathbf{x}(t) + B(t)\mathbf{u}(t)$$
$$\mathbf{y}(t) = C(t)\mathbf{x}(t) + D(t)\mathbf{u}(t)$$

Case 1: when both switches S_1 and S_2 are on:

There are five energy storing elements in the circuit. They are two capacitive and three inductive elements C_{dc}, C_{sn}, L_b, L_m+ L_k and L_{sn} and are assumed with the state variables. The current through the inductors L_b, L_{sn} and L_m+ L_k are i1, i2, i3 and are represented by state variables x1, x2 and x3 respectively.

And voltages across capacitors C_{sn} and C_{dc} is V1 and V2 are represented by state variables x4 and x5 respectively.

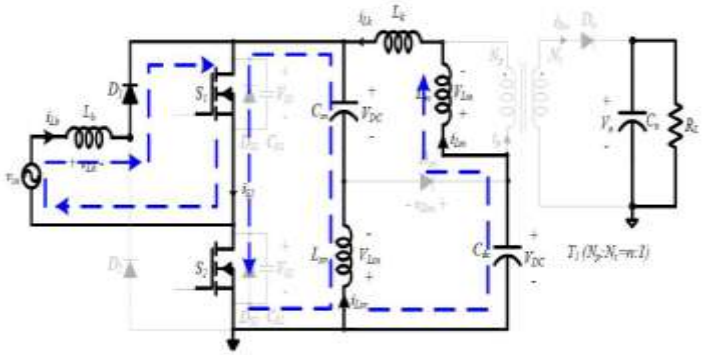

Fig. 5(a) Equivalent circuit when both S_1 and S_2 are on

Assume x1=i1 , x2= i2, x3=i3, x4=v1 and x5=v2

$$Vin = Lb\frac{di1}{dt}$$

$$u = Lb\,x'1 \qquad (1)$$

$$V1 + Lsn\frac{di2}{dt} = 0$$

$$x'2 = -\frac{x4}{Lsn} \qquad (2)$$

$$V2 + (Lm + Lk)\frac{di3}{dt} = 0$$

$$x'3 = -\frac{x5}{Lm+Lk} \qquad (3)$$

$$x'4 = \frac{x2}{Csn} \qquad (4)$$

$$x'5 = \frac{x3}{Cdc} \qquad (5)$$

Y=0

Equation (1) to (5) are written in the matrix form as given below

$$\begin{bmatrix} x'1 \\ x'2 \\ x'3 \\ x'4 \\ x'5 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{Lsn} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{Lm+Lk} \\ 0 & \frac{1}{Csn} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{Cdc} & 0 & 0 \end{bmatrix} \begin{bmatrix} x1 \\ x2 \\ x3 \\ x4 \\ x5 \end{bmatrix} + \begin{bmatrix} \frac{1}{Lb} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u$$

Comparing this equation with the standard state space equation

$$A1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{Lsn} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{Lm+Lk} \\ 0 & \frac{1}{Csn} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{Cdc} & 0 & 0 \end{bmatrix} \quad \text{and} \quad B1 = \begin{bmatrix} \frac{1}{Lb} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Case 2: when both switches S_1 and S_2 are off:

Assume x1=i1, x2= i2, x3=i3, x4=v1 and x5=v2

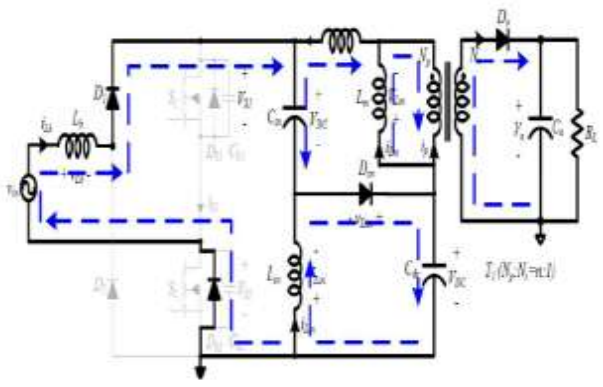

Fig. 5(b) Equivalent circuit when both S_1 and S_2 are off

Comparing this equation with the standard state space equation

$$A2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{Lsn} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{Lm+Lk} \\ 0 & \frac{1}{Csn} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{Cdc} & 0 & 0 \end{bmatrix} \quad \text{and} \quad B2 = \begin{bmatrix} \frac{1}{Lb} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$y = Rl(x1 - x2 - x3) \qquad (11)$$

$$y = [Rl \quad -Rl \quad -Rl \quad 0 \quad 0] \begin{bmatrix} x1 \\ x2 \\ x3 \\ x4 \\ x5 \end{bmatrix} + 0$$

A= A1*D+A2*(1-D)

D=0.5, Therefore A= A1*0.5+A2*(1-0.5) =A1

Similarly B=B1,

$$C=0.5*C1=[0.5Rl \quad -0.5Rl \quad -0.5Rl \quad 0 \quad 0]$$

Transfer function is given by= C [SI-A]' B+D

Inverse of [SI-A] is found by Gauss Jordan Elimination Method

Transfer Function=

$$\frac{C(S)}{R(S)} = \frac{3.18S^5 - 243.9S^4 + 0.0000045865S^3 - 3.185S^2 + 81.3S + 56400000}{3.18S^5 - 81.311S^4 + 0.0000045865S^3}$$

By using the MATLAB environment the bode plot of the system is found to be

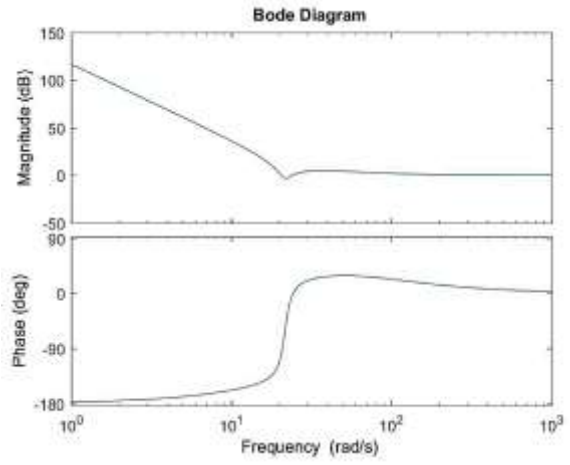

Fig. 6(a) Bode plot of the system

[Gm,Pm,Wg,Wpc]=margin (sys)

>> Gm = 2.9903 Pm = 77.2445

Wg = 0.0012 Wpc =20.4093

As both the gain margin and phase margin are positive the closed loop system hence designed is stable.

4. SIMULATION AND RESULS

1) SIMULINK MODELLING-OPEN LOOP

The Simulink model of the open loop of the single stage bridgeless boost-Flyback Converter with the Snubber circuit is shown in the figure 7(a).

Table 4.1 Components and parameters

Parameter/Components	Values
Input voltage, $V_{in(peak)}$	$90*\sqrt{2}$ V, 50 Hz
Switching frequency	60 KHz
Boost inductor, L_b	510 µH
Snubber inductor, L_{sn}	1.2 mH
Output voltage, V_o	54 V
Output load, watts	80 W

Table 4.1 shows the components and its ratings used in the simulation work.

The open loop simulation of the converter is performed and results are verified on an output 54V and 80W model.

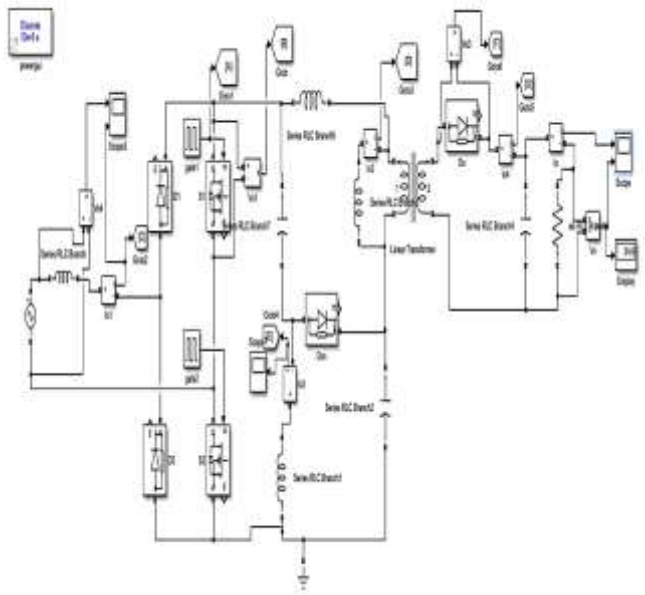

Fig. 7(a) Open loop Simulink model of bridgeless boost-Flyback PFC Converter with Snubber circuit

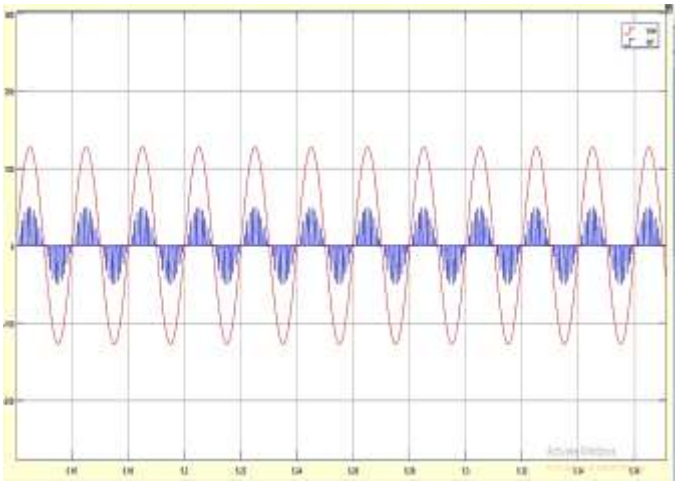

Fig. 7(b) Input current and voltage

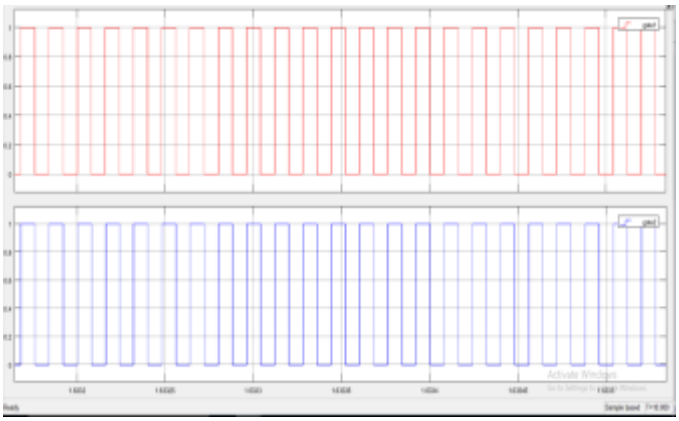

Fig. 7(c) Gating pulses for switch 1 and 2

It is seen that the input current and voltage are almost in phase from the figure 7(b) .The power factor is observed to be nearly unity.

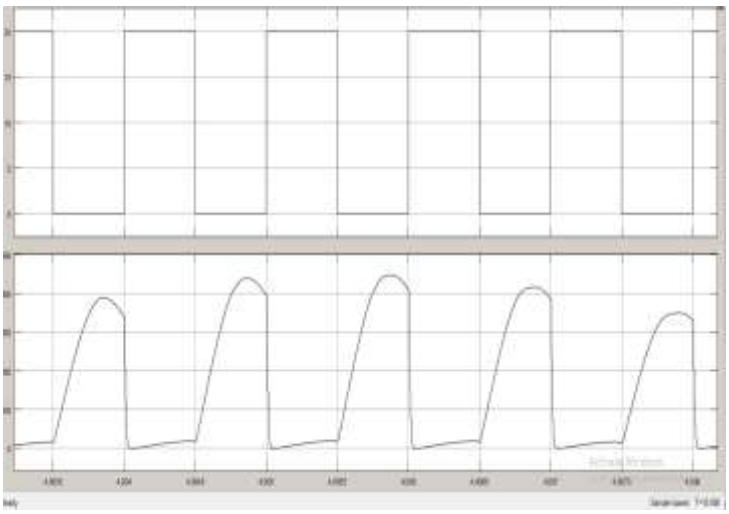

Fig. 7(d) Gating pulse and voltage across the switch 1

Figure 7(c) shows the gating pulses generated using the pulse generator with switching frequency of 60 KHz hence

with a time period T=16 μsec and considering the duty cycle D=0.5.

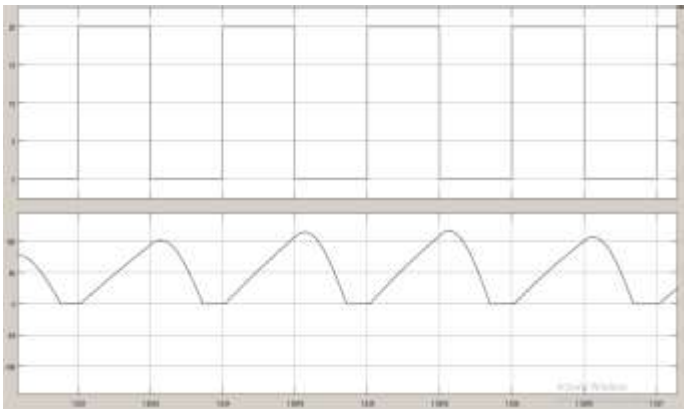

Fig. 7(e) Gating pulse and current in boost inductor i_{LB}

As shown in the figure 7(e) the input boost inductor current is not continuous because the input inductor is operated in discontinuous mode to improve the power factor.

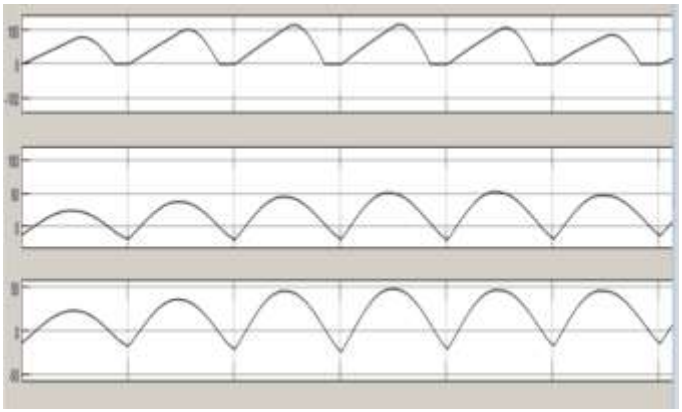

Fig. 7(f) Inductor currents i_{Lb}, i_{Lm} and i_{Lk}

From figure 7(f) it is seen that the inductor currents i_{Lm} and i_{Lk} are continuous unlike the current i_{Lb}.

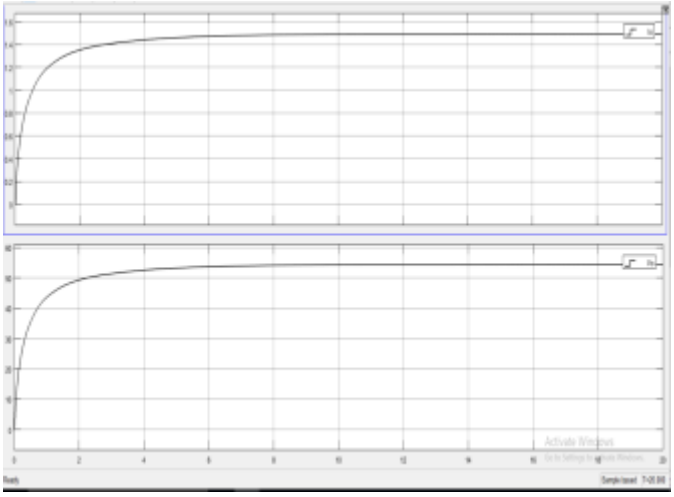

Fig. 7(g) Output current and voltage

2) SIMULINK MODELLING- CLOSED LOOP

The Simulink model of the closed loop of the single stage bridgeless boost-Flyback Converter circuit is shown in the figure 8(a).

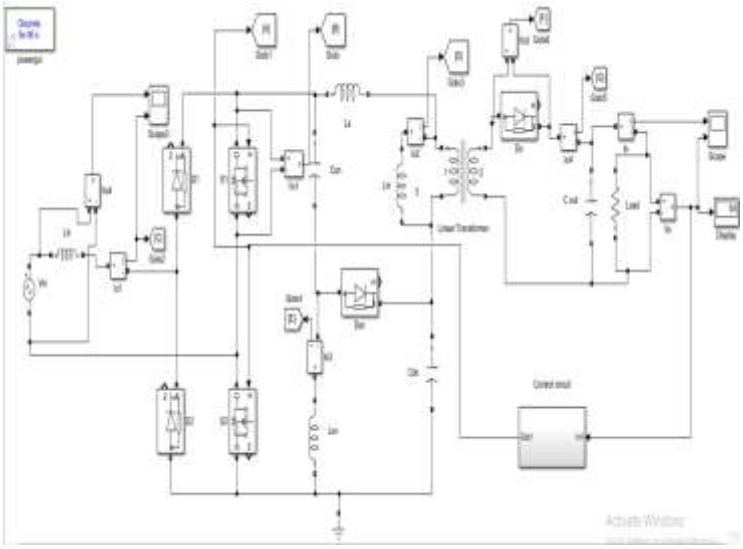

Fig. 8(a) Closed loop Simulink model of bridgeless boost-Flyback PFC Converter with Snubber circuit

The closed loop is designed by comparing the feedback signal with the reference and then error thus obtained is fed to the PI controller and compared with the repeating sequence to generate the pulses as shown in the figure 8(c). The control constants Kp, Ki are obtained by tuning the step response of the system using the PID tuner of the MATLAB.

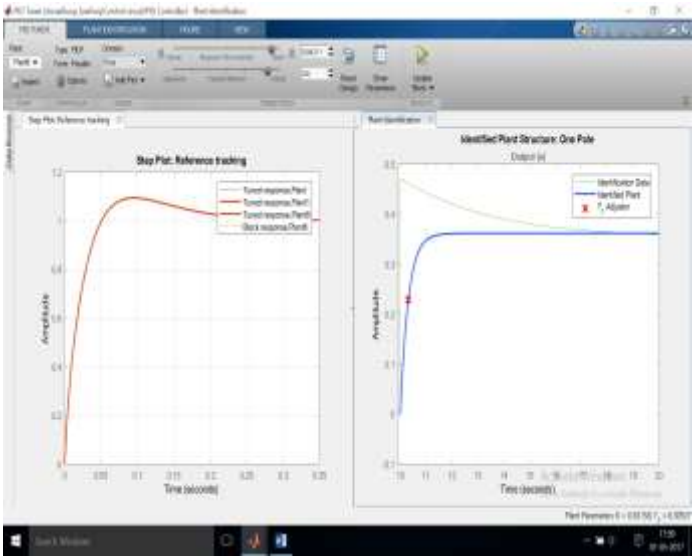

Fig. 8(b) Step response of the plant for Tuning of PI Controller

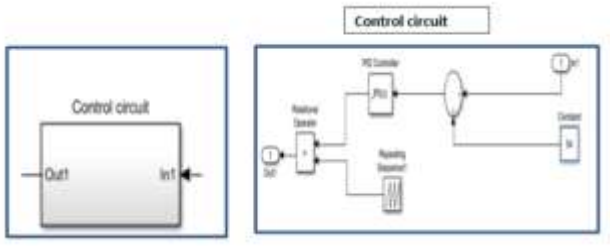

Fig. 8(b) Control circuit in the closed loop system

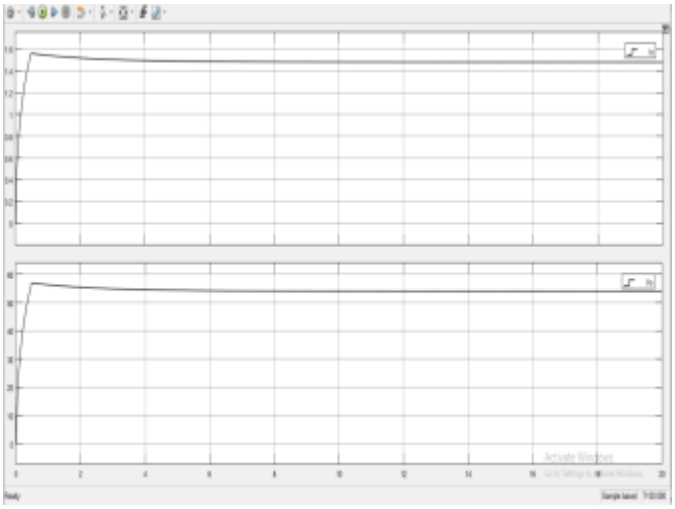

Fig. 8(c**)** Output response of current and voltage

From the figure 8(c) it is seen that the output voltage and current are in the transient state initially for about 1second and later the system achieves the steady state thus maintain the constant voltage.

From the simulation the output voltage is observed to be constant and V_{out}= 54.62V

$$power\ factor, pf = \frac{P_{in}}{V_{rms} * i_{rms}} == 0.9905681$$

5. CONCLUSION

A single stage bridgeless boost Flyback PFC converter along with Snubber circuit is designed and Simulated in this project. An input full bridge of the diodes is removed in the rectifier circuit thereby reducing the conduction losses. A Flyback circuit is used as the DC-DC voltage regulator which even provide the electrical isolation. High power factor nearly equal to unity is achieved by operating the PFC converter in the discontinuous mode. In addition to this, the LCD Snubber circuit is employed to reduce the voltage spikes of the switches during turn-on and also the leakage inductor energy is reused. The single DC capacitor is split into two, among which one is used as Snubber capacitor and also a part of the input power is transferred to the output end directly without the interference of the DC-link capacitor. Therefore Dc-link capacitor with the low voltage rating can be used. Hence the power transfer efficiency is improved.

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