International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 07 | July 2019 www.irjet.net p-ISSN: 2395-0072

Performance Evalution of Gate Diffusion Input and Modified Gate Diffusion Input Techniques for Multipliers and Fast Adders design

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Abstract - *Power consumption is the bottle neck of system performance in VLSI design. Minimization of power consumed by the circuit tends to improve the performance and reduce the cost of the system. Power consumption is mainly due to increased number of transistors and leakage power. The reduction of transistor count and leakage power is done by using techniques like "Gate diffusion input"(GDI) and "Modified gate diffusion input"(MGDI). Multipliers are vital components of any processor (or) computing machine. Performance of microcontrollers and digital signal processors are evaluated on the basis of number of multiplications performed in unit time. Moreover the speed of any digital system heavily depends on the fast adders. Hence, better multipliers and fast adders architectures are bound to increase the efficiency of the system. In this project, fast adders and multipliers design is proposed for low area and power consumption using GDI and modified GDI techniques. The simulated results are expected to obtain in micro-wind. The comparisons are to be made in terms of transistor count and power consumption using GDI and modified GDI techniques as well. The total architecture is designed CMOS technology using micro-wind.*

Keywords— CMOS technique, GDI technique, modified GDI technique, low power consumption, micro-wind.

1. INTRODUCTION

Electronics as we know today is characterized by reliability, low power dissipation, extremely low weight and volume, and low cost, coupled with an ability to cope easily with high degree of sophistication and complexity.[1]

MULTIPLIER is an electronic circuit used extensively in modern processors. It is building block of many high speed systems such as 'Digital signal processor'. The performance of any digital system is mainly evaluated by performance of the multiplier and fast adder. Present processor aim is to design low power multiplier and adder. Therefore power consumption and dissipation of multiplier and adder should be minimized. Power dissipation in a CMOS circuit is determined by two components.

1) Static power dissipation , 2) Dynamic power dissipation

Static power dissipation becomes an issue when the circuit is inactive mode or in a power down mode. Dynamic power dissipation occurs when the circuit is in operation mode, i.e. the circuit performing some task.[1]

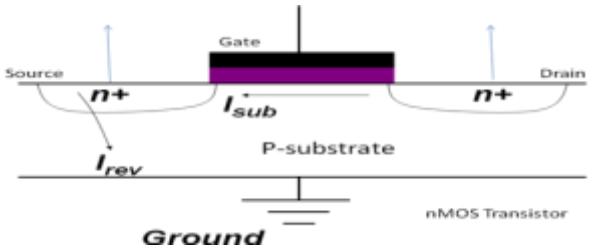


Fig-1: leakage power components in NMOS transistor

The static power components become important when the circuits are rest, i.e. when there is no activity in the circuits. It is defined as product of supply voltage and leakage Current. The static power dissipation includes Sub-threshold leakage current and Reverse biased diode leakage current. Sub-threshold leakage current has a strong dependence on the threshold voltage. It is the current between source and drain of the MOSFET when transistor is in sub-threshold region or weak- inversion region, that is, gate to source voltage is below the threshold voltage of device. The reverse bias diode leakage is due to the reverse bias current in the parasitic diodes that are formed between diffusion region of transistor and substrate. It results from minority charge carriers and drifts near the edge of the depletion regions, and also form the generation of electron hole pairs in the depletion regions of reverse bias junctions.[2]

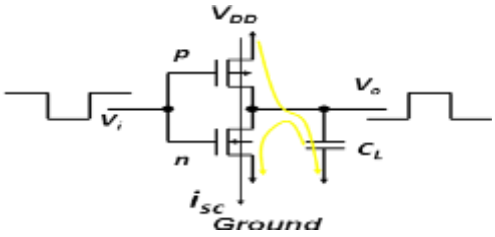


Fig-2: Dynamic power dissipation in CMOS inverter

Dynamic power dissipation can be divided into three mechanisms: switched, short circuit and glitch power dissipation. Switched power dissipation comes due to repeated charging and discharging of output capacitor. Short circuit dissipation is occur in a circuit when, both PMOS and NMOS transistors are 'ON'. In real circuits signals have non-zero rise and fall times, which causes both P-net and N-net of CMOS gate to conduct current simultaneously. This leads to the flow of a short circuit current for a short period of time.

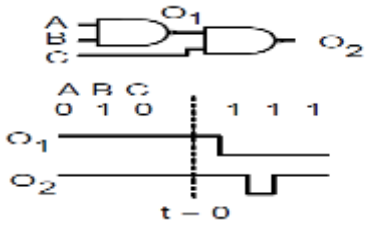


Fig-3: example for glitch power dissipation

Glitches are undesired transitions which do not contribute any useful information. In digital circuits glitch is occur before the signal settles to its intended value. In other words glitch is an electrical pulse of short duration that is usually the result of a fault or design error. As shown in fig 3, there is some delay at the output O1, which results in glitch at output O2. As there is some capacitance associated with the output O2, it leads to switching power dissipation. However glitch can be minimized by scale down the supply and threshold voltages probably at different phases.

GATE DIFFUSION INPUT is the VLSI technique to reduce the dynamic and static power dissipation in digital circuits. By using this technique various digital circuits can be designed with low transistor count as compare to CMOS designs which results in low power dissipation.

2. GATE DIFFUSION INPUT TECHNIQUE

Gate diffusion input technique is named itself because of one of the inputs are directly diffused into the gates of NMOS and PMOS transistors. GDI reduces power dissipation and area of digital circuits. This method is based on the simple cell which looks exactly like basic inverter. It is shown in fig 4.

The GDI cell contains 3 inputs.

1) G (Common input to the gate of PMOS and NMOS)

2) N (input to the source/drain of NMOS)

3) P (input to the source/drain of PMOS)

In GDI technique N,P,G terminals are could be given to a power supply 'Vdd' or can be grounded or can be supplied with input signal depending upon the circuit to be designed and hence effectively minimizing the number of transistors used in case of most logic circuits (eg. AND, OR, NOT, XOR, etc). Bulks of PMOS and NMOS are connected to the 'P' or 'N' terminals respectively.

2.1 Basic Logic Functions

The implementation of different logic functions using GDI technique are as follows.

Table-1: Basic GDI CELL FUNCTIONS

TABLE I
FUNCTIONS THAT CAN BE IMPLEMENTED USING BASIC GDI CELL

N	P	G	Out	Function
0	1	A	A'	INVERTER
0	B	A	A'B	FUNCTION1
B	1	A	A'+B	FUNCTION 2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
B'	B	A	A'B+B'A	XOR
B	B'	A	AB+A'B'	XNOR

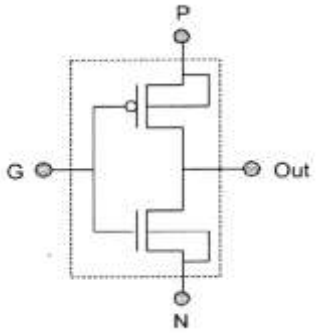


Fig-4: BASIC GDI CELL

The TABLE 1 shows information about the logic functions which are implemented by using GDI technique. So any logic function can be implemented with GDI technique.

The operation of GDI technique based two input AND gate can be explained with respect to basic GDI cell, 'P' of the transistor is given to the ground, it will cut-off from its operation, hence the logic either '1' or '0' at the input 'a' will be reflected at the output. Thus the output will be a*b.[3]

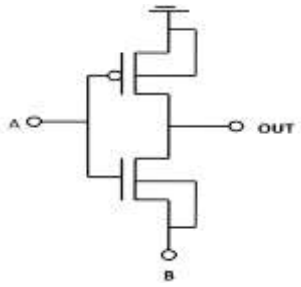


Fig-5: GDI AND GATE

To obtain the two input OR logic using GDI cell, both the inputs are given to the 'G' and 'P' terminals and power supply is given to the terminal 'N'. Thus, output will be 'A+B'.

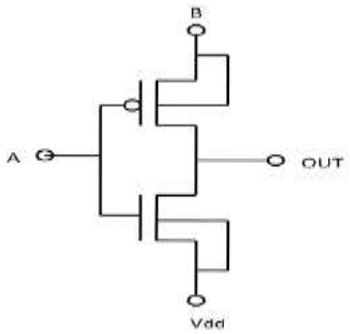


Fig-6: GDI OR GATE

To obtain the inverter logic using GDI cell, 'P' terminal is connected to the logic '1'; 'G' terminal is connected to the input 'A' and terminal 'N' is connected to the ground. Thus the output will be A'.

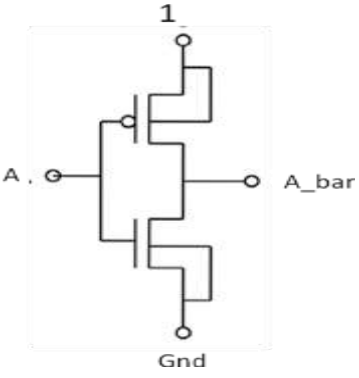


Fig-7: GDI INVERTER

To obtain the two input XOR logic using GDI cell, one input 'A' is given to the terminal 'G', second input 'B' is given to the terminal 'P', and for terminal 'N', complement of 'B' is given. Thus the output will be (A'B+AB') .

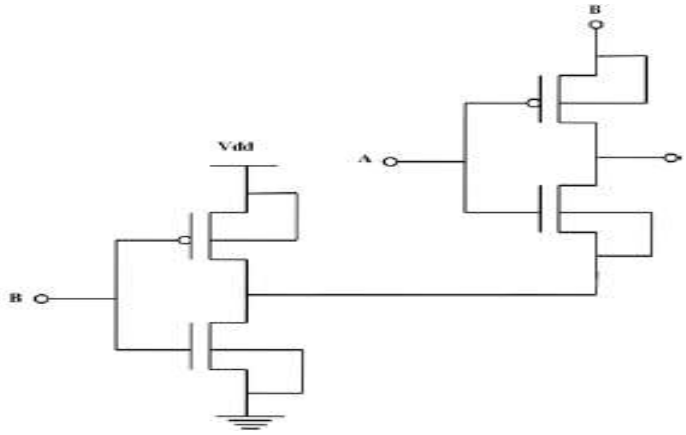


Fig-8: GDI XOR

2.2 ADDERS

By using GDI XOR and GDI AND gates we can design GDI half adder as shown in fig 9.[4]

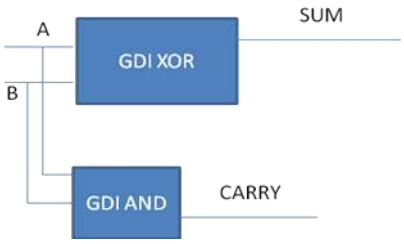


Fig-9: GDI HALF ADDER

Low power 6 transistor GDI full adders are obtained from sum and carry expressions of full adder as follows.

$$sum = (a \oplus b) \oplus c$$
$$\Rightarrow (a \oplus b)c' + (a \oplus b)'c$$
$$carry = ab + bc + ca$$
$$\Rightarrow (a \oplus b)'a + (a \oplus b)c$$

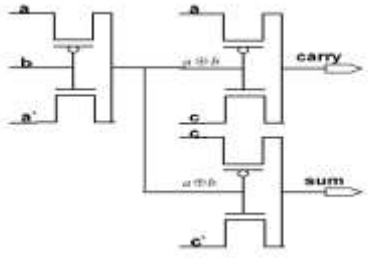


Fig-10: 6 TRANSISTOR GDI FULL ADDER

By using the logic functions based on GDI technique, we can design multiplier with low power consumption.

3. MODIFIED GATE DIFFUSION INPUT TECHNIQUE

MGDI is a new technique for designing low power digital circuits. This technique is adopted from GDI technique.

MGDI technique is used to reduce power dissipation, transistor count and area of digital circuits. MGDI also consists of three input terminals - G, (input of both PMOS and NMOS) P, (input to drain/source of PMOS) and N (input to drain /source of NMOS) except the bulks of PMOS (SP) and NMOS (SN) are constantly coupled to VDD and GND, respectively.[5]

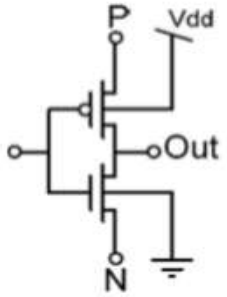


Fig-2: Basic MGDI cell

MGDI overcomes the drawbacks of GDI cell.

In this technique the substrate terminals (P bulk & N bulk)are permanently tied to VDD and GND. Therefore the advantages of Modified GDI are [2]:

1. The variation in threshold drop is overcome.

2. This configuration provides suitability for fabricating the logic cells in CMOS n-well and p-well process.

3. Except for inverter, function F1 and F2 remaining logic functions implemented with gate input, which reduces the static power dissipation shown in Table 2.

4. Improves the logic swing adding some more transistors, like NMOS for getting strong logic „0" and PMOS for strong logic „1". [7]

On varying the values of G, P, N, SP and SN in MGDI cell, SP and SN will remain constantly coupled to VDD and GND various functions are obtained, shown in the following table .

Table -2: Miscellaneous functions using MGDI cell

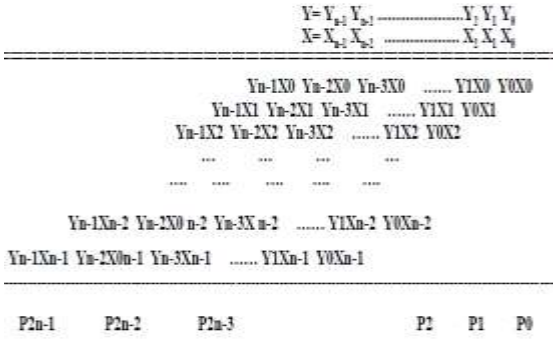
N	S_N	P	S_P	G	D	FUNCTION
0	0	1	1	A	A'	INVERTER
A	A	0	A	B	AB	AND
1	0	A	D	B	A+B	OR
A'	0	A	1	B	A'B+AB'	XOR
A	0	A'	1	B	AB+A'B'	XNOR
0	0	B	B	A	A'B	F 1
B	0	1	1	A	A'+B	F 2
C	0	B	1	A	A'B+AC	MUX

From table-2, it is noticed that different logic styles can be designed using one MGDI cell. OR gate and AND gate is designed using two transistors only, while in conventional CMOS it requires 6 transistors. The main advantage of MGDI technique is that it reduces transistor counts and area on chip that's cause of low power consumptions. So it is easy to design complex circuits using MGDI technique.

4. MULTIPLIER

Multiplication is one of the basic functions used in various VLSI applications. The multipliers are widely used in arithmetic logic unit, DSP processors, math processors, etc. digital multiplication is series of bit shifts and bit additions, where two numbers, the multiplicand and the multiplier are combined into a result. Considering the bit representation of the multiplicand Y0, Y1, Y2.....Yn-1 and the multiplier X0, X1, X2 ...Xn-1, in order to form the product, up to 'n' shifted copies of the multiplicand is to be added for unsigned multiplication.

The multiplication algorithm for N bit multiplicand by N bit multiplier is shown below.



In this paper we are presenting 2 multiplier approaches. They are,

1) Array multiplier

2) Tree multiplier

3.1 Array Multiplier

Array multiplier is well known due to its regular structure. The array topology is a two dimensional structure, that fits nicely on the VLSI planar process. 4-bit array multiplier architecture is shown in fig 11. It uses short wires that go from one full adder to adjacent full adder horizontally, vertically, or diagonally. For N-bit array multiplier, 'NxN' array of AND gates can compute all the partial product terms simultaneously.

The terms are summed by an array of 'N[N-2]' full adders and 'N' half adders. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic. The number of rows in array multiplier denotes the length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders. The advantage of array multiplier is comes from its regular structure. Since it is regular, it is easy to layout and has a small size.

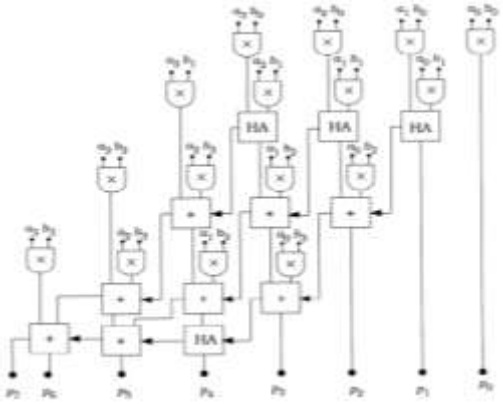


Fig-11: 4-BIT ARRAY MULTIPLIER ARCHITECTURE

The design time of array multiplier is much less than that of a tree multiplier. The limitation of array multiplier is that they are very large. As operand size increase, linear array grows in size at a rate equal to the square of operand size. This is because number of rows in array multiplier is equal to the length of the multiplier, with the width of each row equal to width of multiplicand. The large size of full arrays typically prohibits their use, except for small operand sizes, or on special purpose math chips where a major portion of silicon area can be assigned to the multiplier array.

4.2 Tree Multiplier

The first tree multiplier was introduced by C.S.WALLACE. He suggested a fast technique to perform multiplication in 1964. Tree multiplier is an extremely fast structure for summing partial products. In linear array each row sums one additional partial product. Such linear arrays require order 'N' stages to reduce 'N' partial products. In contrast by doing the additions in parallel, tree structure requires only order of 'log N' stages to reduce 'N' partial products. The result of multiplication is obtained by first generating partial products and then adding the partial products.

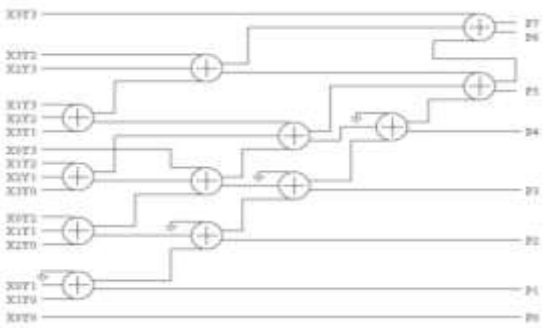


Fig-12: 4-BIT TREE MULTIPLIER ARCHITECTURE

In tree multiplier partial-sum adders are arranged in a tree like fashion, reducing both the critical path and number of adders needed as shown in fig 12 .

5 .FAST ADDER

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that Cin = 0).[7]

The layout of a ripple-carry adder is simple, as shown in Fig 13 which allows for fast design time.

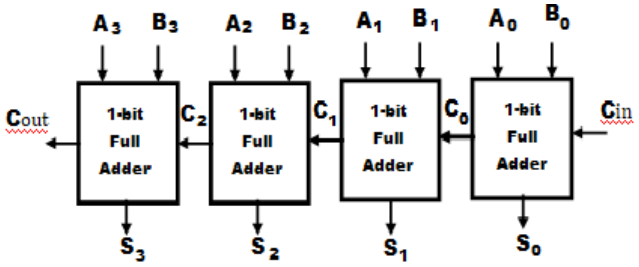


Fig-13 : 4-BIT RIPPLE CARRY ADDER

However, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. [8]

5.1 Carry Select Adder

In electronics, a **carry-select adder** shown in Fig 14 is a particular way to implement an adder, which is a logic element that computes the (n+1) -bit sum of two n-bit numbers. [8][10]

5.2.1 Construction

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry-in is known.[11]

The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs for a block size of $[\sqrt{n}]$. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The $O(\sqrt{n})$ delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays.

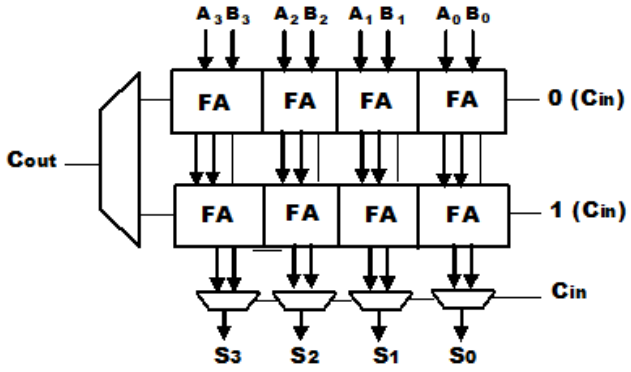


Fig-14: 4-BIT CARRY SELECT ADDER

Above is the basic building block of a carry-select adder, where the block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.

5.2 Carry Save Adder

A carry-save adder is a type of digital adder shown in Fig 15, used in computer micro architecture to compute the sum of three or more n-bit numbers in binary. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits.[9]

Carry save adder used to perform 3 bit addition at once. Here 3 bit input (A, B, C) is processed and converted to 2 bit output (S, C) at first stage. At first stage result carry is not propagated through addition operation. In order to generate carry, implemented ripple carry adder on stage 2 for carry propagation. [10]

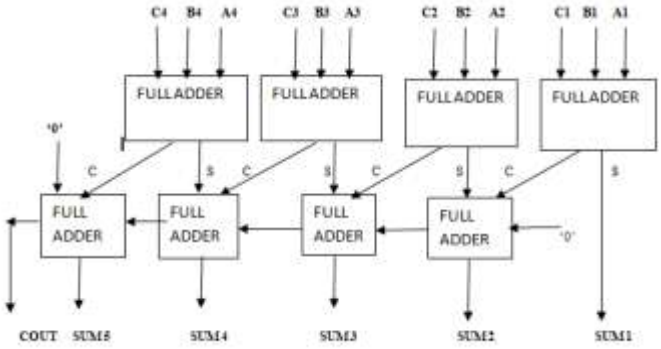


Fig 15: 4-bit CARRY SAVE ADDER

5.2.1 Implementation

Consider the sum:

5 6 7 8

\+ 4 3 2 2

= 1 0 0 0 0

Using basic arithmetic, we calculate right to left, "8+2=0, carry 1", "7+2+1=0, carry 1", "6+3+1=0, carry 1", and so on to the end of the sum. Although we know the last digit of the result at once, we cannot know the first digit until we have gone through every digit in the calculation, passing the carry from each digit to the one on its left. Thus adding two n-digit numbers has to take a time proportional to n. In electronic terms, using bits (binary digits), this means that even if we have n one-bit adders at our disposal, we still have to allow a time proportional to n to allow a possible carry to propagate from one end of the number to the other. The

schematic diagram for 4-bit carry save adder is shown in Fig 15.

Until we have done this,

1.We do not know the result of the addition.

2.We do not know whether the result of the addition is larger or smaller than a given number (for instance, we do not know whether it is positive or negative).

Carry Save Adder performs Addition of 3 (A, B, C) 4-bit values and output 5 bit Sum and Cout. Example result (1100 + 1101 + 1110) = 100111 (MSB Bit '1' Cout , Sum 5 bit " 00111").

6. MICROWIND

MICROWIND software comes from Toulouse, France, dedicated to provide innovative EDA solutions to the mixed-signal IC market.With our up to date MICROWIND layout tool and design methodologies one can transfer product ideas into highly integrated ASIC and IC solutions.

MICROWIND software tool is the industry's most comprehensive package dedicated to microelectronics and nanotechnology; deep-technology business of ASIC and custom IC design and simulation, as well as the latest in electronic design automation design. Technically speaking, the MICROWIND is a comprehensive solution for designing and simulating microelectronic circuits at layout level with different modules for layout designs in nm scale, schematic editor, mixed signal and analog simulator, memory simulator, real-time 3D display of the atomic structure of silicon and virtual fabrication process in 3-D view, verilog and SPICE support combined in one package.

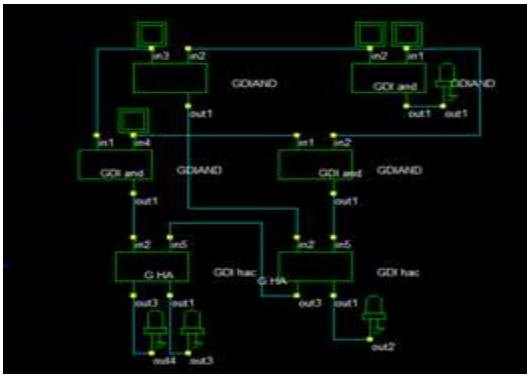
6.1 DSCH

The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures.

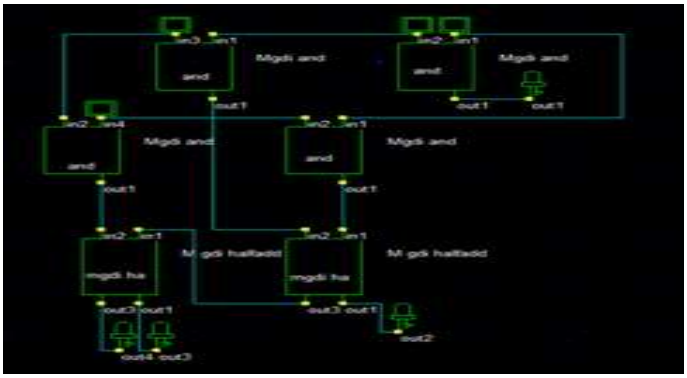
7. SCHEMATICS

Schematics for GDI and MGDI techniques based different logic functions ,4-Bit Array and Tree multipliers ,Ripple carry adder, Carry select adder and carry save adder architectures are designed in CMOS technology in MICROWIND. This is a powerful tool that allows the user to design circuits and simulate them. Designs are extensively used in industry and research. MICROWIND consists of several programs for different applications such as schematic drawing, layout, verification, and simulation. These applications can be used on various computer platforms.

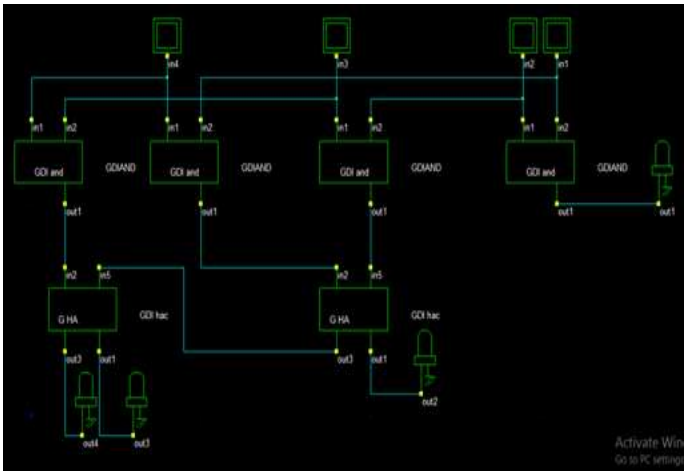
7.1 GDI ARRAY MULTIPLIER



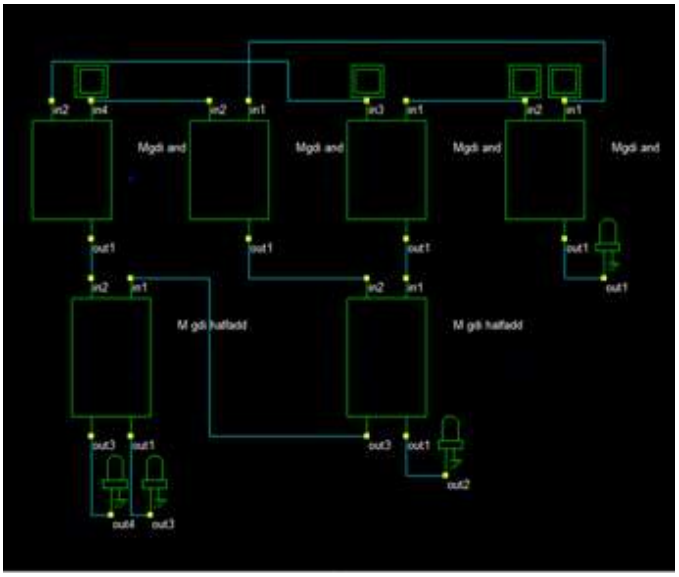
7.2 MGDI ARRAY MULTIPLIER



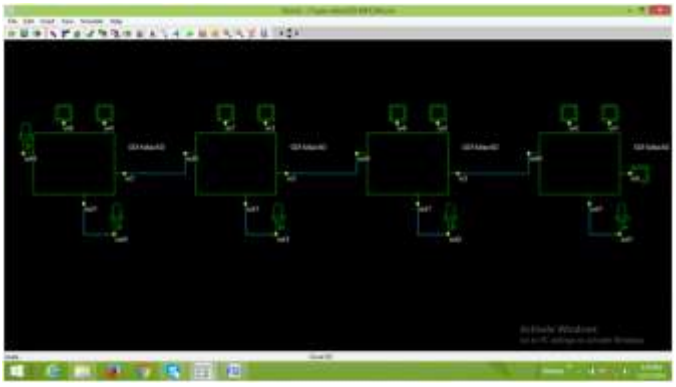
7.3 GDI TREE MULTIPLIER



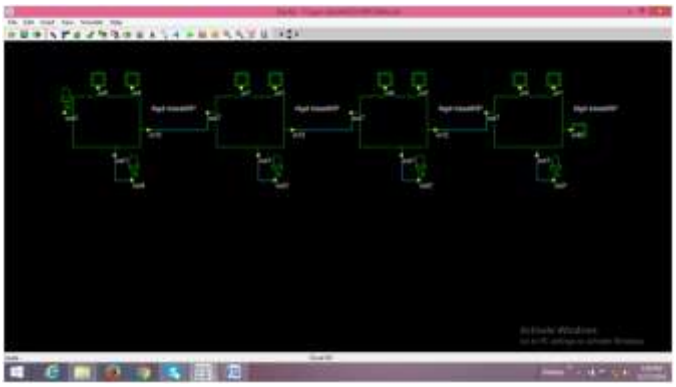
7.4 MGDI TREE MULTIPLIER



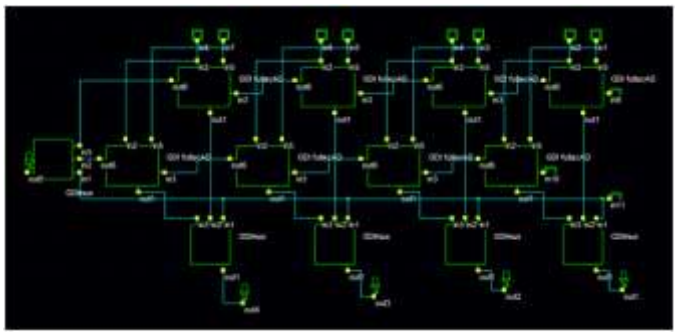
7.5 GDI 4-BIT RIPPLE CARRY ADDER



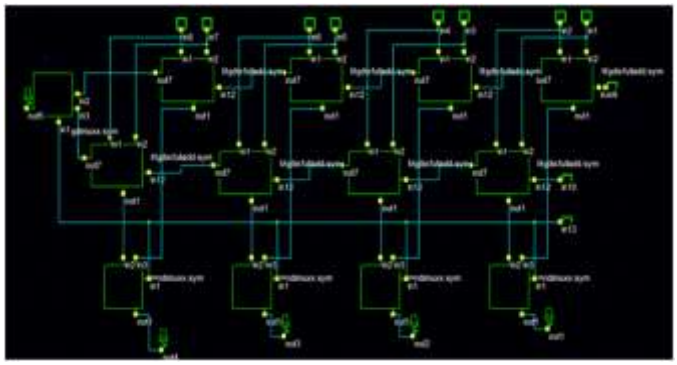
7.6 MGDI 4-BIT RIPPLE CARRY ADDER



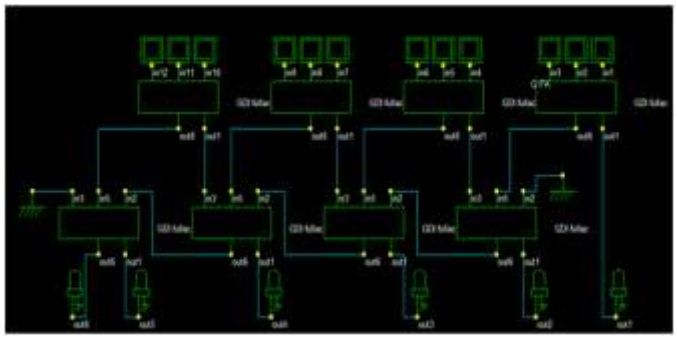
7.7 GDI 4-BIT CARRY SELECT ADDER



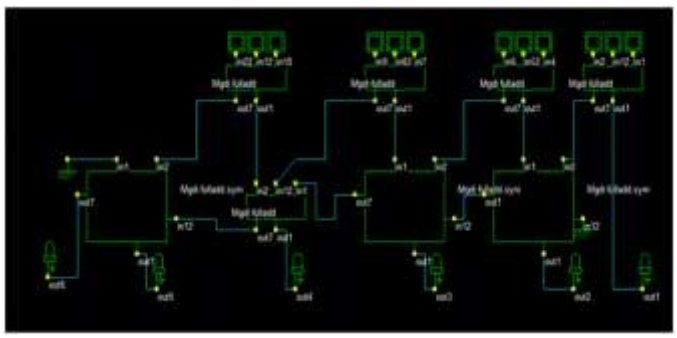
7.8 MGDI 4-BIT CARRY SELECT ADDER



7.9 GDI 4-BIT CARRY SAVE ADDER



7.10 MGDI 4-BIT CARRY SAVE ADDER



8. PERFORMANCE ANALYSIS

8.1 Comparative Performance Analysis of CMOS,GDI and MGDI Based Digital circuits

MODULE NAME	CMOS DESIGN		GDI DESIGN		MGDI DESIGN	
	POWER(watts)	Transistor Count	POWER(watts)	Transistor Count	POWER(watts)	Transistor count
INVERTER	2.105µ	2	2.105µ	2	2.105µ	2
AND	3.022µ	6	0.453µ	2	0.864µ	2
OR	7.156u	6	0.327µ	2	0.676µ	2
HALF ADDER	14.682µ	20	2.444µ	6	1.312µ	6
FULL ADDER	42.682µ	46	3.934µ	14	3.224µ	14
XOR	0.553m	14	1.816µ	4	1.248µ	4
2-INPUT MUX	17.314µ	20	3.872µ	8	1.314µ	8

8.2 Comparative Performance Analysis of CMOS, GDI AND MGDI Based Multiplier circuits

MULTIPLIER CIRCUIT	CMOS DESIGN		GDI DESIGN		MGDI DESIGN	
	POWER(watts)	Transistor Count	POWER(watts)	Transistor Count	POWER(watts)	Transistor Count
ARRAY MULTIPLIER	0.321m	64	3.845µ	20	1.244µ	20
TREE MULTIPLIER	15.334µ	64	2.105µ	20	0.521n	20

8.3 Comparative Performance Analysis of CMOS, GDI AND MGDI Based Fast adder circuits

FAST ADDER CIRCUIT	CMOS DESIGN		GDI DESIGN		MGDI DESIGN	
	POWER(watts)	Transistor Count	POWER(watts)	Transistor Count	POWER(watts)	Transistor count
RIPPLE CARRY ADDER	90.453µ	184	10.308µ	56	0.036µ	56
CARRY SAVE ADDER	0.110m	368	18.374µ	112	8n	112
CARRY SELECT ADDER	1.083m	468	10.580µ	152	0.013µ	152

9. CONCLUSIONS

We are primarily focused on the design of low power and high performance multipliers and adders. MGDI cell and GDI cell provides digital designs superior than other CMOS techniques in terms of power and transistor count .

The disadvantage of the GDI technique is that, it is not possible to obtain a strong 0 and strong 1 at the output under certain combinations of inputs . This disadvantage is reduced by using MGDI technique.

MGDI approach allows realization of a broad variety of multifaceted logic functions by means of only two transistors. MGDI gates lower the transistor count and in turn the silicon area required whencompared to standard static CMOS and Domino CMOS based approaches. The leakage power and switching power of MGDI gates is lower than the traditional logic styles.

The problem of fabrication of GDI gates in standard nano-scale CMOS process is overcome by connecting the sources of pMOS and nMOS to VDD and GND respectively in Mod-GDI logic style. The comparison between our analysis and prior works indicates that one of this logic styles for low power digital design does provide many advantages. In short, the proposed MGDI logic style based designs can be taken a better alternative in future.

The types of Multipliers and adders are used in many applications and processors, like DSP. Tree multiplier has less number of adder stages compare to array multiplier.

This work can be further extended for higher order number of bits. New architectures can be designed in order to reduce the power and area of the circuits.

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