FPGA CONTROLLED THREE LEVEL DIODE CLAMPED MULTILEVEL INVERTER FOR SOLAR PV SYSTEM

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Abstract- This paper includes the discussion about the principle of working and simulation of FPGA controlled 3-level diode clamped inverter, which is fed by solar PV based DC bus. DC bus was created with help of solar PV models and charge controller to feed DC loads directly or AC loads indirectly through proposed 3-level inverter.FPGA based 3-level inverter was simulated on Xilinx and MATLAB Simulink environments. Firing pulses ware generated through Xilinx system generator flat form to control the switches of multi-level inverter in MATLAB Simulink environment and also discussed and calculated the performance parameters of inverter to judge the performance. FPGA is used to generate pulses at fast switching frequency and also with the addition of FPGA this three level inverter having the fast processing speed and since the FPGA having low cost in order to hardware implementation. So, this will make these topologies better than the previous topologies which have been made in inverters.

Keywords- 3-Level Inverter, SPV system, Diode Clamped Multi Level Inverter, FPGA Controller, SPWM.

I. INTRODUCTION

With the increasing growth of population in rural, urban and suburban sectors the basic needs of an electrical energy going to be increases and in order to meet this excess demand of energy, there are (solar/wind etc) renewable energy available. Among these two sources solar energy is more preferred from these two as it is remain available in everywhere, where as in coastal area wind energy is restricted. Also, Solar powered systems can generate electricity using photovoltaic (PV) panels, or thermal collectors. So today's trends go through solar energy. Earlier conventional inverter has been in used for conversion from dc to ac. Normally conventional inverter nothing but a two level inverter.

1.1 Two-Level Inverter Operation

In these topologies there are two combination possible, one is half bridge configuration and other is full bridge configuration. The half bridge configuration is simplest one having two switches S_1 and S_2 center tapped with the two series connected capacitor as shown in fig.1. The supply voltage V_{dc} split into $V_{dc}/2$ across each of these capacitor. It is to be noted that at a time, only one switch has to be operated otherwise if both operate at the same time, short circuit occurs across supply voltage V_{dc}.

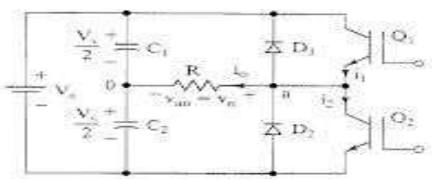


Fig.1 single phase half bridge inverter

The operating principle shown as:

V_{ao}	S_1	S_2
$V_{dc}/2$	1	0
$-V_{dc}/2$	0	1

Table: 1 Switching combination

Similarly, in Fig.2, the full bridge configuration having four switches in which S_1 and S_4 operate simultaneously in order to obtain $V_{dc}/2$ and S_2 and S_3 in order to obtain $-V_{dc}/2$. Since there will be delay in turning on the other pair of switch from one pair,because already turn on switch will take time to come to off position.

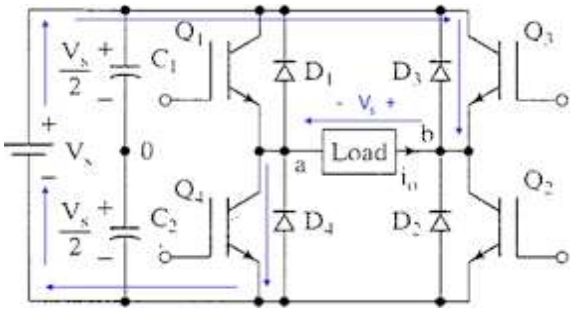


Fig.2 single phase full bridge inverter

The output waveform of half bridge and full bridge shown in fig.3 (a) and fig.3 (b)

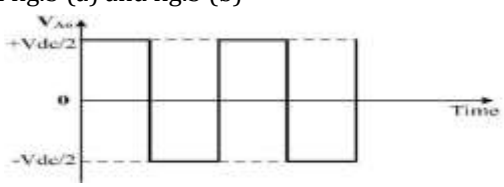


Fig.3 (a) Output Waveform of Half-Bridge Configuration

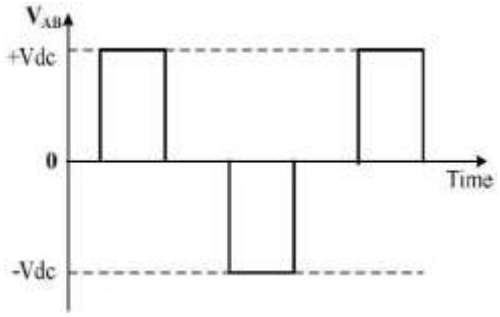


Fig.3 (b) Output Waveform of Full-Bridge Configuration

However in the field of high voltage and high power application, the switching frequency of the power converters has been restricted up to 1 KHz even with the HVIGBT and GCT due to the increased switching losses. The maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult. From the aspect of harmonic reduction and high DC link voltage level, three-level approach seems to be the most promising alternative.

This paper organized as follows: section II discussed about the distinction between conventional and multilevel inverter and the method of adopted topologies in order to obtained more stepped waveform at the output of multilevel inverter so that the harmonics get reduces. Section III introduced the three level diode clamped inverter with the Field Programmable Gate Array (FPGA) and its working principle and discussed its advantages. This section also discussed the various problems which has been already short out earlier. Section IV having the simulation of three level diode clamped inverter with the implementation of field programmable gate array (FPGA) and its various stages waveforms which gives the overall more stepped output waveform having reduced harmonics.

II. PROPOSED INVERTER

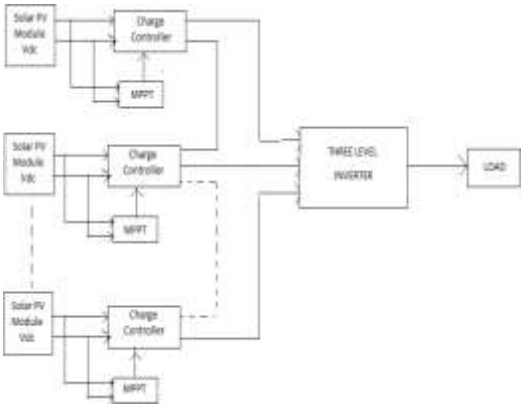


Figure 4. Proposed System

1.1 PV module:

The equivalent circuit of a PV cell is shown in below. It consists of an ideal diode in parallel with an ideal current source.

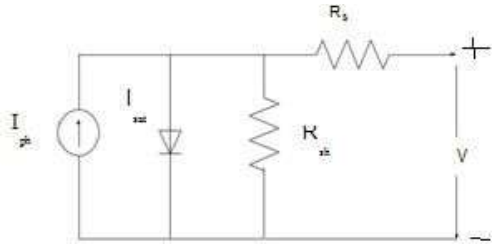


Fig.5 equivalent circuit diagram of PV module

The current generated by photons is represents by the current source (often denoted as I_{ph} or I_L), and under constant temperature and constant incident radiation of light, its output is constant from the PV cell. The output current (I) is found by applying the Kirchhoff's current law (KCL) on the equivalent circuit shown:

$$I = I_{sc} - I_d \quad \ldots\ldots (1)$$

where: $I_{sc}$is the short-circuit current equal to the photon current generated by photon and I_d is the current shunted by intrinsic diode. By the Shockley's diode equation the diode current I_d is

$$\mathbf{I_d = Io(e^{qVd/kT} - 1)} \quad \ldots\ldots (2)$$

Where: Io is the diode's (A) reverse saturation current, q is the electron charge (1.602×10-19 C),$V_d$is the voltage across the diode (V), k is the Boltzmann's constant (1.381×10-23 J/K),T is the junction temperature in *Kelvin (K)*.Replacing I_d of the equation (1) by the equation (2) gives the current-voltage relationship of the PV cell.

$$I = I_{sc} - Io(e^{qVd/kT} - 1) \quad \ldots\ldots (3)$$

Where: V is the voltage across the PV cell, and I is the output current from the cell. Using the equation (3), let I = 0 (no output current) and solve for Io.

$$0 = Isc - Io(e^{qVd/kT} - 1) \quad \ldots\ldots (4)$$

$$Isc = Io(e^{qVd/kT} - 1) \quad \ldots\ldots (5)$$

$$I_o = \frac{I_{sc}}{e^{qVoc/kT} - 1} \quad - - - - - - (6)$$

To a very good approximation, the photon generated current, which is equal to I_{sc}, is directly proportional to the irradiance, under the standard test condition, Go=1000W/$m2$ with air mass (AM) = 1.5, the current generated by photon generated current at any other irradiance, G (W/$m2$), is given by:

$$Isc = I_G(G/G_o)\ Isc I_{Go}$$

II. MULTILEVEL INVERTER

The multilevel starts with the three-level which is also known as neutral point clamped three-level inverter proposed by AkariNabae [2].Cleary distinction in conventional and multilevel inverter. So many PWM strategies have been proposed to solve the neutral-point potential unbalance problem [6],

[7].Multilevel inverters are based on the fact that a sine-wave can be approximated to stepped waveform having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or different DC sources like different solar modules, and it is to be noted that having more no. of levels correspond to the more stepped waveform. On the basis of the circuit topologies the multilevel inverters are classified into following three basic categories [3-4].

- Diode-clamped multilevel Inverter (DCMLI)
- Capacitor-clamped or Flying Capacitor multilevel Inverter (FCMLI)
- Cascaded multilevel (H-bridge) Inverter.

III. THREE LEVEL DIODE CLAMPED INVERTER

Fig.4 shows a three level diode clamped multilevel inverter having two capacitors C_1, C2.With the source voltage V_{dc} each capacitor having voltage $V_{dc}/2$ and the middle point of these capacitors(n) defined as neutral point and each device to be limited by voltage level $V_{dc}/2$ through clamping diodes. To define three level voltages across a and n the possible combinations of switches have made as follows

For voltage level $V_{an}=V_{dc}/2$, switches S_1 and S_2 to be turn on
For voltage level$V_{an}=-V_{dc}/2$, switches S_1' and S_2'to be turn on
For voltage level $V_{an}=0$, switches S_2 and S_1'to be turn on.

Two complementary switches are there that means one switch turn on then their complementary switch to be turn off at the same instant. In this case, the two complementary pairs are (S_1, S1') and(S_2, S_2').

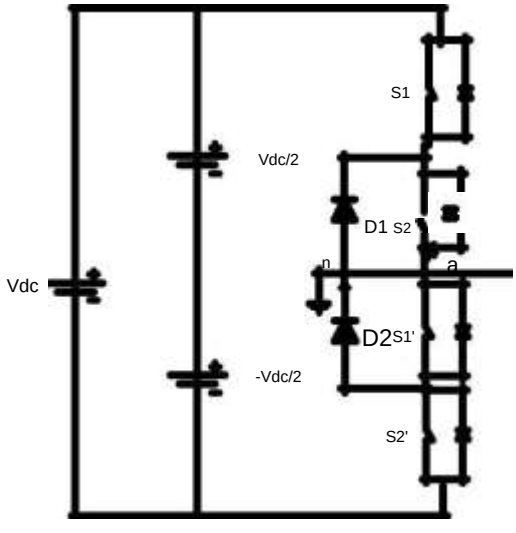


Fig.6 Three-Level Diode Clamped Inverter

The three switch combinations to synthesize three level voltages across 'a' and 'n' are Formed below.

TABLE:2 switching combination for output Voltage

Output voltage (Van)	S_1	S_2	S_1'	S_2'
Vdc/2	1	1	0	0
0	0	1	1	0
-Vdc/2	0	0	1	1

Where, '1'represent on state and '0' represent off state. With the addition of FPGA this three level inverter has the fast processing speed and also here the FPGA available at low cost in order to hardware implementation for more number of switching elements. These are the benefits with FPGA which make these topologies better than the previous topologies made in inverter.

Here each device, which is active enough to block a voltage level of (V_{dc}/m^{-1}) . Where m is number of Level. Fig.---- shows the voltage waveform of three level inverter.

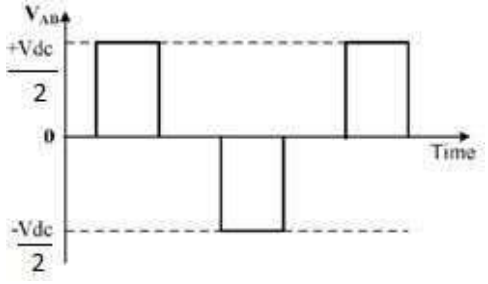


Figure:7 stepped waveform the topology of Fourier analysis

The key component that distinguished the three level inverter from conventional two level inverter is D1 and D2. This switched voltage level clamped into half the level of dc bus voltage through these two diodes. here are D2 balances out the sharing voltage between S_1' and S_2', S_1' blocking the voltage across C_1 and S_2'blocking the voltage across C_2. If the output across 'a' and 'o' is removed then it work as dc converter having three voltages $V_{dc}/2$,0 and $-V_{dc}/2$.It is to be noted that output voltage V_{ao} is dc and across Van is AC. Now in order to obtain the more is going to be used.

Fourier series of the instantaneous output voltage:

$$Vo=\frac{ao}{2}+\sum_0^{\infty}(an\cos(nwt)+bn\sin(nwt))$$

$$a_0,a_n=0$$

$$bn=\frac{1}{\pi}\left[\int_{-\pi}^{0}\frac{-Vs}{2}\sin(nwt)d(wt)+\int_0^{\pi}\frac{Vs}{2}\sin(nwt)d(wt)\right.$$

$$bn=\frac{2Vs}{n\pi},n=1,3,5,\ldots.$$

Hence the output voltage waveform becomes:

$$V_o=\sum_{n=1,3,5,..}^{\infty}\frac{2Vs}{n\pi}\sin nwt$$

And on passing it through low pass filter, we get the fundamental component's rms value.

$V_{01}=(1/\sqrt{2})(2Vs/\pi$
$V_{01}=0.45Vs$

Also with this output voltage, can also get the Fourier series expansion of output current in case of RL load as shown below

$$Io=\frac{Vo}{Z}=\frac{Vo}{R+jnwl}=\sum_{n=1,3,5,..}^{\infty}\frac{2Vs}{n\pi\sqrt{R2+(nwl)2}}\sin(nwt-\Theta_n)$$

$$\Theta_n=\tan^{-1}(\frac{nwl}{R})$$

In most cases the fundamental output power is:

$$P_{01}=Vo1Io1\cos\Theta_1=I\hat{}2_{01}R$$

$$P_{01}=[\frac{2Vs}{\sqrt{2}\pi\sqrt{R2+(wL)2}}]2R$$

If lossless inverter is there, than the load absorb the power equals to the average power supplied by the dc source.

$$\int_0^T Vs(t)i_s(t)dt=\int_0^t Vo(t)i_o(t)dt$$

Current is approximately sinusoidal for an inductive load and the power supplies to the load by the fundamental component of the output voltage and also the dc supply voltage remains essentially at Vs.

$$\int_0^T is(t)\ dt=\frac{1}{Vs}\int_0^t\sqrt{2}(t)\ V_{01}\ \sin(wt)\ \sqrt{2}\ Io\ \sin(wt-\theta_1)dt=Is$$

$$I_s=\frac{vo1}{vs}I_0\cos(\theta_1)$$

Here, the performance parameters discussed in order the minimization of harmonics content in the output waveform:

1. From these above equation can calculate the harmonic factor having **n^{th} harmonic(HF_n)**

$$HF_n=\frac{Von}{v01}\text{ for n>1}$$

V_{0n}=harmonic component's rms value.
V_{01}=fundamental component's rms value.

2. **Total Harmonic Distortion(THD):**

The THD harmonics are those harmonics which measures the closeness in shape between a waveform and its fundamental components.

$$THD=\frac{1}{V_{01}}(\sum_{n=2,3,...}^{\infty}V_{on}{}^2)^{1/2}$$

3. **Distortion factor(DF):**

Those harmonic which is remain in a waveform after the harmonic subjected to attenuate to second order, the indication of these amount of H_d called distortion factor.

$$DF=\frac{1}{V01}[\sum_{n=2,3,....}^{\infty}(\frac{von}{n2})^2]^{1/2}$$

$$DF=\frac{von}{vo1n2}\text{ for n>1}$$

4. **Lowest order harmonic(LOH):**

It is defined as those harmonic components having the frequency are almost close to fundamental and also its amplitude either greater than or at least equal to 3% of fundamental component's amplitude.

Unequal device rating and capacitor voltage unbalance:

Here, it is to be seen that S_1 conducts only for $V_{ao}=V_{dc}/2$ and S_2 only for $V_{ao}=0$.The difference between V_{ao} and $\mathbf{V_{an}}$ is the capacitor voltage $V_{dc}/2$ and also there will be needs of power for transfer real power factor. Charging time for rectifier operation and discharging time for inverter operation for each capacitor is to be different. In order to short out the problem of voltage unbalance , the capacitor is replaced by controlled constant DC voltage source such as PWM Voltage regulators or batteries[6] and [7].Use of controlled constant dc system results complexity and less economical in system- subject matter is not understandable and in order to avoid switching losses for electromagnetic interference problem, the output switching frequency should be maintained minimum.

A different converter topology introduced, having different source which is based on the series connection of single-phase inverters [4].

A control method for a hybrid cascaded multilevel inverter Investigated [11] is more advantage of conditioning inverter utilizes in order to increase efficiency and hence minimizes the harmonic content. conditioning inverter act as energy storage which increases the efficiency. Both having three outputs so that one unit cell of h-bridge can be minimize with the conditioning inverter outputs or in case one cell of main inverter is worse than the conditioning inverter can supply the energy to main inverter.

Simple balancing method of capacitor voltage is buck-boost converter [6] in which the half cycle of charging of inductor is used to compensate capacitor's loss charge.

To control capacitor voltage of three level inverter, the method of zero sequence current has been presented [7], the system slightly complex and complexity increases as per increasing higher levels. Generalized topology has been presented [8]. It present a structure from which any type and any level inverter can be deducted with self voltage balancing and also this topologies does not required any extra component like clamping diodes and voltage balancing capacitors.

Thus the diode clamped inverters having the advantages:

- All devices switched at fundamental frequency, therefore no switching losses hence the efficiency get increases.
- Large number of level increases, so the harmonic content get reduced
- Avoided the need of filters.

IV. SIMULATIONS AND DISCUSSIONS

Simulations for the proposed system have been completed and tested on MATLAB Simulink and Xilinx System generator environments. Simulink block diagram of proposed system has shown in following figure.

In this proposed system, Power circuit has been implemented in MATLAB Simulink environment and

Controlling circuits for converters have been implemented in Xilinx system generator environment.

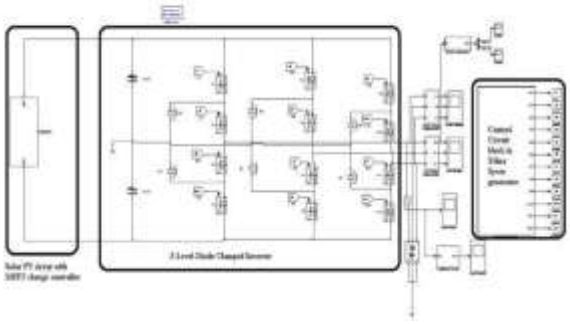


Figure:

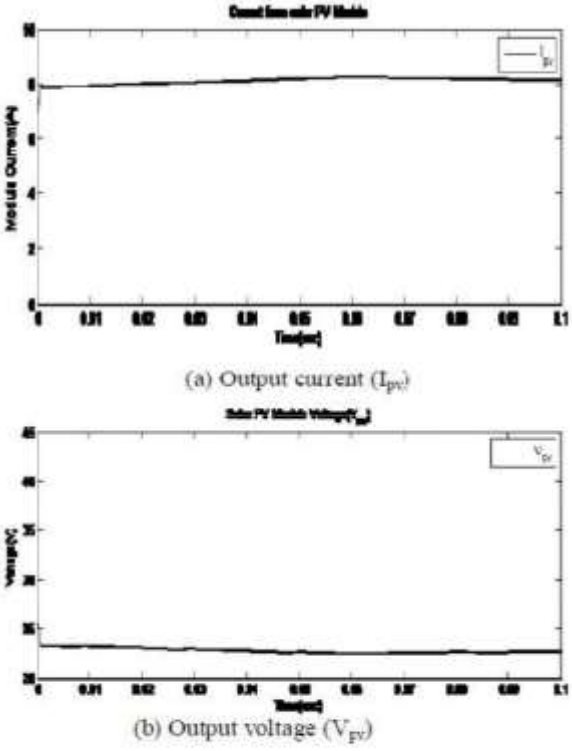
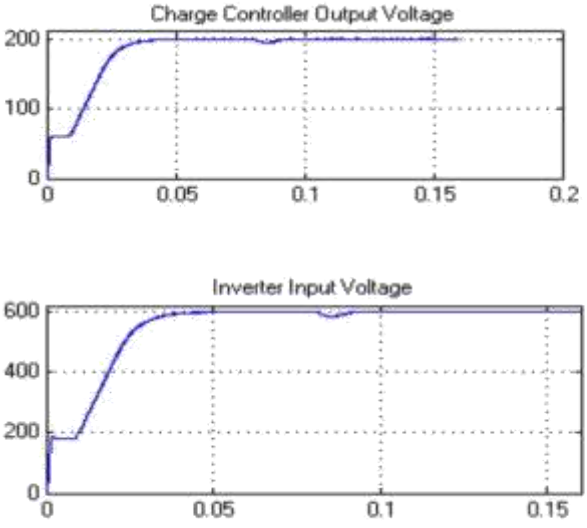


Figure 9. Output voltage and current of SPV module



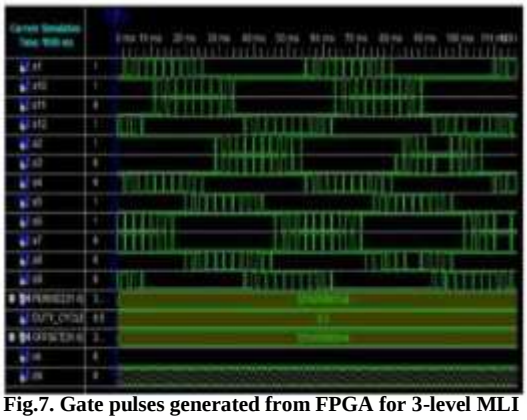
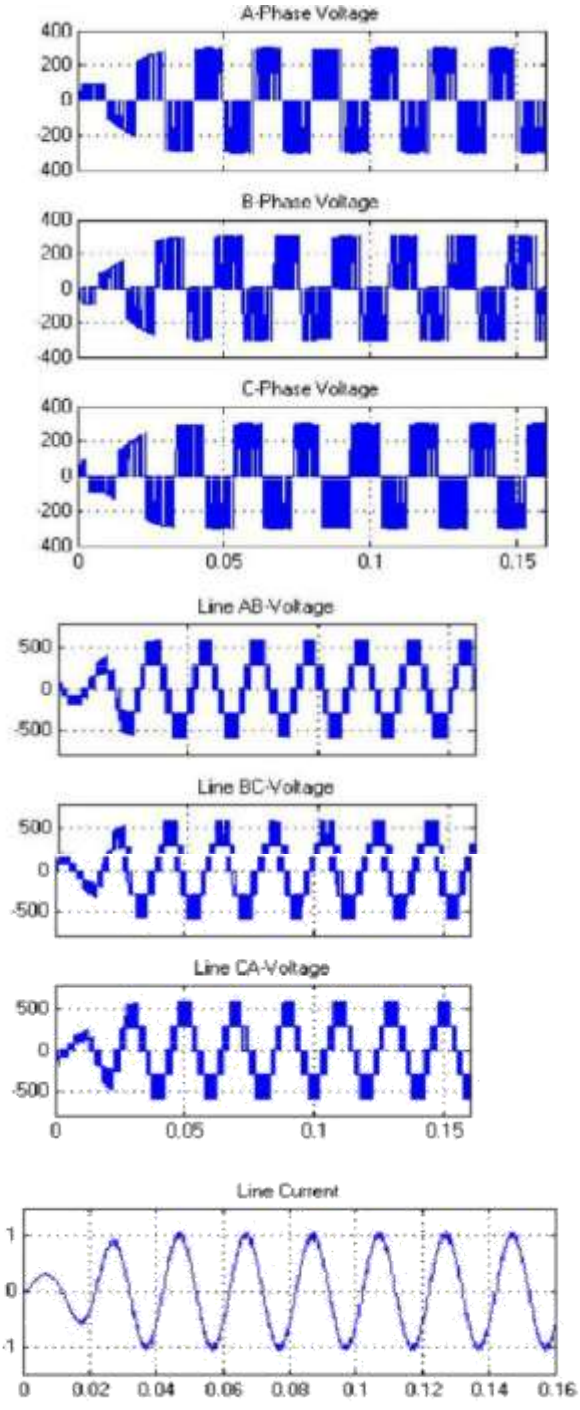
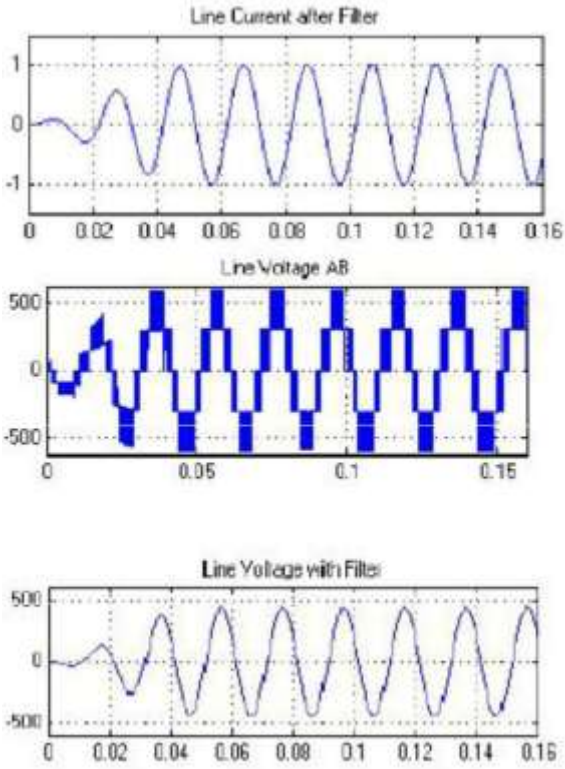


Fig.7. Gate pulses generated from FPGA for 3-level MLI





CONCLUSION

The controller implementation with the help of FPGA can be made fast processing speed, resulting the performance becomes significantly enhanced over microprocessor-based implementations. Based on these results, it is expected that multilevel inverter will become an effective solution for PV system shortly.

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