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Analysis of Low Noise Amplifier using 45nm CMOS Technology

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Abstract - *In the receiver section of the communication system, there is a highly need of amplification of weak signal received from the antenna. This amplification is accomplished by using a prime component of the receiver part, namely, Low Noise Amplifier. There are certain parameters that describe the characteristics of the Low Nosie Amplifier. The parameters are gain, linearity, noise figure, bandwidth, chip area and power consumption. This paper is designed in 45nm CMOS Technology. The pre-simulation and post-simulation waveforms are obtained for Transient Analysis and AC Analysis. The proposed design is a low power Low Nosie Amplifier with 1.2V power supply that provide gain of 13.631 dB, bandwidth of 10.71 KHZ, power consumption of 35.31uW and with the small chip area of 0.6um².*

Key Words: **LNA, Common Gate Amplifier, Common Drain Amplifier, Active Inductor, Gain, Bandwidth, power supply, chip area.**

1. INTRODUCTION

In the present days, radio receivers are the major devices in the field of communication. The main purpose of receivers is to convey the exact information from the transmitters to the users by the conversion of electromagnetic waves present in the environment [1]. The major device is present in receiver section, that can amplify the received weak signal. Since the process of amplification is necessary because the signal received from the antenna while transmitting to the environment degrades due to the environmental influence. As a result, there is a necessity of amplification of the received signal, this makes it important to use Low noise amplifier that amplifies the weak signal.

LNA targets on maintaining gain, power, and noise figure in required level [2]. To make the working of a Low Noise Amplifier efficient for the higher-level and also signals at the low power level, the signal to noise ratio is managed to be in the required range with no noise added [3].

The efficiency of Low Noise Amplifier is dependent on factors like Gain, Noise Figure, Bandwidth, Linearity. With the increase in the number of the usage of the Bluetooth, GPS and many other wireless devices there is also an increase in need of Low Noise Amplifier with high gain to reduce the noise present in the received signal, and also the amplifier need to have low Noise Figure. High gain and low noise figure shows how efficient the amplifier is.

The LNA configurations are of many topologies which can be used for various applications. On designing a particular LNA as per the requirement then it is necessary to have better working features which is described by the gain, bandwidth, power consumption and also including the circuit area. Normally, common gate amplifier (CGLNA) or common source amplifier (CSLNA) form the input stage of Low Noise Amplifier design and the output stage consists of Common Drain Amplifier.

2. LITERATURE SURVEY

K.Sakthidasan, Sankaran and K.E.Purushothaman [1], has proposed a paper which explains variety of Low Noise Amplifier designs, for the purpose of designing a front end receiver. The paper involves common gate, resistive parallel feedback and cascading feedback network are designed for low power. They have also used current reuse circuit to enable the generation of necessary current to the design. The circuit is designed in cadence analog library in 180nm technology. The designed LNA achieves bandwidth of 0.1-8GHz, Noise Factor of 8.2dB, and power consumption of 1.86mW.

H. Aljarajreh, M. B. I. Reaz, M. S. Amin, H. Husain [2] has proposed a paper which explains a design that gives various solutions to solve the problem caused by using the passive inductors with the idea of creating a small chip area. In addition to this, the effect of parasitic capacitors at the high frequencies can also be lowered by using active inductor. The design is with 180nm CMOS Technology. The circuit is designed with chip area of 0.003 mm² and also shows a noise figure of 3.1 dB, gain of 20dB.

M. I. Idris, N. Yusop, S. A. M. Chachuli, M.M. Ismail, Faiz Arith and N. Shafie [3] proposed a paper that describes a LNA design made of three important stages. 130nm CMOS Technology is preferred in the designing. the design involves common gate and common drain amplifier in the input and output stages since these amplifiers provide good input and output matching. They also exhibit the potential of lowering the noise. The contribution of active inductor is such that the circuit consumes less power and also makes a compact chip area. This design conveys the output received with chip area

of 0.26mm^2, power consumed to be 0.8mW with gain of 9dB and noise figure of 7dB.

Das, Tim [4] has proposed a paper that gives the idea of the practical considerations required in designing a Low Noise Amplifier. This paper has also explained the device and board level variables that can affect the working process of an LNA. This paper also shows the examples of practical challenges by considering three LNA topologies. The paper aims at providing a brief survey of the important factors that might bring changes in the LNA performance and implementation.

Jouni Kaukovuori, Mikko Kaltiokallio and Jussi Ryynanen [5] has proposed that explains the usage of common gate low noise amplifier for the wideband applications. The effect of the different components in matching network is analyzed in detail. In addition, the effect of the matching network on the noise and the linearity of a CG stage is studied. With the purpose of demonstrating the effectiveness of this theory a design example is being explained.

3. OBJECTIVE

The major intension of this paper is to design a low power Low Noise Amplifier with the appropriate parameters exhibiting less power consumption and high gain, suitable bandwidth and small size consuming less space in the receiver section, which will also lower the cost of the device. The design has also undergone both the pre-simulation and post simulation of transient analysis and AC analysis.

4. METHODOLOGY

The LNA design is composed of CG amplifier, Active Inductor and CD stage, as shown in fig -1. Basically, CG amplifier is used at the input stage and CD amplifier is used at the output stage as they provide best input and output matching. The LNA is bound with certain characteristics like noise figure and gain. The selection of LNA also depends on certain parameters like bandwidth, power supply, linearity and chip area.

Fig -1: Block diagram of the proposed LNA [1].

4.1 Common gate amplifier:

Common Gate Amplifier forms the first stage of the proposed. Low Noise Amplifier. With CG stage in the circuit it is not much difficult to receive input impedance matching [2]. CG amplifier can be used as voltage amplifier or current buffer [3].

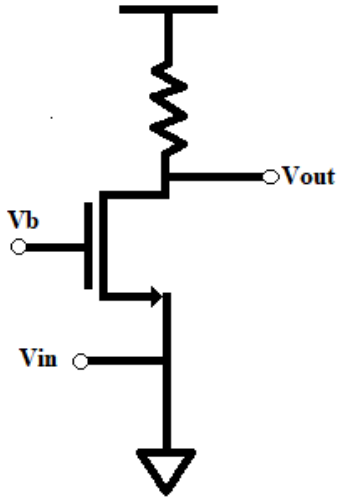

Fig -2: Common Gate Amplifier

4.2 Active inductor:

Active inductor consists of CMOS transistors and it also performs the operation same as passive inductor [2]. Active inductor is designed to provide good quality factor that determines its efficiency.

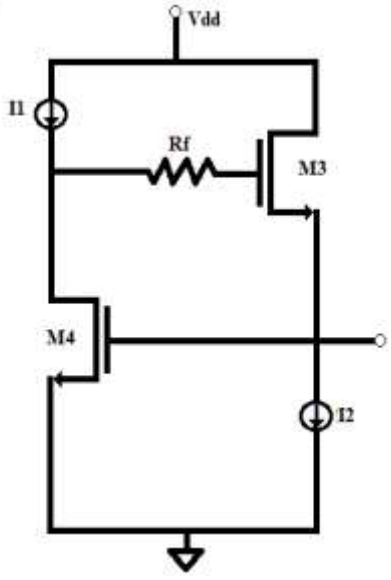

Fig -3: Active inductor circuit and its equivalent circuit [2].

Active inductor can be improved in its performance by introducing double feedback to the circuit design. Active inductor with double feedback is shown in the figure.

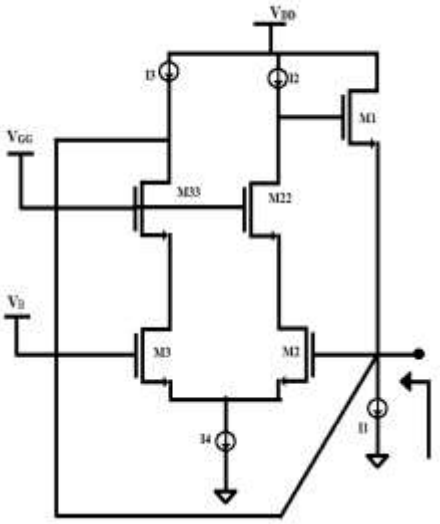

Fig -4: Double feedback active inductor with second order effects [2].

4.3 Common drain (CD) amplifier:

CD amplifier, also usually referred as a source follower or buffer. It is commonly used at the output stage in most of the LNA design. Common Drain amplifier has low output impedance. As a result, it can provide favorable output impedance matching [2].

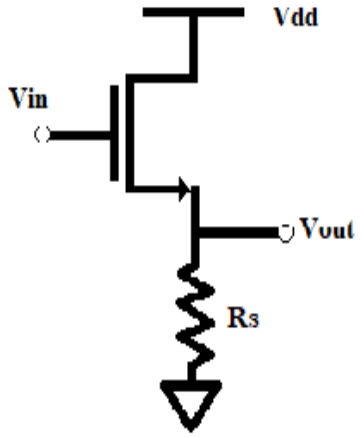

Fig -5: Common Drain Amplifier

4.PROPOSED LNA DESIGN

The proposed LNA Design is accomplished in 45nm CMOS Technology. The Low Noise Amplifier consists of 12 transistors. Using minimum number of transistors in the design will be helpful for reducing the parasitic effects and also lowers the consumption of the power. The power supply to the circuit is 1.2V. With V1= 0.7V, Vgg= 1.1V, V2= 1.2V and V3= 0.6V the circuit shows great amplification with gain Av= 13.67dB, bandwidth = 10.34KHz and power consumption of 33.37uW.

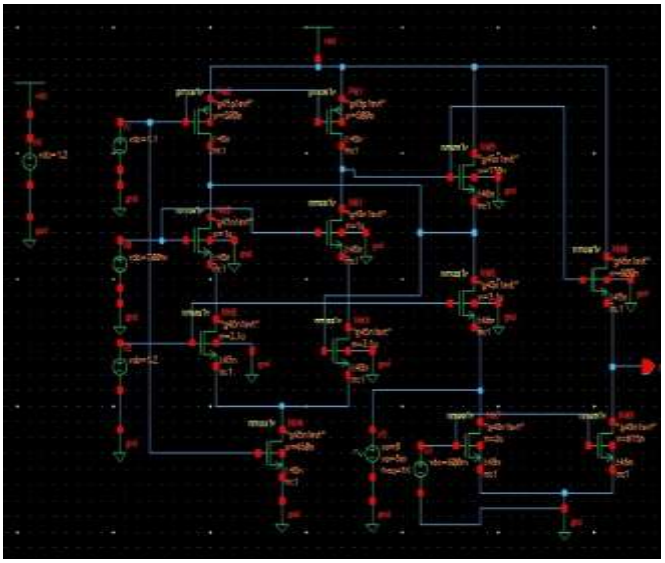

Fig -6: Schematic of proposed LNA

Table -1: Widths of the transistors for length 45nm

Transistor	Width(m)
M0	2u
M1, M2, M3	3.1u
M4	170n
M5	450n
M6, M7	500n
M8, M9	1u
M10	900n
M11	675n

5. RESULTS

5.1 Pre-Simulation Result

Transient analysis shows the output of amplification of the given input signal. It is displayed in time domain. Through transient analysis, the power consumed by the circuit design can be calculated in the cadence tool.

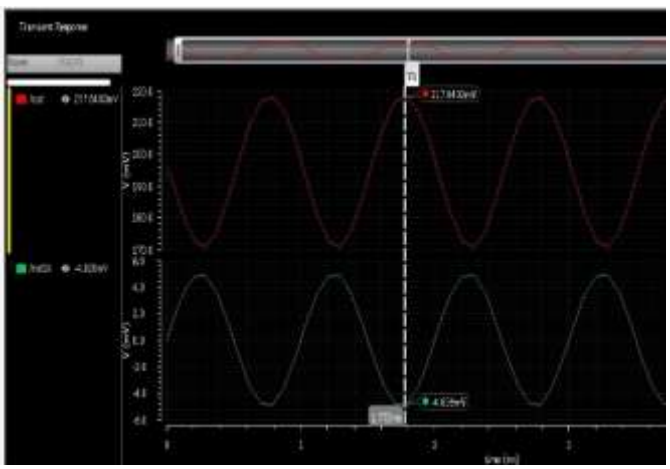

Fig -7: Transient Analysis of proposed LNA

The AC analysis describes the frequency response.

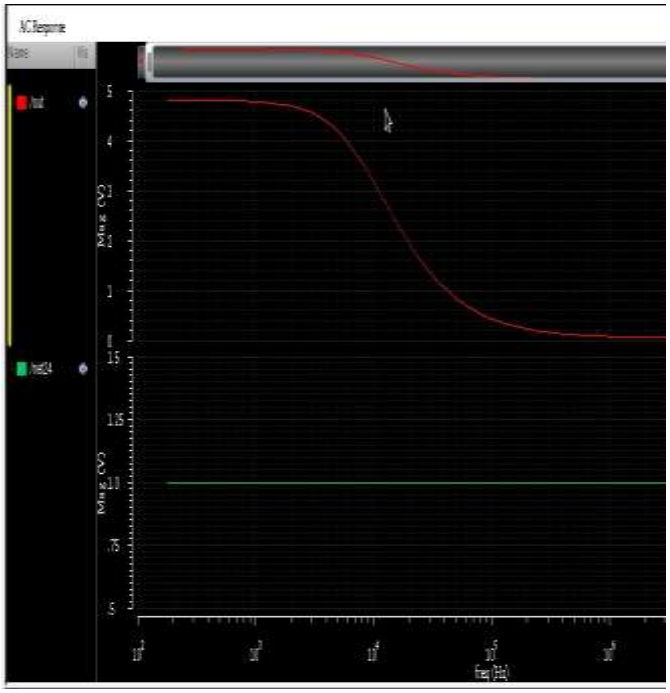

Fig -8: AC analysis

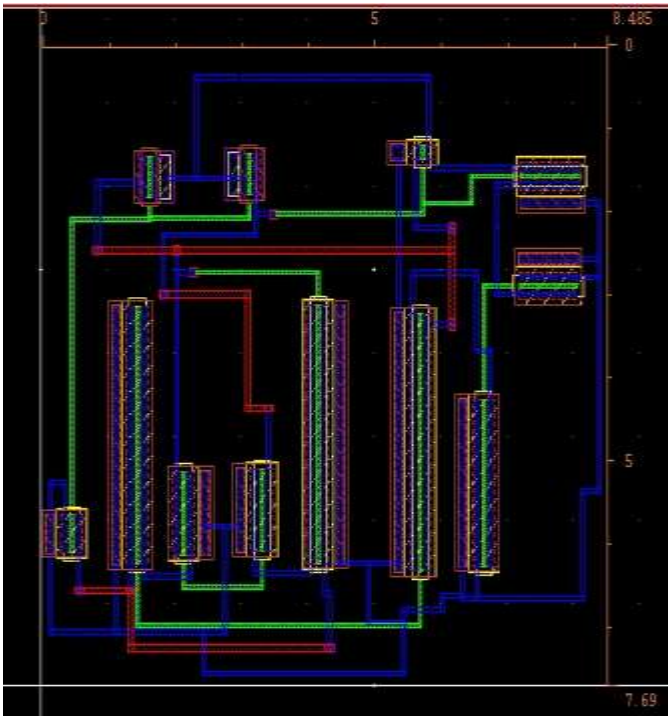

Fig -9: Layout of the proposed LNA design

5.2 Post Simulation Result

Post simulation is performed to obtain the result after considering the parasitic effects obtained in in the av-extraction of the design.

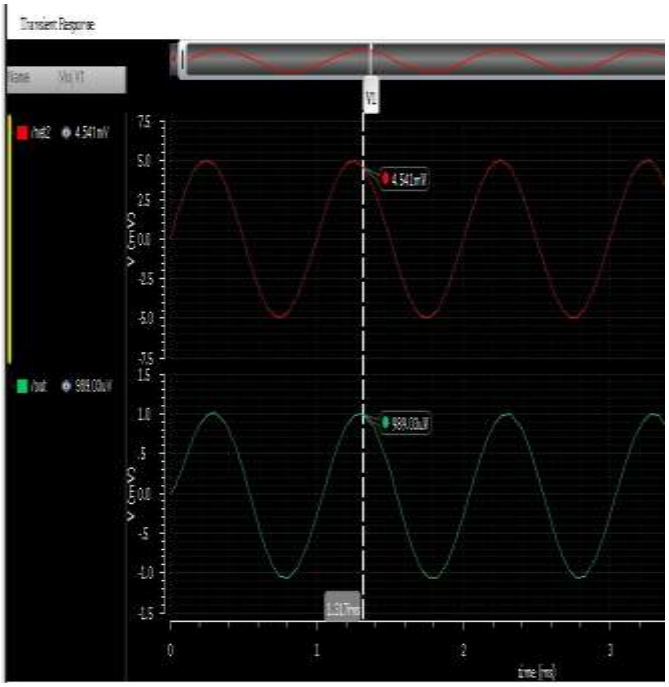

Fig -10: Transient Analysis

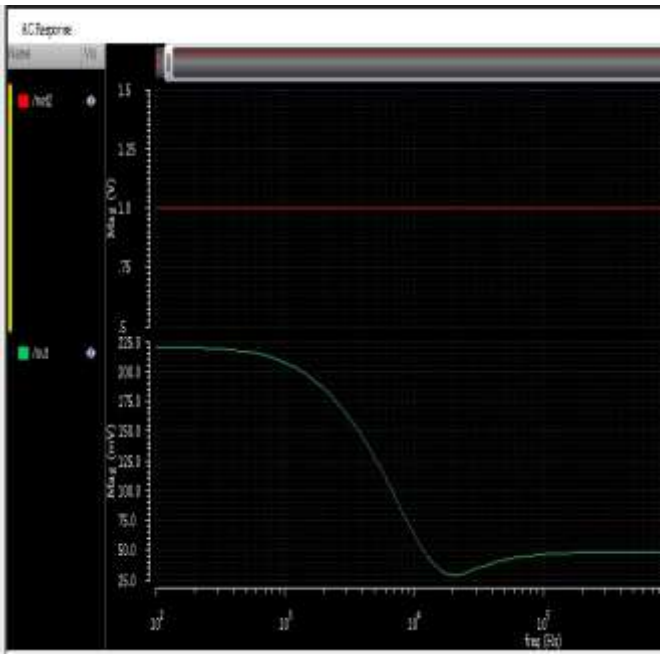

Fig -11: AC Analysis of post simulation

6. DISCUSSION

As it is already explained what are the main parameters that describe the characteristics of the Low Noise Amplifier, it is important to keep note that the parameters obtained for the designed LNA makes it efficient. The parameters that are calculated in this implementation are gain, bandwidth, power supply and chip area. The future work involves working on the parameters like noise figure and linearity.

7. CONCLUSION

With the rapid increase for the demand of the wireless communication system there is a high need for low noise amplifier that can amplify the weak signal received at the receiver section from the antenna. Here the circuit is design in 45nm CMOS Technology with low power supply of 1.2V. This paper mainly concentrated on the gain, bandwidth, power consumption and also on the compact size of the chip. Hence showing the output with gain of 13.631dB, bandwidth of 10.71KHz, power consumption of 35.31uW and area of 0.6um^2.

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