Design and Simulation of 12-bit Current Steering DAC

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Abstract - *Most of signals in nature are analog, so electronic systems requires analog processing, hence there are analog processing devices like amplifiers as input and output devices in use, design and implementation of analog system are difficulty, and stability is the matter of concern. On the other hand, digital system design and their implementation are more feasible. Therefore, there is a need to convert the analog input signals into digital signals at the input end, and after processing them in the digital domain; they have to be converted into analog signals in most of the applications. Here current steering Digital to Analog converter implemented with advantage of speed, power and high accuracy.*

Current Steering DACs has indicated that segmented architectures can reduce the need for having large variations in the widths of current source transistors. The current steering DAC architectures helps in keeping the load current (i. e. current drawn by the DAC) constant, and in achieving a higher speed of operation. Keeping these considerations in view, an 12-bit segmented current steering DAC has been designed. The DAC has been divided into four segments of 3-bits each. One segment caters to lower LSB 3-bits of input digital word, second segment caters to lower MSB 3-bits of input digital word, third segment caters to upper LSB 3-bits of input digital word and the last segment caters to upper MSB 3-bits.The design will be implemented in a state of the art 180 nm process, with a supply voltage of 3 V and at a sampling speed of 2 GHz.

Keywords— Current steering DAC, Switch Driver, Cascode Current Mirror, Differential Switch.

I. INTRODUCTION

Nature is completely with analog signal so need to convert analog input signals into digital signals at the input end, and after processing them in the digital domain; they have to be converted again into analog signals in most of the applications. The two obvious types of data converters are Analog to Digital (ADC) and Digital to Analog (DAC) converters.

A. Objectives

The main aim of this paper is to Design a 12 bit current steering DAC. To achieve the aim, the following objectives have been carried out.

1) Design of Switch Driver Architecture.
2) Design of Binary to Thermometer decoder.
3) Design a Dynamic Element matching coder.
4) Design of a 3 bit Current Steering DAC.
5) Design of a 12 bit Current Steering DAC

B. Motivation

The penetration of electronics into areas like computers, communications, instrumentation and embedded systems such as mobile phones, camcorders, HDTVs has given rise to the need for DACs with stringent requirements. The requirements span over features like high accuracy, linearity, reliability, high speed, low power and so on. There are various approaches adopted to achieve specific characteristics as given below:

Speed: Higher speed is generally achieved by the use of current steering DAC architecture

Accuracy: Accuracy can be improved by adopting the segmentation approach in the design of current source array architecture where the ratio of transistor widths is not too high in each segment

C. Problem Description

The binary weighted DAC suffer from a drawback of larger glitch energy induced during mid code transition due to the high switching activity of current sources. The work attempts to achieve minimum switching activity and thus reduce the resultant glitch energy. Binary to thermometer decoders are often used to convert binary codes into thermometer codes to control unit current cells. However the matching property of current sources is still a critical problem. Currently the most effective approach to reduce the mismatch effect and transistor size is the Dynamic Element Matching (DEM) method implemented with a randomizer. This can be designed to have minimum switching activity. The glitch energy can be further reduced in addition to the significant reduction in its transistor size, thus easily allowing for resolutions higher than 14 bit with a small chip area.

D. Literature Survey

To fulfil the objectives of the work, technical papers were referred. Switch Driver and Current Cell were taken from "**A 10 bit 1 GS/s Nyquist current steering CMOS Digital to Analog converter"** Anne van den Bosch student Member IEEE, Marc A.F. Borremans, Student Member IEEE vol .36 No 3. Dynamic element matching

block has taken from "**A Compact Dynamic Performance Improved Current Steering DAC with Random Rotation Based Binary weighted selection"** Wei Te Lin, Student Member, IEEE and Tai Haur kuo VOL 47, NO 2. 3 bit Current steering DAC has taken from "**A 12 bit 40nm DAC Achieving SFDR >70dB at 1.6 GS/s and IMD < -61 dB at 2.8 GS/s with DEMDRZ Technique".**

II. ARCHITECTURE OF 3 BIT DAC

Architecture of the 3 bit Current Steering DAC consists of four blocks such as Thermometer Decoder, Switch Driver, Differential Switch and Cascode Current Mirror.

A. Binary to Thermometer Code

In binary weighted DAC when binary code switches from 011 to 100, three bits change simultaneously and this may cause glitches. The Thermometer decoder will takes binary inputs then converts into unary outputs. For Ex: if the binary inputs are 000 is applied to thermometer decoder then it will produce 0000000. 16 bit thermometer codes has to be used to represented by binary ones in a length of 4, and so on. Although the thermometer codes need much more bits than their counterparts, (especially when bits are large) they have advantages in only changing one bit every time to avoid glitches.

Table 2.1 Truth Table of Binary to Thermometer

Binary b2 b1 b0	Thermometer t1 t2 t3 t4 t5 t6 t7
000	0000000
001	0000001
010	0000011
011	0000111
100	0001111
101	0011111
110	0111111
111	1111111

According to Truth Table 2.1 the logical relationship can be expressed as follows. Here **t** represents the thermometer code and **b** represents the binary code

t1 = b1 X b2 X b3; t2 = b1 + b2;

t3 = b1 X b2 + b3; t4 = b1;

t5 = b1 + b2 X b3; t6 = b1 + b2;

t7 = b1 + b2 + b3

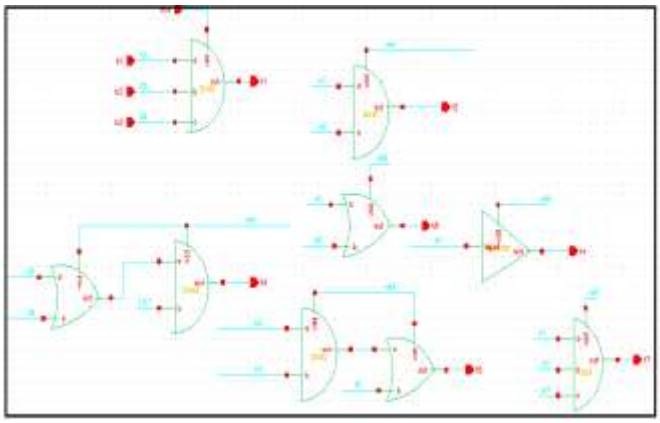

Fig 2.1: Schematic of Binary to thermometer Decoder

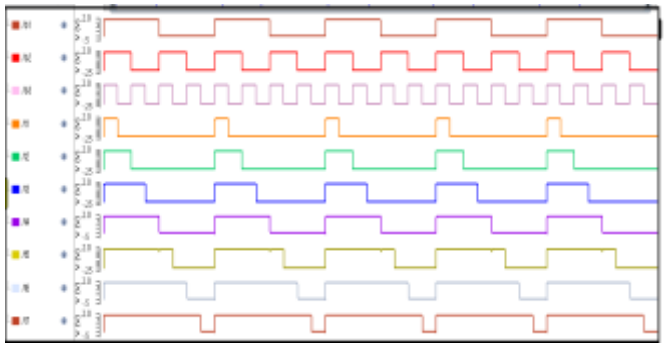

Fig.2.2: Waveform of Binary to thermometer Decoder

B. Switch Driver

The dynamic performance degradation of a current-steering D/A converter can be caused by several reasons. Some important issues that have been identified to cause dynamic limitations are:

1) Imperfect synchronization of the control signals at the switches;

2) Drain-voltage variation of the current-source transistors.

3) Coup ling of the control signals through the switches to the output.

To minimize these three effects, a well designed and carefully laid out synchronized driver is used. A major function of this driver is shifting the crossing point of the switch transistors differential control signals, in such a way that these transistors are never simultaneously in the off state [2]. The driver also performs the final synchronization. By placing it in front of the switches and by paying much attention to symmetrical interconnections in the layout, the difference in delay between the different digital decoder outputs is minimized. Furthermore, the dynamic error caused by the parasitic gate drain feed through capacitance is significantly lowered by the use of a reduced voltage swing at the input of the switches. This

reduced voltage swing is achieved by lowering the power supply of the digital driver. The circuit schematic of the driver circuit in this design is given in Fig. 2.3. Here Vpulse is (Inp) applied to one of the two inputs of switch Driver and inverted input (Inn) is applied to other input of Switch Driver. This switch Driver gives the inverted output to both the inputs.

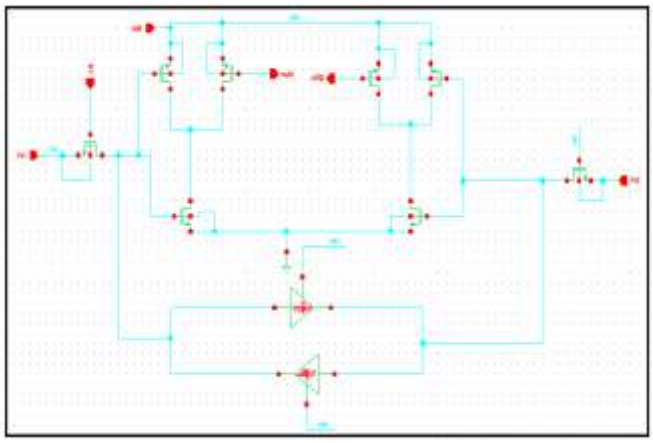

Fig.2.3: Schematic of Switch Driver

C. Differential Switch

Fig. 2.4: shows Switch element. Switch means ON or OFF. Here the switch voltage more than threshold voltage then only the transistor will be ON otherwise it will be OFF.

To ensure the correct operation, transistors should be in the saturation region. The output from the current source is connected to the input of switch element. The current from input is same as the summation of both output currents.

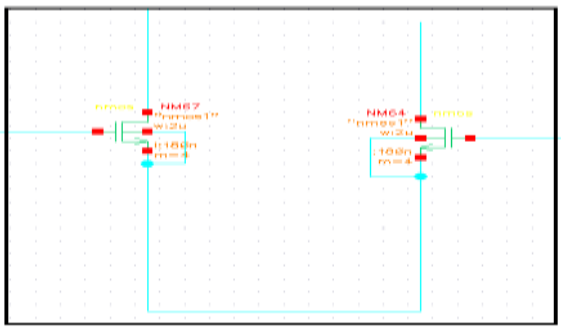

Fig.2.4: Schematic of differential Switch

D. Cascode Current Mirror

The Cascoded current mirror is as shown in Fig. 2.5. There are two Cascoded transistors with the current mirror. The preparatory action is made by using the feedback, to supply the current to Cascoded circuit and the feedback acts like a buffer. By doing Cascoding output impedance will be increased and have better accuracy but it reduces flexibility. The Cascoded current mirror has some advantages like, with the help of Cascode transistors, the channel length modulation effect is eliminated in Cascode current mirror, and output impedance is high. And it has also some disadvantages like; accuracy is less, current is constant when the V_{ds} is large because of the body effect the output current will disturb.

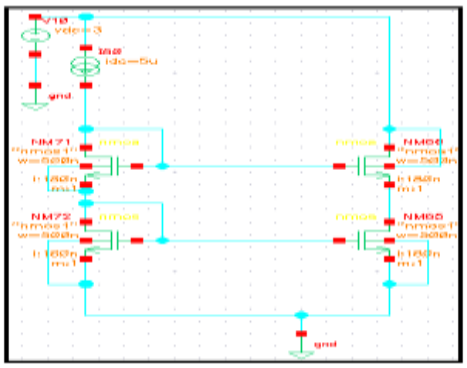

Fig.2.5: Schematic of Cascode Current Mirror

Fig. 2.6 shows a 3-bit binary-weighted DAC with seven unit elements (U_7, U_6,....U_1). Conventional binary to thermometer DAC will converts binary codes into unary codes. Here the three binary inputs B_3, B_2 and B_1 given to the Thermometer decoder so it will converts into seven unary bits such as U_7, U_6,....U_1 for ex; when the binary inputs 000 giving to Thermometer decoder then it will converts into seven unary bits like 0000000.These unary bits will give it to Switch Driver so Switch Driver will take Differential inputs and clock signal then it will gives the Differential outputs so depends on their outputs differential switch will be ON or OFF. Binary to Thermometer coder will be converted into seven elements 0000001 when the binary input increase by 1 bit 001. By doing this the output of the Thermometer decoder follows the monotonicity. These outputs of the thermometer decoder are connected to the input of the switch driver.

The major function of the switch driver is shifting the cross point of the switching transistors differential control signal, in such way that these transistor are never OFF simultaneously. These outputs of the switch driver is connected to the switches of differential controls signal. Differential switches are never off simultaneously if both the switches are glitch produced at the output so any time one switch should be ON. If one switch is ON the tale current is passing through the switch to the output. Here termination resistor will converts current to voltage at the output. So that will get step at the output similarly it follows

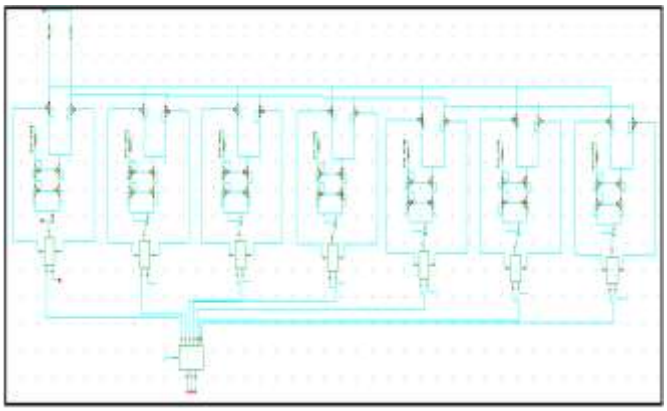

Fig. 2.6: Schematic of 3 bit Unary Weighted DAC

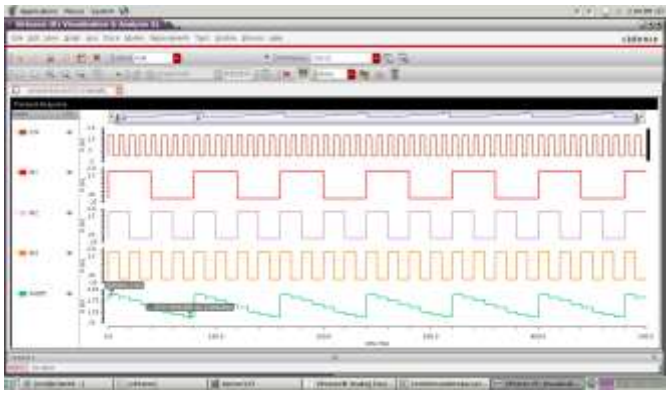

Fig. 2.7: Waveform of 3 bit unary weighted DAC

In order to reduce the size of the DAC, small transistors need to be used for both the current sources and the switches. The DEM technique in is adopted to reduce the nonlinearity effects due to the mismatch of small transistors.

E. SFDR calculation for 3 bit DAC

1) Highest harmonic = 2.164V and
2) Second highest harmonic = 0.419V
3) First harmonic 20 log(2.164) = 6.7dB .
4) Second harmonic 20 log(0.419) = -7.55dB
5) SFDR = 14.25dB

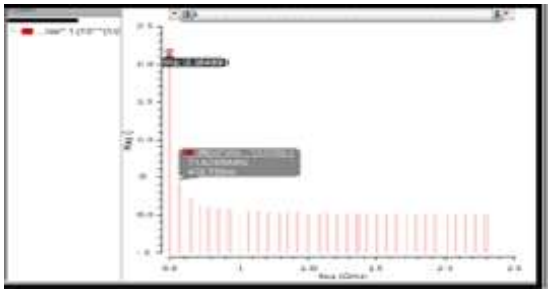

Fig.2.8: SFDR calculation of 3bit Unary DAC

SFDR means difference between Fundamental signal and highest harmonic in the Spectrum.

Table 2.2 obtained Specifications of 3 bit current steering DAC

Specifications	Range/values
Supply voltage	3V
Output swing	1V
Termination Resistance	50ohm
Sampling rate	2GS/s
Technology	UMC180nm
Resolution	3bits
SFDR	14.25dB

III. IMPROVE SFDR IN DAC

A critical challenge for DAC design is to realize a High Spurious Dynamic Range (SFDR). To meet this challenge two problems must be solved. First one parasitic capacitance induced finite output impedance and Current source mismatch. For the first problem, the parasitic capacitance of current sources lowers the high frequency output impedance and there by deteriorates the signal bandwidth of DACs. Current steering with Cascoded transistors are commonly used to increase the output impedance [1]. However the parasitic capacitance due to large transistors used for lower mismatch still limits the high frequency output impedance.

In this paper, by reducing the mismatch effect the current sources including the Cascode transistors are designed to be as small as possible to reduce the parasitic capacitance and increase the high frequency output impedance.

The second problem is the nonlinearity coming from the mismatch of current sources with small transistors. To enable the use of small transistors, several methods have been proposed to prevent the current source mismatch effect from deteriorating the performance, such as calibration circuits to directly compensate the mismatch error and Dynamic Element Matching (DEM) techniques to randomize the selection of current sources to reduce mismatch effects. DEM technique requires less circuit overhead and complexity, and thus can be effectively used to reduce the mismatch effect and transistor size. By using a DEM technique, the chip area can be smaller, allowing for shorter wires and smaller parasitic capacitance, thereby widening the signal bandwidth and shortening the wires for reducing timing skew.

A. Principle of Random Rotation Based Binary Weighted Selection

A DEM method, RRBS is proposed which offers the circuit simplicity of binary-weighted coding and greatly

reduces the mismatch effect. Compared with the conventional binary-weighted architecture, the switching activity of RRBS is improved and the glitch energy issues are inherently reduced by randomization. Although its switching activity is not near-minimum, the binary to thermometer decoder is not required, thereby further saving chip area. As a result, the required implementation area is lower when compared to all other DEM architectures.

A conventional binary-weighted DAC is generally operated with current groups where each group is binary-weighted, and formed with predetermined members of a unit current-source array. Each group is controlled by a digit of binary input for connecting to or disconnecting from the DAC

output. **Fig.3.1** shows the schematic of the proposed current-steering DAC with the RRBS method. RRBS efficiently performs DEM by randomly rotating the sequence of a unit current-source array to form new binary-weighted current groups for each DAC output. Unlike prior DEM techniques with extra binary-to-thermometer decoders and complex algorithm logic, the proposed RRBS is implemented with a simple randomizer circuit and without binary to thermometer decoders.

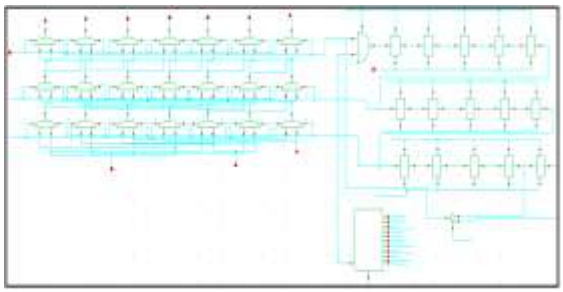

Fig.3.1 Schematic of RRBS

Depending upon the three given inputs (B2, B1,B0) , the outputs are obtained. For example,

- if "000" is given as input, then the output obtained is "0000 000".
- if "001" is given as input, then the output obtained is the value of One(1) Somewhere in seven Zeros.
- if "010" is given as input, then the output obtained is the value of two One(s11) Somewhere in seven Zeros so on.
- if "111" is given as input, then the output obtained is "1111 111".

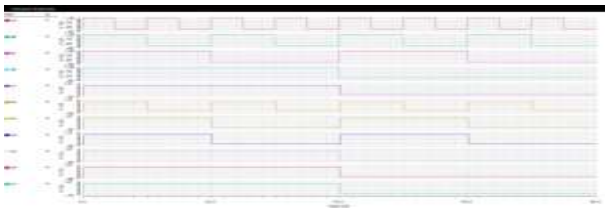

Fig.3.2 waveform of RRBS

Fig 3.2 Shows as operating principle Conventional binary weighted and RRBS .Thus a DEM coder, which contains a Rotator and a Pseudo Random Number Generator with 16 bit length, is used to replace the conventional binary to thermal coder to realize the DEM technique. The operation of the DEM technique with three input codes, 110, 001 and 110, where the R represents a random rotation step ranging from 0 to 6. For the first signal phase with R equal to 0, B_3, B_2 and B_1 control $U_7U_6U_5U_4$, U_3U_2 and U_1 respectively. For the second signal phase with R equal to 6, B_3, B_2 and B_1 are rotated 6 steps counterclockwise, with respect to the conventional operation, to control $U_7U_6U_5U_4$, U_3U_2 and U_1 respectively. For the third signal phase with R equal to 2, B_3, B_2 and B_1 are rotated 2 steps counterclockwise, with respect to the conventional operation, to control $U_2U_1U_7U_6$, U_5U_4 and U_3 respectively. In brief, the controlled unit elements are randomized by the random number R to suppress mismatch-induced distortions.

B. 12 bit Current steering Unary Weighted DAC

Fig. 3.3 shows the architecture of the proposed 12 bit DAC with Unary weighted DAC, which is segmented into 3 MSB bits, 3 upper LSB (ULSB) bits, 3 LSB bits, 3 lower LSB bits. The current weighting of the LLSB bit is defined as $I_{LLSB.}$ The current weighting of the other segments are $I_{MSB} = 512\ I_{LLSB,}$ $I_{ULSB} = 64\ I_{LLSB}$, $I_{LSB} = 8\ I_{LLSB}$ mismatch effect is negligible by using of segmentation approach.

This design chooses unit-element current-steering topology. There are four major portions in this design:

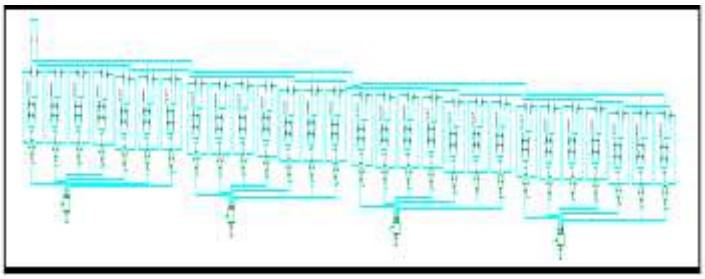

Fig 3.3: Schematic of 12 bit DAC

C. *Circuit Analysis of 12 bit current steering DAC:*

Vdd=3 V, Vref = 1V, Termination Resistance = 50ohm

Iout = 1V/50ohm = 20mA;

I_{LSB} = 20mA/ 2^{12}: I_{LSB} = 20mA/4096

I(Unit current)=5uA.

V_{LSB} = 1V/8 = 0.244mV

Table 3.1 Obtained Specifications of 12 bit current steering DAC.

Specifications	Range/values
Supply voltage	3V
Output swing	1V
Termination Resistance	50ohm
Sampling rate	2GS/s
Technology	UMC180nm
Resolution	12bits

D. *Frequency response of 12 bit DAC*

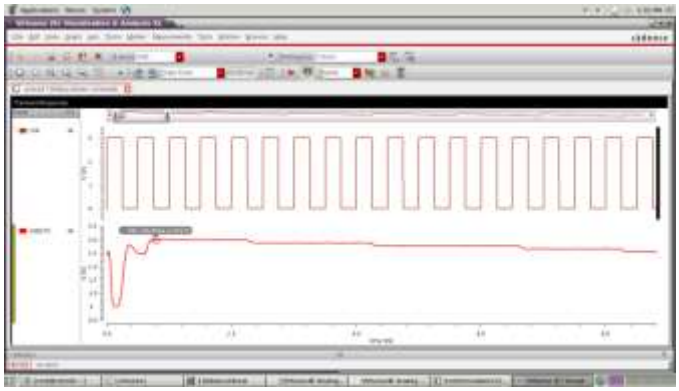

Fig.3.4 Frequency response plot of 12 bit DAC

Here inputs are given 500ps Time period and 250ps pulse width. From the above Fig.4.3 plot Frequency. The DAC output is changed after 788.63ps. So Speed of the DAC is = 1/788.63ps = 1.268GHz.

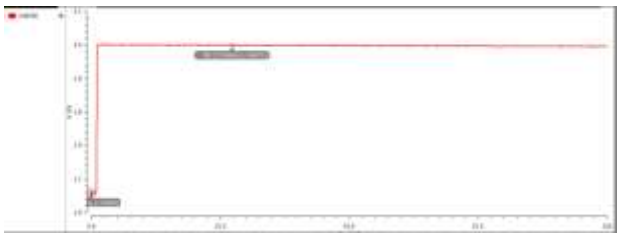

Fig 3.5: 12 bit DAC output Plot

E. Obtained specifications of 12 bit DAC

Table 5.1 Designed and obtained for designed 12 bit DAC

Specifications	Desired	Obtained
Input Supply Voltage (Vdd)	**3V**	**3V**
Input Current (Idc)	**5uA**	**5uA**
Output Voltage swing	**1V**	**0.9V**
Resolution	**12**	**12**
Sampling Frequency	**2GS/s**	**1.27GS/s**
Termination Resistance	**50 ohm**	**50 ohm**
Technology	**UMC 180nm**	**UMC 180nm**

IV.CONCLUSION

In this paper Current steering 12-bit DAC was proposed to improve Sampling Frequency for high speed application. The implemented DAC achieves Sampling Frequency at 1.27 GS/s. The proposed Segmented DAC is suitable for high speed and high resolution current steering DACs.

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