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Design of Fault Injection Technique for Digital HDL Models

A. S. Kalbande

M.TECH, (Electronics system and Communication Engineering), GCOEA, Amravati, India

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Abstract - *Faults are occurred in the VLSI chips. Detecting the fault in the digital circuit is hard process. Detecting the multiple number of time fault has shown to outcome in defect coverage. Fully specified bit increases the complexity of test process. S27 Benchmark circuit, Maximally Redundant Sign Digit (MRSD) Adder and Carry Select Adder (CSA) has been used for testing purpose, where S denotes sequential. Test sequences are produced randomly. The Generated pattern move through the whole circuit, and compares it with the faults which are present in the circuit component. The faulty output of the digital circuit is compare with normal output of the circuit. If both the response are same the then it consider as the fault free circuit, if the response differ from each other then it consider as faulty. In this way, various patterns detect the different faults or same faults. Fault injection is done at the coding phase. Simulation based fault injection and detection gives high observability and controllability of circuit which has taken under test consideration. Stuck at zero, stuck at one and bit flip fault are considered. Fault injection gives ability of fault insertion before genuine implementation, it assist in evaluating the testability of digital system.*

Key Words: *— Fault injection, Fault simulation, Fault injector, VHDL fault models*

1. INTRODUCTION

After the manufacturing of the VLSI chip, it is tested for the defects present in it. But it is not all possible to generate similar defects in the actual circuit or apply the test to all possible defects in the chip. So defects are modeled as fault to ease the test generation process. From the various fault model proposed the single stuck at fault model is widely acceptable because it is closed to the actual defects. However, the smaller levels are wanted for devices and circuits in most applications better fault models are needed which can accurately model the defects. Such fault model tends to be a complex making test generation even harder or impossible.

- *Permanent faults:* It is caused by the irreversible component damage create permanent fault.
- *Transient faults:* It is caused due to environmental condition such as power-line fluctuation, electromagnetic interference or radiation get created.
- *Intermittent faults:* It is caused by changing the hardware or unstable hardware states. It can be replacement or redesign this faults can repaired.

There are four types of fault injection process which given as fallow.

Hardware-based fault injection: In this technique at the physical level faults are injected. Injector produce change in voltage or current and it has real and direct physical contact with target system. Target system which has not direct physical contact with injector some phenomenon like radiation, interference cause false current inside the target system.

Software-based fault injection: The aim of this technique is introducing errors at software level that occurred in hardware level. It can be targeted to applications and operating systems.

Simulation-based fault injection: The target of this procedure is faults insertion at high-level of models. It assist all system cogitation level. It gives full control of both injection process and fault model. In this method target system and possible hardware fault are model and simulate by software program.

Emulation-based fault injection: Field Programmable Gate Arrays (FPGAs) has used for fault injection. The main objective is effective circuit emulation and speeding-up fault simulation.

2. LITERATURE REVIEW

Fault injection is done by using various algorithms which define as fallow.

Lavanyashree B.J presented, 'Design of Fault Injection Technique for VLSI Digital Circuits' is an efficient fault insertion technique for cover-up all possible fault occurrences and speed up the fault injection. They have taken two benchmark circuit one is S27 circuit and another is maximally redundant sign digit adder circuit. The demultiplexer based fault injection technique is chosen. Fault are injected in the coding phase. This technique automatically inject fault in all faulty point. One normal fault free circuit is consider and it output response saved in the stored memory. Two or more copies in which fault are inserted are taken into considerations. The output of faulty copies compared with the normal copy in the comparator block.

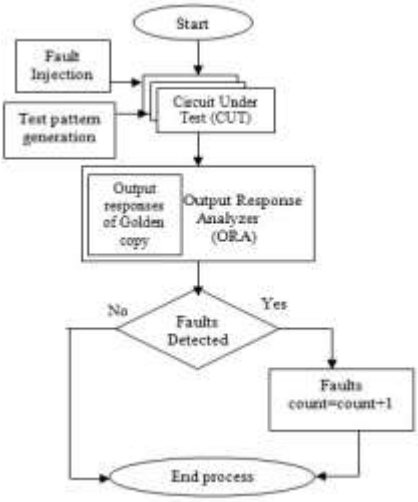

Figure 1: Methodology

Abdul Rafay Khatri, Ali Hayek, and Josef Borcsok[2] presented, 'ATPG Method with a Hybrid Compaction Technique for Combinational Digital Systems' a simple hybrid compaction technique. It is an instrumentation based technique in which extra circuit are added which is used to inject fault in target system. Hybrid compaction method quicken up the fault detection process, the most compact set of test vector can be find out by this method. The hybrid compaction include both static and dynamic compaction. Test pattern generation process is very fast process. Using hybrid compaction the compaction of test vector had done and compared with state-of-the-art methods. Fault coverage can be calculated as given below,

$$Fault\ coverage = \frac{Number\ of\ fault\ detected}{Number\ of\ fault\ injected} \text{ x } 100\%.$$

Mohammad Shokrolah-Shrirazi and Seyed Ghassem Miremadi [3] presented, 'FPGA-based Fault Injection into Synthesizable Verilog HDL Models'. The FPGA based fault injection tool says as FITO. FITO is made up of three sections.

- Source code modifier and fault list generator,
- Fault injection manager
- Result analyzer.

Permanent and transient fault model are presented in the gate level fault model. Fault insertion process can be completed by adding some additional gates and wires to the initial circuit. One of the extra wire in Fault Injection Signal (FIS) which play the important function in the fault insertion experiment. With choosing the FIS signal permeant fault is injected into the already declared wire. FPGA-based fault injection tool called FITO tool that support gate level fault model and RTL level fault injection model. Synthesizable improved Verilog source code of the targeted system can be generated by FITO. Software part of FITO is source code modifier, fault list generator and result analyzer which are located into the host of the computer. There are three phases of FITO. The setup Phase, the emulation phase and the evaluation phase. Main objective of setup phase phase is to modify the Verilog source code. In emulation phase code created by previous phase are emulated. In evaluation phase fault tolerance parameter estimated. It is done in the result analyzer part in FITO. FITO delivers controllability over 255 wire and register of targeted microprocessor.

Ms. Humera Fatima, Ms. Imthiyazunnisa Begum and D. Naga Poornima [8] has presented, high speed fault injection process for creating fault tolerant system. Fault injection technique is validation technique for dependability of the fault tolerant system. There are two type of fault injection method, one is hardware oriented fault injection method another is software oriented fault injection method. In the hardware system fault insertion can be implemented with three main technique. Physical fault injection, Software implemented fault injection and simulated fault injection. Real time fault injection is done by using the fault injection manager. Fault injection manager consist of the VHDL package, fault scheduler and fault insertion components. VHDL file is automatically modified and updated by the C program every time. The author purposed double ALU based fault tolerant mechanism for handling the soft error. FITO support several synthesizable fault model for analysis of dependability. For supporting bit-flip model FITO provided with additional signal like FIS and Bit with one multiplexer. Fault injection component are gate with FIS regulate to insert the fault with FIS is active high. Fault insertion becomes easier with implementation of following steps, to generate code to present the signal with same size of the port on which the fault need to be injected, addition of the analogous fault insertion component instance interlinking the port signal. Both output signal and line control by FIS. Replace all the port signal instance with declared new signal.

In [9] P.K.Lala proposed VHDL level description for sequential and combinational circuit In this paper fault injection system is proposed and fault insertion block is included in package body. This system method give independence to design to control the VHDL package for injecting the fault on each signal inside the block of VHDL code. To insert the fault in program code at any selected point called checkpoint is permitted by the permanent fault. The simple function call at the beginning of VHDL code and instantiation of component is require to actuate the injection mechanism. In injection system for checking fault injection into given system two linear feedback shift register (LFSR) are used. Random sequence can be generated with LFSR. Fault injection One-Hot Encoded shift resister and logic block keep an eye on the control inputs to the circuit and determine ether it need to perform transient and permanent fault injection in the data. It also decide fault has occurred on which bit. The

rate of fault injection is governed at control logic block. For evaluating the testability of a system which is digital before it actually carry out and actually helped by the capability of injecting transient and permanent fault. Technique which is fault injection give access VHDL package to insert fault in each block.

3. RESULTS

Three circuits or digital models are taken under consideration for carry out the fault analysis are s27 sequential benchmark circuit another one is Maximally Redundant Sign Digit (MRSD) Adder and last Carry Select (CSA) Adder.

3.1 S27 sequential benchmark digital circuit

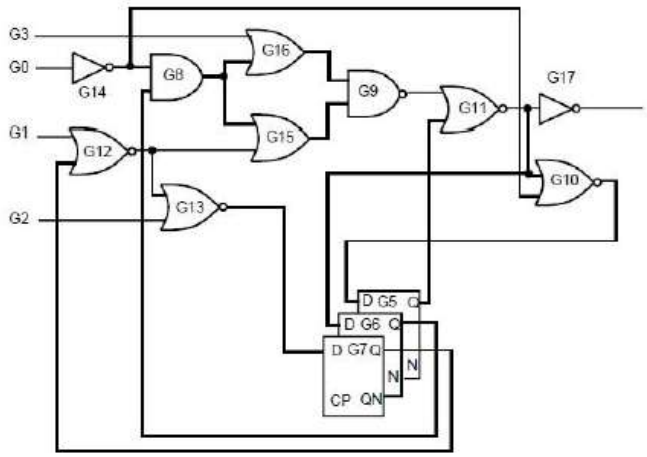

Figure 2: s27 sequential benchmark circuit

It purely a sequential circuit with four input and one output, three D-type flip-flop, two inverters, one AND gate , one NAND gate, two OR gates and four NOR gates. Circuit has been tested for built in self test.

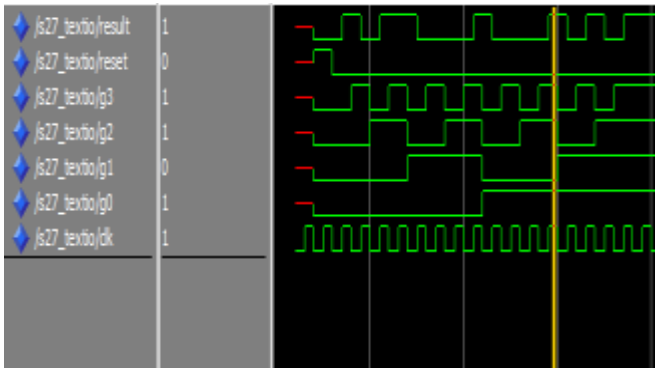

Figure 3: Normal output of the s27 sequential circuit

The fault is added in the tg8out, tg15out and tg9out location. After adding the fault the circuit is again simulated and faulty output is obtain. In faulty circuit timing diagram the fault is propagated from one node to another till it reaches to the output node.

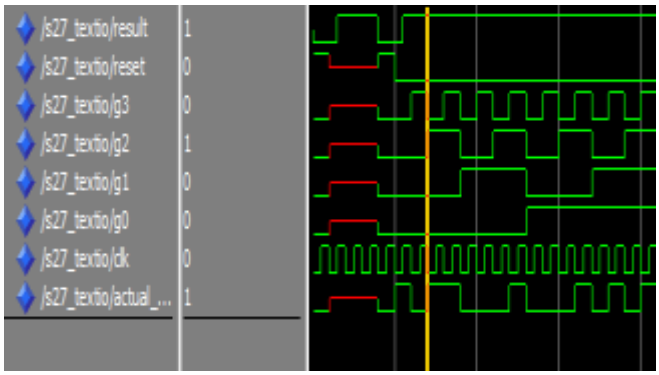

Figure 4: Faulty output of s27 sequential circuit

Table 1: Synthesis report of the s27 circuit

Parameters	Value
Total logic elements used	10
Total Registers	10
Time Delay T_{pd}	7.675 ns
Frequency	130.30 Mhz
Throughput	130.30 Mbps
Total thermal power dissipation	112.20 mW
Core static power dissipation	79.93 mW
I\O thermal power dissipation	30.77 mW

3.2 Maximally Redundant Sign Digit (MRSD) Adder

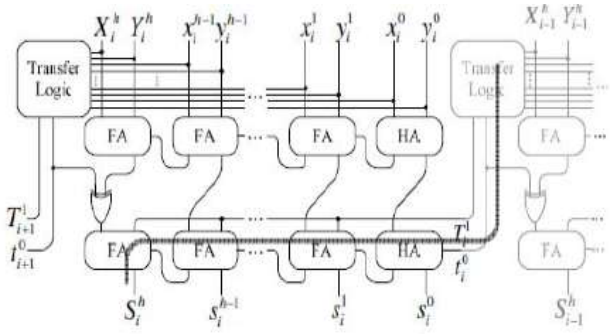

Figure 5: MRSD adder circuit

MRSD adder is implemented using eight full adder and two half adder. Previous stage output is feed to the next full adder circuit.

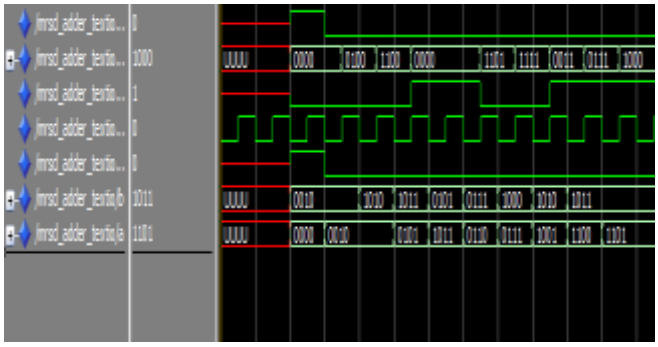

Figure 6: Normal output of MRSD adder circuit

The fault is added in $C_0(0)$, $C_0(2)$, $C_1(0)$ and $C_1(2)$position in the circuit which are tested for the stuck at faults and bit flip fault. Circuit is simulate and timing diagram is observed.

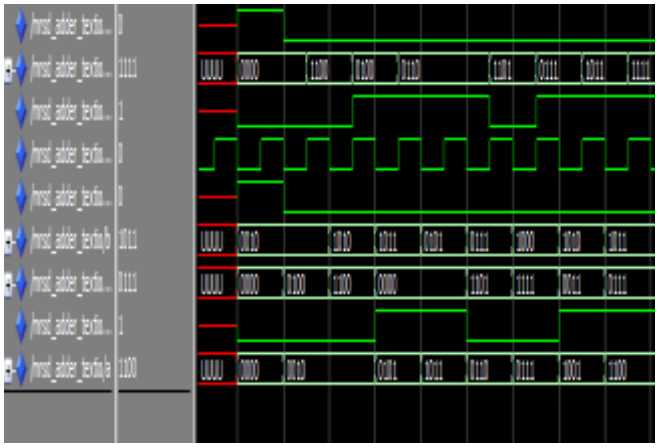

Table 2: Synthesis report of the MRSD adder circuit

Parameters	Value
Total logic elements used	13
Total Registers	5
Time Delay T_{pd}	8.915 ns
Frequency	112.17 Mhz
Throughput	112.17 Mbps
Total thermal power dissipation	111.75 mW
Core static power dissipation	79.93 mW
I\O thermal power dissipation	31.82 mW

3.3 Carry Select Adder (CSA)

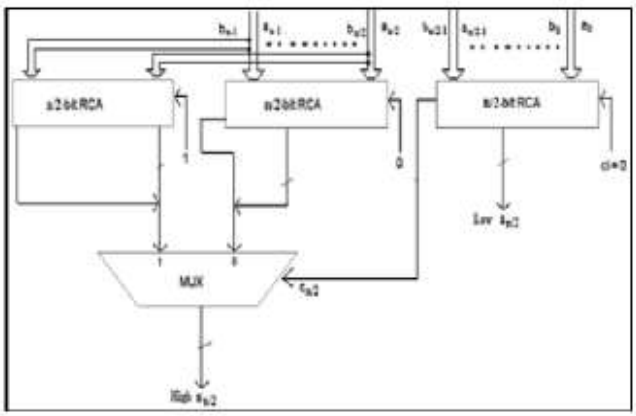

Figure 8: Carry select adder circuit

Carry select adder is implemented using the four full adder which are used in making of the two ripple carry adder.

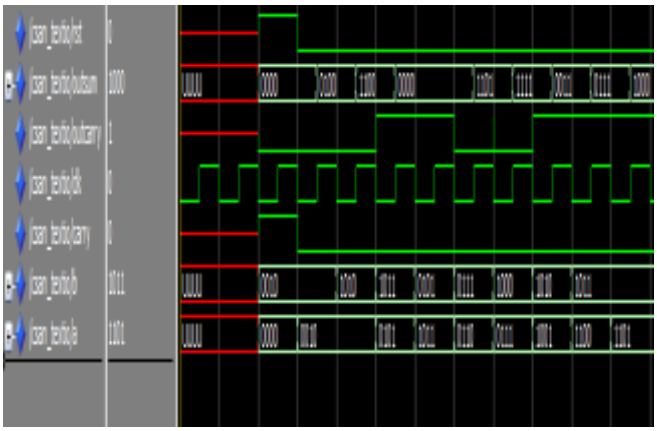

Figure 9: Normal output of Carry select adder circuit

Faults are added into the CSA circuit at carry and $C_0(3)$ position. The fault is propagated to each node and outputted at last output node.

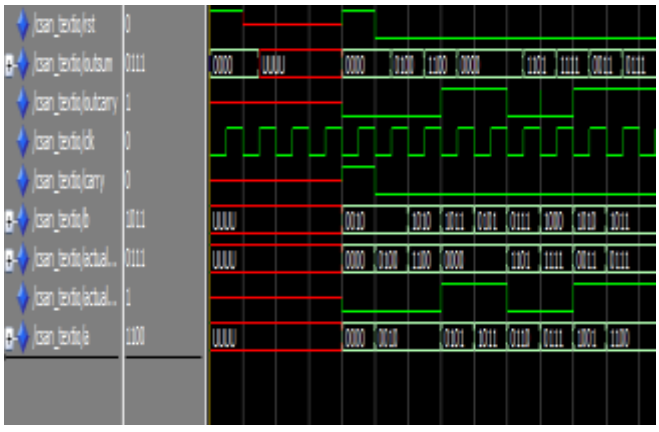

Figure 10: Faulty output of the Carry select adder

Table 3: Synthesis report of Carry select adder circuit

Parameters	Value
Total logic elements used	13
Total Registers	8
Time Delay T_{pd}	13.96 ns
Frequency	71.63 Mhz
Throughput	71.63 Mbps
Total thermal power dissipation	111.71 mW
Core static power dissipation	79.93 mW
I\O thermal power dissipation	31.78 mW

These are the synthesis report of the three circuit s27 circuit, MRSD adder circuit and carry select adder (CSA) circuit. The s27 circuit require less number of the total logic elements and MRSD adder and CSA adder require the same amount of the total logic elements.

4. CONCLUSION

Fault injection is important process in for creating the fault tolerant system and evaluating the design metrics. Fault injection involve fault insertion and observe its behavior. Faults injection are done at coding phase. Out of the four fault injection technique the simulation based fault injection technique is most popular technique. Using this technique maximum controllability and observability can achieve. The s27 circuit require least number of the total logic elements. Also it has the highest number of throughput. The total thermal power dissipation is highest in the s27 circuit.

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