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A NOVEL MODIFIED SWITCHED CAPACITOR NINE LEVEL INVERTER TOPOLOGY WITH REDUCED SWITCH COUNT FOR HIGH FREQUENCY AC POWER DISTRIBUTION

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Abstract - *This project proposes a new topology of switched-capacitor multilevel inverter with reduced switch count for high frequency AC power distribution systems. Due to reduced switch count of this proposed topology, the size, weight and cost of the switched capacitor multilevel inverter is reduced. The proposed topology produces a staircase waveform with nine level output voltage employing fewer components compared to several existing multilevel inverters. This project deals with harmonic reduction content for switched capacitor multilevel inverter with asymmetric dc sources. It can also step-up the input supply voltage without using a bulky transformer. Utilizing the available DC sources from renewable energy farms as inputs for a single inverter solves the major problem of connecting several inverters in parallel. This inverter inherently solves the problem of capacitor voltage balancing as each capacitor is charged to the value equal to one of input voltage every cycle. The modulation technique used for switched capacitor multilevel inverter is Level Shifted multicarrier Pulse Width Modulation. The total harmonic distortion is found out through five different types of level shifted multicarrier pulse width modulation. The performance and feasibility of the proposed multilevel inverter topology is modelled and simulated using MATLAB/Simulink..*

Key Words: **Switched capacitor, multilevel inverter, H-bridge, Level shifted multicarrier pulse width modulation, high frequency dc to ac inverter.**

I. INTRODUCTION

High Frequency Alternating Current Power Distribution Systems (HFAC PDS) provide more advantages over conventional DC PDS .HFAC PDS does not require the rectifier and a filter stage in front end, and an inverter stage in the point of load power supply [1], [2].]. The certain reduction in the number of power conversion stages results in less component number, which will improve reliability and efficiency, and further reducing the cost. HFAC PDS will reduce the size of passive components which leads to higher power density systems, and it improves heat distribution and has ability to employ connector-less power transfer. Smaller output capacitors may improve dynamic response. High-voltage low-current distribution can easily be obtained by using compact HF transformers. It provides the flexibility to satisfy loads at different voltage levels, provide galvanic isolation and are crucial to realize connector-less power transfer. Switching off a large magnitude of AC when passing through a zero is simple when compared to switch off large DC. More studies show that frequencies over 10 kHz are safer to human cells and tissues than DC [1]. These exciting features and benefits over DC PDS makes HFAC PDS a more promising alternative for future power net.HFAC PDS architecture consists of a front-end HFAC power source, a HF distribution line and point-of-load voltage regulator modules. These systems employ resonant converters which will enhance efficiency, power factor and energy density, and alleviate adverse EMI effects. In 1980s, NASA make research on HFAC PDS for its space station. A single phase system rated at 25 kW include 20 kHz line frequency and $440V_{rms}$ line voltage was done successfully [3]. At this frequency, the energy transferred per cycle which will reduced by 50 times as compared to a 400 Hz system (which may failed to provide efficient and reliable solution [4]). The number of components is lowered by a factor of 5 and power loss will be reduced by 67% when compared to three-phase systems [1].

Papers claim and conclude that HFAC scheme solve more problems in efficient power delivery. This paper which mainly concentrate on switched-capacitor multilevel inverters (SCMLI) as input sources for HFAC PDS.

High Frequency AC (HFAC) Power Systems provide frequencies higher than the usual 60 Hz – may have more benefits in certain applications, such as telecommunication, computer and aerospace systems has been presented in [7] and also extend to lighting systems [2], motor drives, automotives [8] and gate drivers [9], especially where small size and weight is more significant (aircraft, ships, etc.), or in place of variable operating

speed increases efficiency. While 400 Hz systems are widely used in aircraft, which never include parallel-connected generators that operate at megawatt power levels for many industrial [10] and commercial applications, especially ship and marine systems.

The enhancement in number of voltage levels may have synthesized output waveform with more steps, which reduces the harmonic content in the output. MLI can be generally classified into neutral point clamped, capacitor clamped and cascaded types [11]. Unbalanced DC link capacitor voltage and more component count to obtain higher output voltage levels are the main drawbacks for diode clamped (DCI) and capacitor clamped (CCI) types, whereas cascaded H-bridge (CHB) MLI need relatively higher number of isolated DC voltage sources to obtain higher output voltage levels. Coupled inductor based MLI have been presented in [12], [13]. This structure is simpler but it is not feasible to obtain higher levels.

Renewable energy farms may have more DC sources, usually batteries. These inverters can effectively be needed in such renewable energy based microgrids as it employs multiple DC input sources of different magnitude. HFAC PDS include compact transformers, smaller filters and high density power converters which will provide several benefits to the micro-grids user.

Multilevel inverters (MLI) may overcome exciting features they offer MLI output staircase waveforms which greatly reduces the harmonic content when compared to conventional square wave inverters. MLI can be generally classified into diode clamped, capacitor clamped (also known as flying capacitor) and cascaded multilevel inverters [10], [11]. Diode clamped MLI demand several additional diodes for enhancing the output voltage levels and the capacitor voltages are unbalanced and it requires high voltage rating for the blocking diodes .Capacitor clamped MLI also suffer from voltage imbalance issue and need several additional storage capacitors for increasing the output voltage level which makes it more expensive and difficult during the package process. The main drawback in cascaded MLI need separate isolated DC sources.

2. SWITCHED CAPACITOR MULTILEVEL INVERTER:

Switched-Capacitor Multilevel Inverters (SCMLI) have been gaining more attention over the recent few years [15] – [20]. SCMLI is used mainly to solve the problem of unbalanced capacitor voltages. SCMLI offer the benefit to convert input voltage to integral multiple output levels without using inductors. This voltage conversion is achieved by charging the SCs to input voltage magnitude first (by connecting SC in parallel to source) and then connecting the input voltage source and SCs in series to the load.

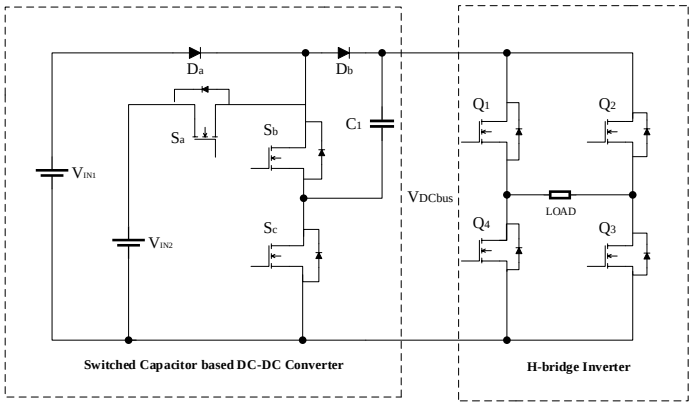


Fig -1: Proposed Switched capacitor multilevel inverter

A nine-level SCMLI using series-parallel conversion which employ single DC source with comparison of level -shifted PWM is presented in [18]. SCMLI includes an SC doubler circuit and conventional cascaded H-bridge to obtain a relatively higher voltage step count with fewer components compared to the traditional cascaded MLI [16], [20]. The partial charging of SC technique is analysed in [15] is more complicated and difficult to control the charging profile of the boost SCMLI. In [21], a multi-source step-up SCMLI contain reduced component count which has ability to drive inductive loads is presented. Similarly, in [20], multiple sources are used along with a single SC cell to obtain a stepup SCMLI. A hybrid nineteen-level MLI which include features of both SC and flying capacitor technique is presented in [22]. Asymmetric voltage sources are used to obtain multilevel output voltage level without stepping up in [25]. SCMLI topologies in [20], [23], which includes multiple DC voltage sources. Both these types can be operated by charging the parallel SC to input voltage and discharging it while connecting in series to the load. SCMLI are especially more required for high frequency output AC inverters [13] as the size of the energy storage capacitor at high frequency is small and the quality of output waveform is better with low harmonic distortion content.

A high frequency AC micro-grid of a few kWs which includes power converters with fewer components are utilized to realize a cost effective system with higher reliability. With the proliferation in renewable energy based solar and wind farms and such multi-input topologies gain more potential. This makes the customers

to install roof top solar panels with HFAC (or even LFAC) PV inverters. The new modified SCMLI topology is used to realize a multilevel staircase output when compared to conventional topologies of MLI. The operating principle will beneficially charges the DC capacitor to a finite voltage each half cycle, which may efficiently solves the voltage imbalance problem.

3. PROPOSED TOPOLOGY WITH OPERATING PRINCIPLE:

A novel proposed topology of SCMLI (in Fig 1) includes two asymmetric input sources (V_{IN1} and V_{IN2}), three transistors (S_a, S_b, and S_c), two diodes (D_a and D_b), and a capacitor (C_1) which can be modified from existing SCMLI topology in [24] which contain two asymmetric input sources (V_{IN1} and V_{IN2}), five transistors (S_1, S_2, S_3, S_4 and S_5), three diodes (D_1 D_2 and D_3) and two capacitors (C_1 and C_2). The DC levels are achieved at inverter DC side which include V_{IN1}, $2V_{IN1}$, V_{IN2}, $V_{IN2}+V_{IN1}$. The H-bridge inverter contain transistors Q_1 to Q_4 effectively produces 8 bipolar levels and a zero (0, $\pm V_{IN1}$, $\pm 2V_{IN1}$, $\pm V_{IN2}$, $\pm(V_{IN2} + V_{IN1})$) across the load. For primary analysis, the switches and the voltage sources employed are assumed to be ideal, and kept the capacitance value large enough to maintain a constant voltage and constant output current, and neglect small voltage ripple across them. Table-I explains the proposed switching logic of the nine level SCMLI.

Output voltage = $\pm V_{IN1}$ state:

Capacitor C_1, is charged to the input voltage source V_{IN1} through D_a by turning ON transistor S_c. Transistors S_a and S_b remain turned OFF. The DC bus voltage at this state is equal to V_{IN1} as V_{IN2} is blocked by OFF transistor S_b. Fig. 3(a) depicts the equivalent state for $V_0 = +V_{IN1}$.

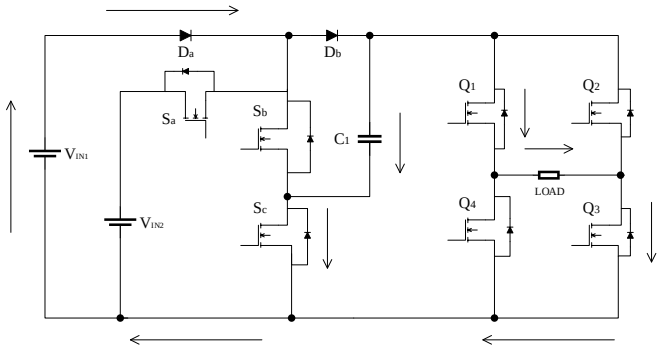


Fig. 3(a)

Output voltage = $\pm 2V_{IN1}$ state:

Transistor S_b is turned ON which connects V_{IN1} in series with capacitor C_1 (charged to V_{IN1}) through diodes D_a and D_b. At this state, V_{DCbus} is equal to $2V_{IN1}$. Transistors S_a and S_c remain turned OFF. Fig. 3(b) depicts the equivalent state for $V_0 = +2V_{IN1}$.

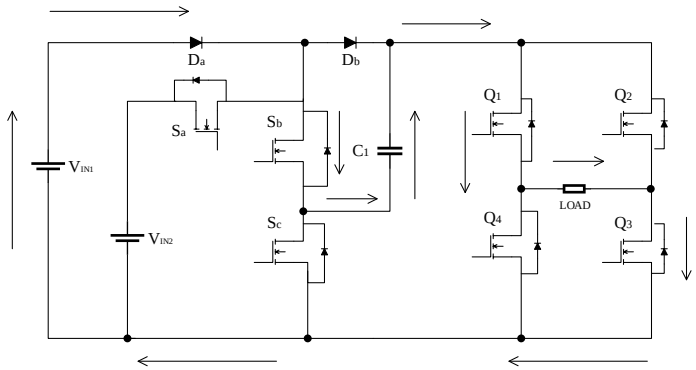


Fig. 3(b)

Output voltage = $\pm V_{IN2}$ state:

For normal operation of the proposed inverter, $V_{IN2} > V_{IN1}$. In the SC front end DC-DC converter, only transistor S_a is turned ON while other transistors S_b and S_c are turned OFF. Therefore, V_{IN2} is connected to the DC bus through diode D_b. Diode D_a are reverse biased and hence block V_{IN1}. Fig. 3(c) depicts the equivalent state for $V_0 = V_{IN2}$.

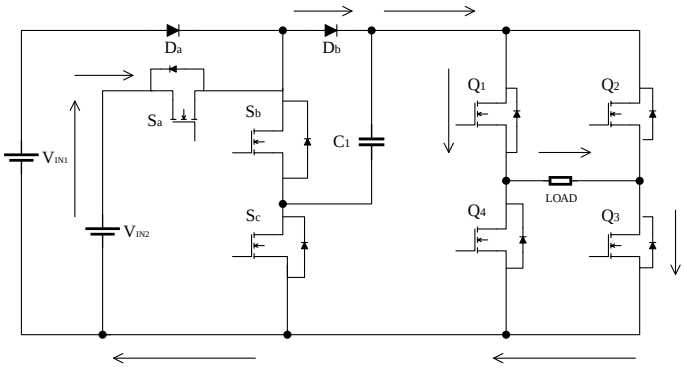


Fig. 3(c)

Output voltage = $\pm(V_{IN1} + V_{IN2})$ state:

V_{IN1} is connected in series with input voltage source V_{IN2} by turning ON transistors S_a and S_b through diodes D_a and D_b. Transistors S_c remain turned OFF The net voltage that appears across the DC bus now is equal to $V_{IN1}+ V_{IN2}$. Fig. 3(d) depicts the equivalent state for $V_0 = (V_{IN1} + V_{IN2})$.

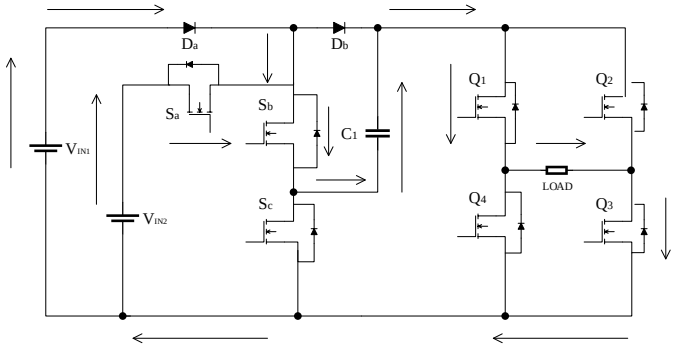


Fig. 3(d)

Output voltage = Zero level state:

To obtain zero level at the output after the positive half cycle, only transistor Q_1 is turned ON, while all the other switches in the full bridge inverter remain turned OFF. The body diode of transistor Q_2 is provided for free-wheeling. Similarly, to yield zero level at the output after the negative half cycle, only transistor Q_4 is turned ON, while all the other switches in the full bridge inverter remain turned OFF. In this case, the body diode of transistor Q_3 is employed for free-wheeling. The switches in the front end DC level shifter remain in their previous states.

Let us consider this example for (Table I) V_{IN1} = 20 V and V_{IN2} = 60 V. If V_{C2} = V_{IN1}, then the output voltage steps would be ± 20V, ±40V, ±60V and ±80V.

TABLE I: Proposed Switching logic for nine level SCMLI:

S_a	S_b	S_c	Q_1	Q_2	Q_3	Q_4	V_0
0	0	1	1	0	1	0	V_{IN1}
0	1	0	1	0	1	0	$2V_{IN0}$
1	0	0	1	0	1	0	V_{IN2}
1	1	0	1	0	1	0	$(V_{IN2}+ V_{IN1})$
0	0	1	1	0	0	0	0
0	0	1	0	1	0	1	$- V_{IN1}$
0	1	0	0	1	0	1	$-2V_{IN1}$
1	0	0	0	1	0	1	$- V_{IN2}$
1	1	0	0	1	0	1	$-(V_{IN2}+ V_{IN1})$
0	0	1	0	0	0	1	0

4. MODULATION FOR THE PROPOSED INVERTER:

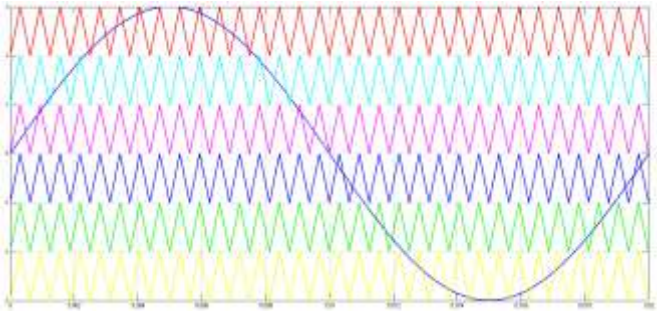
Sinusoidal Pulse Width Modulation (SPWM) is the simplest technique that can be implemented in both two level and multilevel inverters. There are two signals in SPWM a sinusoidal wave as a reference signal and a triangular wave as a high frequency carrier signal are compared to give two states (high or low). The reference is always compared with the carrier signal. If the reference is greater than the carrier signal, then the active device corresponding to that carrier is turned on, and if the reference is less than the carrier signal, then the active device corresponding to that carrier is turned off. The main advantage of pulse width modulation (PWM) control strategies is to reduce the total harmonic distortion (THD) of the output voltage. The switching frequency of the inverter is the frequency of the carrier signal. Multiple carriers PWM techniques are used always in multilevel applications. The proposed topology of this SCMLI with reduced switch count can be analysed by generating gate signals which can be produced by using Level-shifted multicarrier modulation techniques

4.1 Level-Shifted Multicarrier Modulation Techniques:

In level-shifted multicarrier modulation techniques, the modulating signal is a sine wave and the carriers are triangular waves. As the name suggests, there are several carriers which are level shifted. An m-level inverter requires (m-1) triangular carriers. All the triangular carriers have same frequency and amplitude. The level shifted multicarrier modulation techniques

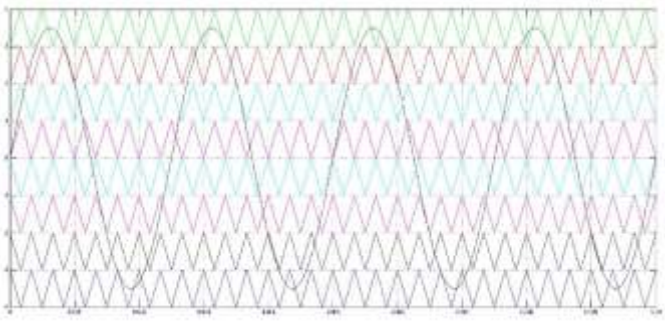
4.1.1 Phase Disposition Modulation (PD):

In this modulation scheme, all the triangular carriers are in phase. An m-level inverter need (m1) triangular carriers. The phase disposition PWM (PD-PWM) method, as one of the carrier-based PWM methods, is based on a comparison of a sinusoidal reference waveform, with vertically shifted carrier waveforms. The PD PWM method uses N-1 carrier signals to generate the N-level inverter output voltage. The carrier signals have same amplitude, Ac and same frequency, f_c and are in phase. The sinusoidal reference wave has a frequency f_r and an amplitude Ar. At each instant, the result of the comparison is decoded in order to generate the correct switching function corresponding to a given output voltage level.



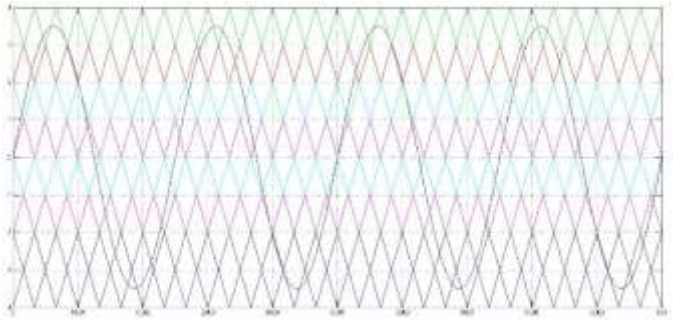
4.1.2 Phase opposite Disposition Modulation (POD):

In this modulation scheme, all the triangular carriers above the zero reference are in phase as similar to phase disposition but in opposition with those below the zero reference. An m-level inverter requires (m-1) triangular carriers. The sinusoidal reference wave has a frequency f_r and an amplitude Ar. In the POD-PWM method the carrier signals above the zero axis are all in phase. The carrier signals have the same amplitude, Ac and the same frequency, fc and are in phase above the zero reference. The carrier signals below zero are also in phase, but 180 degrees phase shifted.



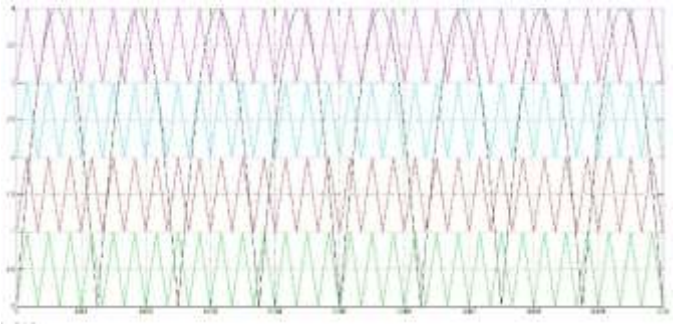
4.1.3 Alternative Phase opposite Disposition Modulation (APOD):

In this modulation scheme, all the triangular carriers are alternatively in opposite disposition. An m-level inverter need (m-1) triangular carriers. The sinusoidal reference wave has a frequency f_r and an amplitude Ar. The carrier signals have same amplitude, Ac and same frequency, fc. Alternate phase opposition disposition (APOD) modulation, every carrier waveform is out of phase with its neighboring carrier by 180 degree.



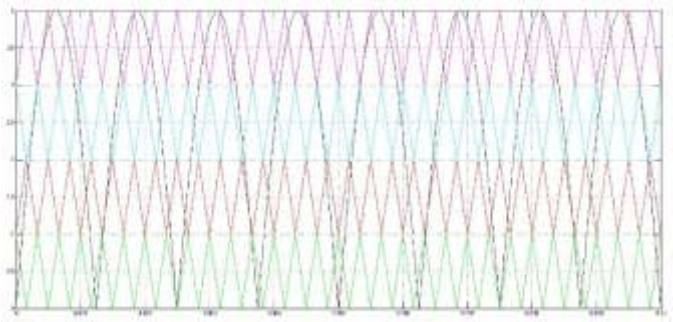
4.1.4 Modified Phase Disposition Modulation (MPD):

In this modulation scheme, all the triangular carriers are in phase similar as phase disposition shown above but the modulating signal should be a rectified sine wave. An m-level inverter requires $(m-1)/2$ triangular carriers.



4.1.5 Modified Alternative Phase Disposition Modulation (MAPOD):

In this modulation scheme, all the triangular carriers are alternatively in opposite disposition as similar as alternative phase disposition shown above the only change here to be followed that the modulating signal is a rectified sine wave. An m-level inverter need $(m-1)/2$ triangular carriers.



4.2 COST FUNCTION:

In Table I, Multi-input SCMLI topologies with symmetric output voltage levels are compared with respect to cost function (CF), similar to the cost function analysis proposed in [21], [25]. More SCMLI structures are compared to proposed SCMLI topology with respect to the number of active switches (n_T) and diodes (n_D) used, number of output voltage levels (n_l) generated and the number of voltage sources (i) by choosing the number of switched-capacitors employed (n) taken as the reference.The cost function is simplified and dependent only on the number of components specified in the below equation. It is given by -

$$C.F = \left(\frac{(2n_T+n_D+n)n_{DC}}{n_l}\right)$$

From the comparsion shown in TABLE II proposed Topology offer the least CF which means it produce higher number of symmetric output voltage levels with fewer components.

TABLE II: COMPASION OF SCMLI TOPOLOGIES:

Topology	N_T	N_D	N	N_{d2c}	N_l	CF
[16]	12	2	2	2	9	6.22
[24]	9	4	2	2	9	5.33
[24]	9	3	2	2	9	5.11
[24]	8	4	1	2	9	4.66
Proposed	7	2	1	2	9	3.77

5. SIMULATION RESULTS:

Simulation of proposed SCMLI rated with V_{IN0} = 20V and V_{IN1} = 60V employing a 560µF SC is done. Fig. 4 and 5 shows the 9-level staircase output voltage and current operating at 400 Hz. Fig 6-10 shows the harmonic spectrum of five different types of level shifted multicarrier pulse width modulation.

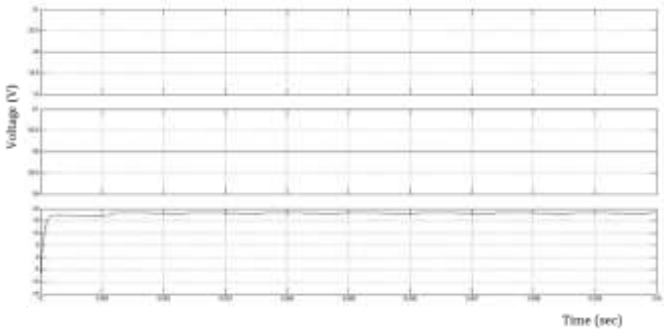


Fig -2: Input voltage for SCMLI

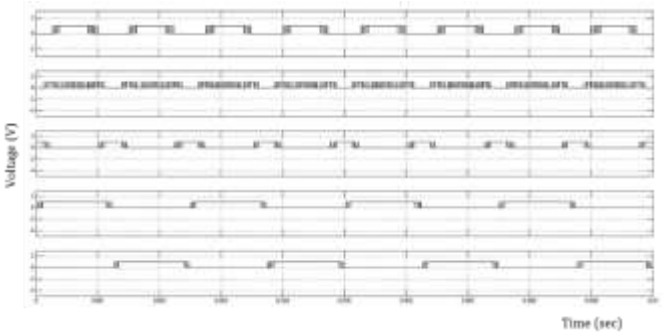


Fig -3: Gate pulse for SCMLI

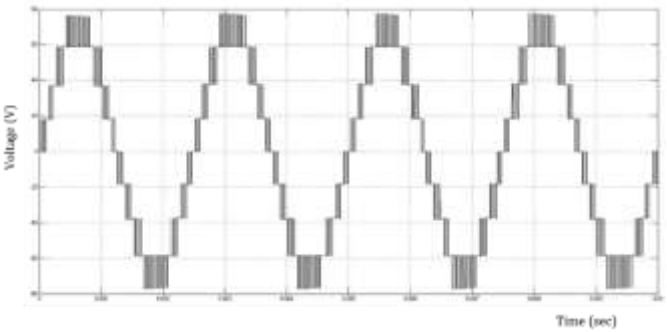


Fig -4: Output voltage for SCMLI

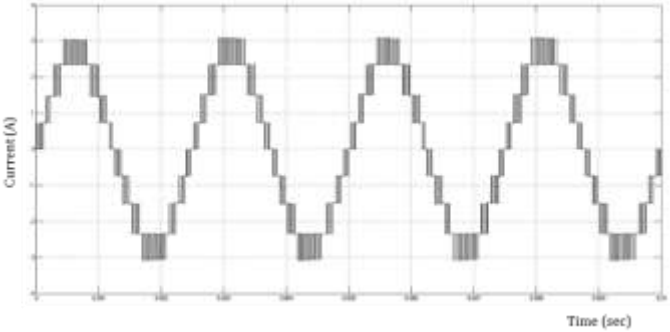


Fig -5: Output current for SCMLI

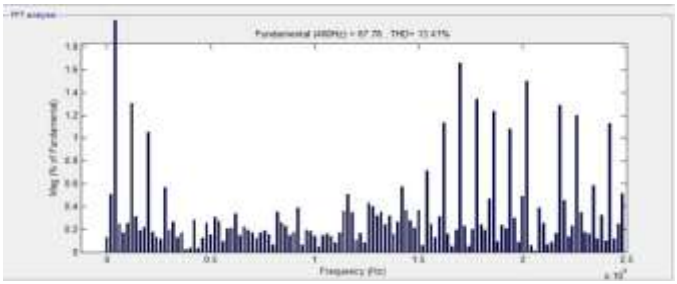


Fig -6: Harmonic Spectrum for PD

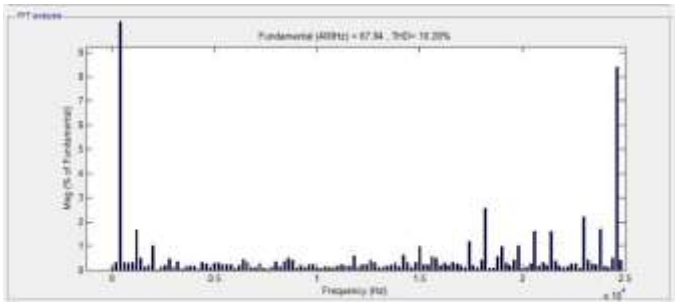


Fig -7: Harmonic Spectrum for POD

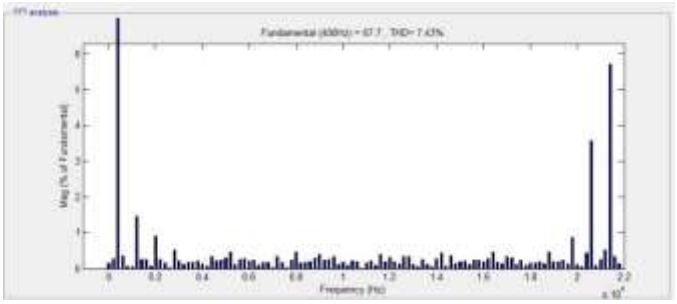


Fig -8: Harmonic Spectrum for APOD

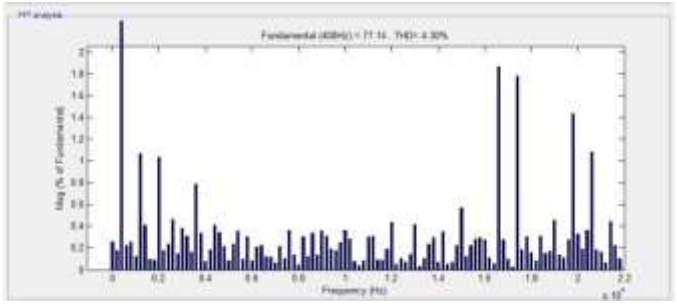


Fig -9: Harmonic Spectrum for MPD

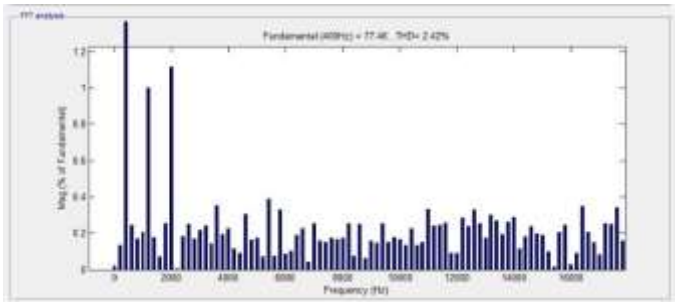


Fig -10: Harmonic Spectrum for MAPOD

TABLE III: COMPARSION OF SCMLI TOPOLOGIES WITH RESPECT TO LEVEL SHIFTED MULTICARRIER PULSE WIDTH MODULATION:

Topology	PD	POD	APOD	MPD	MAPOD
Existing topology	17.18	13.88	10.19	7.99	5.85
Modified Existing topology	16.88	12.99	9.90	5.50	3.19
Proposed topology	13.41	10.28	7.43	4.30	2.42

In Table-III, Proposed topology of SCMLI is compared to existing topologies. From this comparsion proposed topology will yield low total harmonic distortion than other existing topology.

6. CONCLUSION:

In this proposed work, it is more convenient to employ multiple DC sources as input to a single inverter than to employ several inverters in parallel with their respective individual DC input sources. The proposed topology may cut down fewer components compared to other SCMLI topologies shown in [26] and [27] and also it reduces the cost function is the major benefit for SCMLI used as input source for high frequency ac power distribution.The SCMLI inherently solves the issue of capacitor voltage balancing as each capacitor is charged to the value which is equal to one of input voltage at every cycle. The modulation technique is used for this proposed topology of switched capacitor multilevel inverter are Level-Shifted multicarrier Pulse Width Modulation. The different types of Level-Shifted Multicarrier Pulse Width Modulation techniques are analyzed and compared with respect to THD for a proposed topology of switched capacitor nine level

inverter. The simulation of switched-capacitor nine-level inverter using level-shifted multicarrier modulation techniques was done using MATLAB/Simulink software. It can be concluded from the simulation results that the Modified Alternative Phase Opposite Disposition modulation technique offer the least THD for the proposed of switched-capacitor nine-level inverter.

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