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DESIGN OF 4TH ORDER LOW PASS FILTER USING MEMRISTIVE OP-AMPS

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Abstract - *A low pass 4th order Butterworth filter with tunable cutoff frequency is introduced in this paper. The filter is realized using operational trans-conductance amplifier (OTA) using memristor compensation technique. By using memristor component in the design of telescopic opamp there is a gradual increase in the unity gain bandwidth and the overall gain. OTA, memristor modeling and filter design are realized and simulated using Cadence 45nm CMOS technology. This low pass filter's cutoff frequency is tuned to 13.76 MHz with less power consumption of 4.2 mW. The supply is 1.8V and phase margin of 49.10 degrees is achieved. The noise distortion is around 3.88 pV/√Hz. Switching speed of the designed filter is very fast and the designed opamp supports filters to have a higher tunable range and hence, it can be used for receivers in 4G and 5G.*

***Key Words*: memristor, unity gain bandwidth, Operational Trans-conductance Amplifier, analog filter.**

1. INTRODUCTION

Filters are key structure hinders in correspondence frameworks for example software characterized radios. In these frameworks, the ideal properties for the filter incorporate low power utilization, good linearity, low thermal disturbance level, faster operating speed, and a wide tuning range. To achieve the required qualities for a superior usefulness of a filter, the fourth basic circuit component 'memristor' which has been as of late developed is utilized in the plan of the simple analog filter. The utilization of the memristor as a programmable resistance allows the acknowledgment of memristor-based simple circuits with adaptable features.

The new circuit component is dissipative and has a charge dependent relative resistance called additionally memristance, a zero-crossing hysteresis loop under AC excitation, a saturation mechanism which cannot be imitated by past principal fundamental circuit elements. Memristor is an element for both analog and digital applications on account of these properties. Utilization of memristor in oscillators, programmable gain amps, controllers, programmable filters, integrators, and chaotic sources have been under assessment.

The memristor has exposed its superior properties such as nonvolatility, binary, nonlinearity, multiple memory states, and nanometer geometries. As a result, these plentiful features of memristors have been exploited in showing their applications in nonvolatile memory, cryptosystems, neural networks, filtering circuits and memristors can be widely applied in many chaotic circuits and driven-right-leg (DRL) circuits and a series of filter circuits.

In a traditional LPF circuit, many of its properties are constant and time-invariant. When we replace the resistor and capacitor with memristive elements, results will be unequable. A low pass filter which is designed in such a way that it has a capacitor placed as the negative feedback element to an inverting op-amp and a memristor placed as the input element is examined. The filter is inspired by the fact that an R-C integrator shows low-pass filter characteristic for AC signals. Due to its variable adjustable resistance, memristor provides us with a negotiable gain characteristic to the filter. Examined memristor based filter is also a nonlinear circuit since the memristor element being used is a nonlinear circuit element.

2. DESIGN OF TELESCOPIC OPAMP

The telescopic cascode op-amp, has the parameters of larger frequency capability and less power consumption than other topology. Alongside, less power consumption and minimum noise is obtained to the signal way. The design of telescopic amplifier has 4 transistors as in contrast to the 6 transistors of folded cascode design and hence, less power consumption.

2.1 Design of first stage telescopic amplifier

The telescopic differential amplifier is represented in Fig - 1, all transistors should be in the saturation region of operation in order to obtain constant performance over a higher voltage range. We consider the half circuit as it is identical in nature, to result the dc gain.

Making an assumption that all transistors work in the saturation region, we take the small signal characteristics. Constant current flow is obtained when MOSFET works in saturation region. The gain voltage is one and the same as of common source stage. The voltage gain is equal to that of common source stage because the drain current produce by input device must flow through the cascode device.

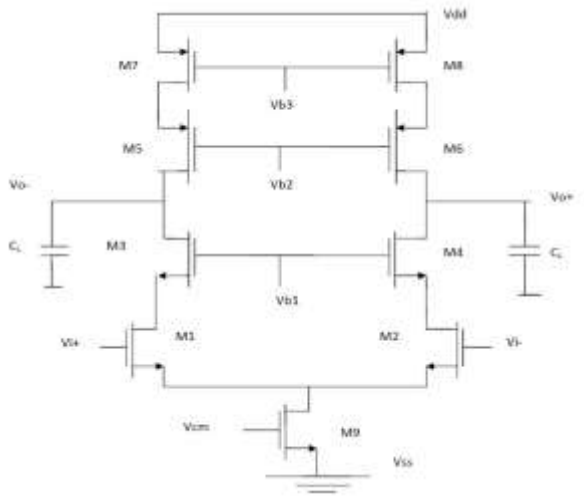

Fig -1: Telescopic differential amplifier [1]

The larger output impudence is a necessary property for the design. The output impedance (R_{out}) of the architecture as represented in Fig-2 is designed by the Equation (1).

$$R_{out} = \{(1 + (g_{m2} + g_{mb2})r_{o2})r_{o1} + r_{o2}\}//\{(1 + (g_{m3} + g_{mb3})r_{o4})r_{o3} + r_{o4}\} \quad (1)$$

Then, calculate the gain as given in the Equation (2)

$$A_v \approx -G_m \times R_{out} \text{ here, } G_m \approx g_{m1} \quad (2)$$

g_{m1} is the trans conductance of M_1 transistor.

The trans conductance g_m can be designed by the Equations (3)-(5)

$$g_m = \mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{th}) \quad (3)$$

$$g_m = \frac{2I_D}{(V_{GS} - V_{th})} \quad (4)$$

At constant V_{DS}

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \quad (5)$$

Hence, overall gain of the cascode structure is represented in the Equation (6)

$$A_v \approx g_{m1}(g_{m2}r_{o1}r_{o2})//(g_{m3}r_{o3}r_{o4}) \quad (6)$$

Apart from consuming higher voltage, it benefits by producing large differential gain. The consumed power of the op-amp is given by Equation (7)

$$P_d = V_{dd} \times I_{total} \quad (7)$$

Where I_{total} combined current through single stage amplifier. Since our requirement is to get larger gain, it is the requirement to attain the gain of 50 dB from the equations (8) and (9) the current across the transistor can be calculated.

For NMOS:

$$I_D = \frac{1}{2}\mu_n C_{OX} \frac{w}{L}(V_{GS} - V_{tn})^2 \quad (8)$$

For PMOS:

$$I_D = \frac{1}{2}\mu_n C_{OX} \frac{w}{L}(V_{GS} - V_{tp})^2 \quad (9)$$

These are the equations for transistors working in saturation region.

To attain a maximum output swing, we must choose the values for the input common mode and the bias voltages $V_{b1}$and V_{b2} as shown in the Fig - 2.

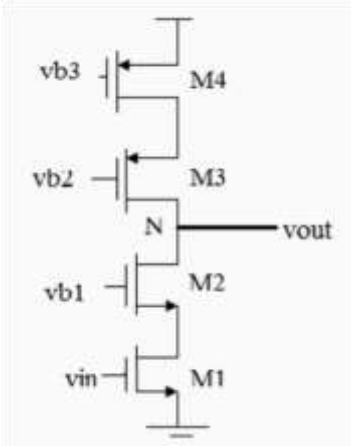

Fig -2: Half circuit of telescopic cascode [1]

Firstly, in the telescopic cascode architecture the main input differential pair transistors M_1 and M_2 are chosen for the sizing. So as to not make an effect on the bandwidth, trans conductance and the gain. We must not make the input pair values too high. M_1 and M_2 transistors act as a buffer between the input and the output pair, so after sizing the main input differential transistors, NMOS M_1 and M_2 transistors are sized. For the required amount to flow through both the legs in the architecture, PMOS load transistors are designed with the required sizing values. Care is taken such that the sizing values of the PMOS transistors do not have a huge effect on the output parasitic capacitance. The value of the tail current is chosen to be 30 µA. By substituting the same in Equation (10), we obtain

$$I_D = \frac{I_{SS}}{2} = 15\mu A \quad (10)$$

Therefore,

$$r_{o1} \approx \frac{1}{\lambda_n I_D} \approx r_{o2} \quad (11)$$

$$r_{o3} \approx \frac{1}{\lambda_n I_D} \approx r_{o4} \quad (12)$$

All transistors has to obey the condition $V_{DS}>V_{GS}-V_t$ in order to work in saturation region. Set the V_{incm}= 0.9 V and V_{tail}= 0.6 V for current source tail transistor and DC level is considered to be 0.6 V for a better response. We obtained voltage conditions by applying all condition by considering the half circuit as represented in the Fig - 2.

2.2 Common mode feedback circuit

Larger differential gain of completely differentially OTA balances out the differentially-mode signals inside OTA, yet common mode signals may skim. Additional circuit is required which is CMFB, to settle the common mode signal which is given in the Fig - 3. The A negative feedback loop which is to be compensated properly for good stability and good strength is actualized by the CMFB circuit. The architecture of the CMFB circuit is more testing when compared to the genuine operation amplifier structure because of the trouble of legitimately countering it. The differential intensifier balances out the common mode signal by CMFB

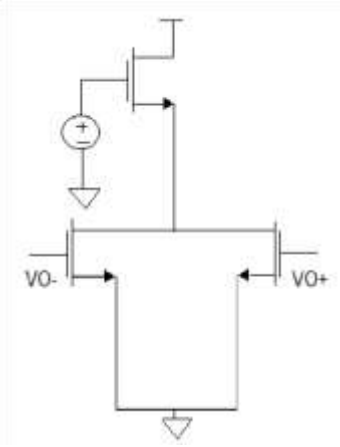

Fig -3: Common mode feedback circuit

By setting value of V_{tail}= 0.6V, transistors M_{28} and M_{27} will be in triode region. Both M_{28} and M_{27} act as two voltage dependent resistances.

$$I_1 = \mu_n C_{OX} \frac{w}{L}\{(V_{O+} - V_{DS}) - \frac{1}{2}V_{DS}\}^2 \quad (13)$$

$$I_2 = \mu_n C_{OX} \frac{w}{L}\{(V_{O-} - V_{DS}) - \frac{1}{2}V_{DS}\}^2 \quad (14)$$

$$I_{OUT} = I_1 + I_2 = \frac{1}{2}\mu_n C_{OX} \frac{w}{L}(V_B - V_{DS} - V_t)^2 \quad (15)$$

From the above equations (13)-(15), if common mode signal become positive, the will be increase vice versa if common mode signal become negative, the will be decrease. Common mode outputs for the op amp are regulated by the common mode feedback circuit.

2.3 Bias circuit

Biasing circuit is needed in operational amplifier as it work is to bias the transistor properly It offer bias voltage to the op amp in order that the transistor will operate in the specific region. For opamp, the required region is saturation. Therefore, in the telescopic op-amp, it needs bias voltages to make the transistor work in saturation region.

The common mode feedback circuit requires one bias voltage. In the initial design, ideal voltage source or current sources were used for biasing. Then, this ideal voltage source will be replace with biasing circuit which will be design later. The Table-1 shows the required bias voltage in the amplifier.

Table -1: Bias voltages

Bias Voltage	Value
Vb1/Vbtail	609.5m V
V_{b2}	1.085 V

Hence, the circuit of biasing as represented in the Fig - 4 is designed based on the require voltages. This circuit is designed by modifying the W/L fractions and check for the node voltages at cascode stage.

Fig - 5 demonstrate the circuit. V_{bias1} gives the value of 1.085V and V_{bias2} gives the value of 609.5mV.

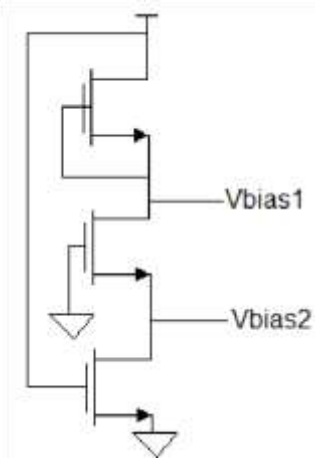

Fig -4: Bias circuit

2.4 Schematic of single stage fully differential op-amp

The common mode feedback circuit and the bias circuit need to be connected to the telescopic op-amp. Therefore, the complete schematic of the fully differential telescopic op amp with biasing circuit and CMFB is shown in Fig - 5.

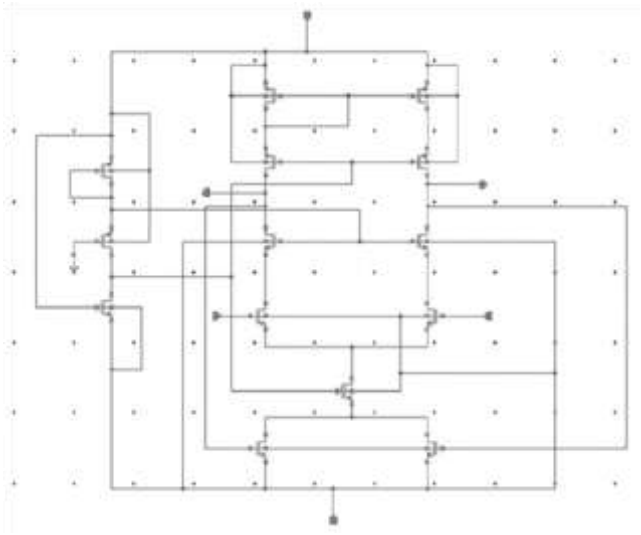

Fig -5: Complete schematic of single stage fully differential telescopic opamp.

3. MODELLING OF MEMRISTOR

After optimizing the parameters in MATLAB, a Verilog-A code for the various memristor models is written. VTEAM model was selected for the realization of the memory architecture for the reasons stated above. Then a symbol in Cadence Virtuoso is created for the memristor from the Verilog-A code. Fig-6 shows the Memristor symbol in the Virtuoso. It has 3 pins namely 'p', 'n' and 'w' position. Out of which 'p' and 'n' are used to apply the voltage.

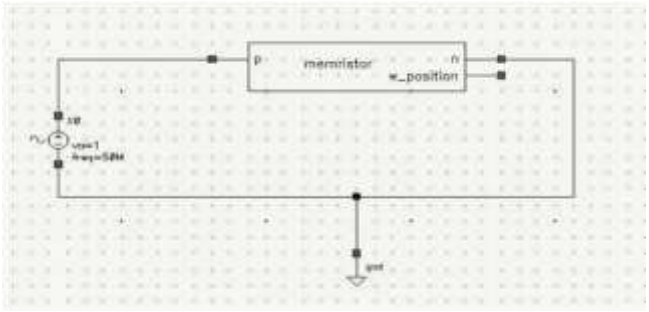

Fig -6: Memristor Symbol created in Cadence using Verilog-A Code

The memristor model is analyzed by plotting its hysteresis loop where current is along y axis and voltage along x axis. The parameters are set as optimized by the MATLAB. Fig - 6 shows memristor symbol and Fig - 7 shows hysteresis loop is plotted.

As seen from the below figure, there are two cutoff voltages V_{on} and V_{off}. For the memristor model shown V_{on}=3.5V and V_{off}=-2.5V. So for the voltages greater than 3.5V, the memristor will change R_{off} to R_{on}. For voltage less than -2.5, memristor will change from R_{on} to R_{off} and for the voltage between V_{on} and V_{off}, the memristor state won't change. So, if previously it was R_{on}, then it will remain R_{on}, if previously R_{off}, then it will remain R_{off}.

By plotting the I-V characteristics of all these above mentioned mathematical model following points are observed:

1. Symmetry in the hysteresis loop i.e. the I-V characteristic is not dependent on polarity of the applied voltage.
2. Values of R_{on} and R_{off} approaches the ideal values.
3. Voltage controlled unlike other models

So it can be concluded that VTEAM model is the best suitable model.

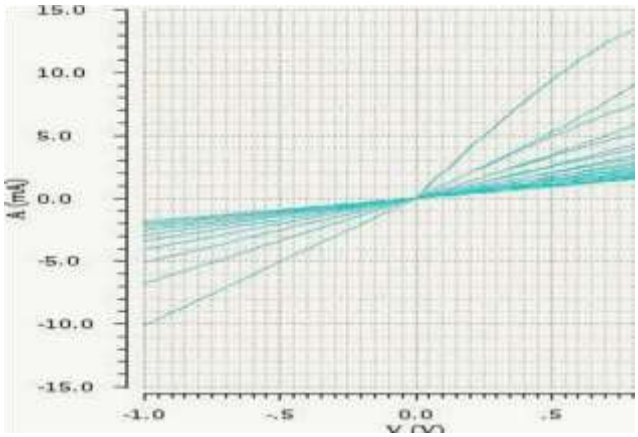

Fig -7: I-V Characteristics (Hysteresis) of Memristor.

4. DESIGN OF MEMRISTIVE OPAMP

The ultra-low power two stage Op-Amp is created by using memristor-based compensation technique. This Op-Amp has a NMOS differential pair cascaded with a PMOS differential pair and then given to PMOS common source amplifier. Also to create a tail current of cascaded stage a current mirror is used. For compensating stage, a memristor programmer with a use of memristor with one capacitor are used as appeared in the Fig - 8. The idea is utilizing the non-volatile conduct of memristor to negate the right plane zero in Miller procedure.

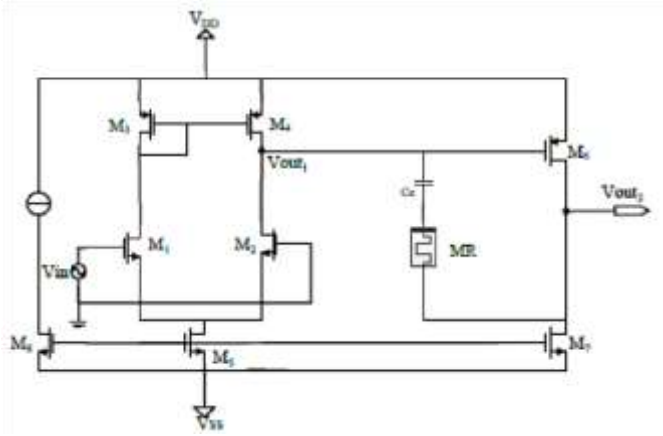

Fig -8: Circuit design of Memristive opamp

The memristor can be controlled by desired resistance with the programmer circuit to send the right plane zero to infinity. As the capacitor and memristor are in series, DC flows can't go through memristor amid Op-Amp activity stage. Additionally, taking into consideration that values for current in first and second stages of the op-amp are insufficient in order to make any change in memristor. This makes the memristance resist change and stays constant for compensation .The Equation (16) gives the transfer function.

$$H(s) = \frac{a(1-s\left(\frac{C_c}{gm_{II}}\right)-MRC_c)}{1+bs+cs^2+ds^3} \quad (16)$$

Where, $a = gm_I gm_{II} R_I R_{II}$

$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + gm_{II}R_I R_{II}C_c$

$c = R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II}) + MRC_c(R_I C_I + R_{II}C_{II})$

$d = R_I R_{II} MRC_I C_{II} C_c$

Here gm_{II}, R_{II} and C_{II} are the calculated trans-conductance, resistance and capacitance of stage II of the Op-Amp. Also gm_I, R_I and C_I gives trans-conductance, resistance and capacitance of stage I of Op-Amp circuit. The C_C is the capacitance of the compensation capacitor. Here in this circuit gm_I and gm_{II} are equal to the trans-conductance of M_1 transistor (gm_1) and M_6 transistor (gm_6) respectively. Based on Eqn. (1) and with the assumption that $C_{II} > C_C > C_I$ the first, second and third pole can be determined through Equations (17)-(19)

$$P_1 = \frac{-1}{gm_{II}R_I R_{II}C_c} \quad (17)$$

$$P_2 = \frac{-gm_{II}}{C_{II}} \quad (18)$$

$$P_3 = \frac{1}{MRC_I} \quad (19)$$

The +ve zero of the circuit proposed is obtained from Equation (20),

$$Z_1 = \frac{1}{C_c\left(\left(\frac{1}{gm_{II}}-M_{MR}\right)\right)} \quad (20)$$

where M_{MR} is the memristance. The 3rd pole is a larger frequency pole and it doesn't affect much on transfer function. From Eqn. (20) it can be seen the memristor can compensate the 1st zero of the circuit. Programming the memristance to $1/gm_2$ leads first zero to infinity. The Op-Amp circuit's unity-gain bandwidth with memristor-based compensation block is determined by the Equation (21)

$$UGB = \frac{gm_I}{2\pi C_c} \quad (21)$$

Considering all the factors and parameters mentioned above a memristive telescopic op-amp is designed as shown in the Fig - 9.

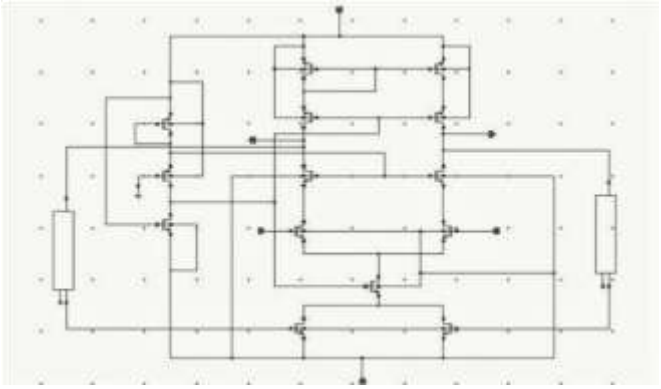

Fig -9: Memristive opamp circuit

5. DESIGN OF 4TH ORDER LOW PASS FILTER

A Using a memristive Op-amp as the basic part a low pass filter is designed. The circuit of the filter is given in the figure 4.1.The single biquad cell's transfer function is given in Equation (22)

$$H(S) \cong -\frac{R_3}{R_1}.\frac{1}{1+sC_2\left(R_2+R_3+R_2\frac{R_3}{R_1}\right)+s^2C_1C_2R_2R_3} \quad (22)$$

And in order to determinate the reliable transfer function, the design equations are given by the Equations (22)-(25)

$$G = \frac{R_3}{R_1} \quad (23)$$

$$\omega_0{}^2 = \frac{1}{C_1C_2R_2R_3} \quad (24)$$

$$Q = \frac{1}{\omega_0}.\frac{1}{C_2\left(R_2+R_3+R_2\frac{R_3}{R_1}\right)} \quad (25)$$

Op-amps with infinite gain and UGBW obeys these expressions, but these can be considered if UGBW>10*$f_0$and DC gain>45dB are still a good approximation given the proposed OPAMP specifications of UGBW>10*f_0 (f_0 = filter cut-off frequency) and DC Gain >45dB.alsoThe extra transistors MB also contribute noise. These additional transistors introduce two new noise sources to the Rauch

cell. The net noise is given by the equation 26 as Input Referred Noise (IRN).

$$IRN^2 \cong 8k_BTR_1G^2 + 8k_BTR_2(1+\frac{1}{G})^2 + 8k_BTR_2(\frac{1}{G})^2 + IRN_{op}{}^2(1+\frac{1}{G})^2 + \frac{16}{3}k_BTg_m(\frac{R_1R_3+R_2R_3}{R_1})^2(\frac{1}{G})^2 \quad (26)$$

Quality factor sensitivity can be affected by limited output resistance of transistors. This can be completely nullified by connecting them to Opamp virtual ground. There will always be a selection criteria between noise and output resistance.

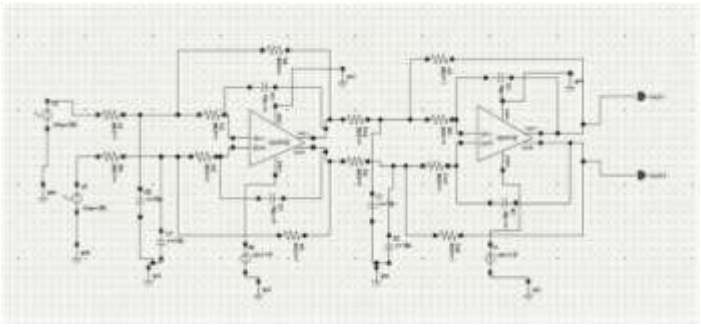

Fig -10: Filter using memristive opamps

The values which are obtained for the given specification of the low pass filter with the cut-off of 13.76 MHz are 270 ohms and 20 pF of resistance and capacitance, respectively.

6. SIMULATION AND RESULTS

All the proposed circuit designs are simulated in Cadence Virtuoso and the results are analyzed.

From Table -2, it can be seen that the required high unity gain bandwidth is achieved when compared to the conventional folded cascode op-amp.

Table -2: Telescopic opamp results

Specification	Obtained
DC gain	46 dB
Phase margin	49.316 degree
Unity gain frequency	654.64MHz
Slew rate	1.3 V/µs
CMRR	73 dB
Power consumption	190.185 µW

The memristive op-amp architecture based on telescopic op-amp which is explained in chapter 3 has been is used for filter design. Here the memristor at the output acts as dominant pole resulting in higher unity gain bandwidth .The simulation results using gpdk 45nm CMOS process was implemented for a gain of 50dB and unity gain bandwidth of 4.66 GHz. The results are summarised in the Table - 3.

Table -3

Specification	Achieved
DC gain	50 dB
Phase Margin	37.02 degree
Unity Gain Bandwidth	4.66 GHz
Slew rate	1.5 V/µs
CMRR	80 dB
Power consumption	93.114 µW

: Memristive opamp results

The current section compare the results of designed op-amps with selecting the better op-amp results. The comparison of results has been shown in the Table - 4.

Table -4: Comparison of results

Specification	Telescopic Op-amp	Memristive Op-amp
DC gain	46 dB	50 dB
Phase Margin	49.316 deg	37.02 deg
UGB	654.64 MHz	4.66 GHz
Slew rate	1.3 V/µs	1.5 V/µs
CMRR	73 dB	80 dB
Power consumption	190.185 µW	93.114 µW

From the Table – 4 Memristive Op-amp is selected for the construction of low pass filter due to its high UGB. As it is seen that the UGB of memristive op-amp is 4.66GHz compared to that of Telescopic which is 654.64MHz. Power consumption is less in memristive op-amp as compared to the Telescopic op-amp.

The simulation results using gpdk 45nm CMOS process for the filter was implemented for a cut-off frequency of 13.76 MHz. The power consumption of the filter has been reduced due to using Memristive Op-amp which has lower power consumption. Hence the filter power consumption is 7.51uW.

Required parameters for the filter are calculated and are compared with the target values as shown in the Table - 5.

Table -5: Filter results

Specification	Target	Achieved
Gain	0 dB	3.71 dB

Cut off frequency	11 MHz	13.76 MHz
Noise	18 nV/√Hz	3.88pV/√Hz
Phase Margin	-	49.10 deg
Power Consumption	14 mW	7.51 uW
Pass Band	-	0-10MHz
Stop Band	-	938 MHz- ∞
Power supply	1.8 V	1.8 V

7. CONCLUSIONS

The telescopic opamp which has better unity gain bandwidth (USB) its gain is compared to folded cascode Op-amp. Studying various memristor models, programmable memristor is designed. In order to increase the UGB of telescopic op-amp memristive compensation has been studied. This compensation technique is coupled with the designed telescopic op-amp leading to the increase in UGB to 4.66GHz and gain to 50dB and slew-rate to 1.5 V/μs.

A self-bias circuit is designed for every Op-amp in order to reduce the power consumed by the circuit. A low pass filter is designed using the memristive op-amp. The biquadratic Rauch cell filter design is learned and is used to design a 4th order low pass filter. The filter is designed with a cut-off frequency of 13.76MHz. The noise is reduced to 3.88 pV/√Hz and power consumption to 7.51uW.

A wide tunable range of 466MHz is achieved and a low pass filter with 13.76 MHz as cut-off is designed for WLAN receivers.

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