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Design of Low Power PLL using Sleepy Inverter Five Stage Current Starved VCO

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Abstract - ***This paper presents the design of low power, low voltage Phase Locked Loop system. A Phase Locked Loop is a closed-loop system that causes one system to track with another. The main source which makes PLL low is the VCO. In this paper a PLL is designed using sleepy Inverter Current Starved VCO which consumes less power and less Voltage. All the simulation work has been done using Tanner Tool at 180nm CMOS technology.***

Key Words: *Low Power, Sleepy Inverter, Current Starved VCO, PLL.*

1. INTRODUCTION

The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant [1]. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. A PLL is essentially a negative feedback loop that locks the on-chip clock phase. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices. PLL simply consists of a phase detector (PD), charge pump (CP), voltage controlled oscillator (VCO), and frequency divider in a feedback loop. The PD compares the phases of output voltage and input voltage, generating an error signal that varies the VCO frequency until the phases are aligned, that is the loop is locked. The output of the VCO is synchronized with the input signal, by the negative feedback loop. Phase-locked loops are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices.

2. BASIC BLOCKS OF PLL

Phase-locked loop mechanisms may be implemented as either analog or digital circuits. Both implementations use the same basic structure. The basic block diagram of the PLL is shown in the Fig.1.

In general a PLL consists of four main blocks:

a) Phase Frequency Detector (PFD)
b) Charge Pump (CP/LPF)
c) Voltage Controlled Oscillator (VCO)
d) Frequency Divider (1/N)

It is basically a feedback control system that controls the phase of a voltage controlled oscillator (VCO). The "Phase frequency Detector" (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. In Fig. 1 [1], input signal is applied to one input of a phase detector. The other input is connected to the output of a frequency divider. Normally the frequencies of both signals will be nearly the same. Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN". The "Charge Pump" (CP) circuit is used in the PLL to combine both the outputs of the PFD and give a single output. The output of the CP circuit is to generate a DC control voltage and this voltage signal controls the VCO.

The output of the VCO is at a frequency that is N times the input supplied to the frequency reference input. The phase and frequency of the "Voltage Controlled Oscillator" (VCO) output depends upon the generated DC control voltage. The output of the VCO is synchronized with the input signal, by the negative feedback loop.

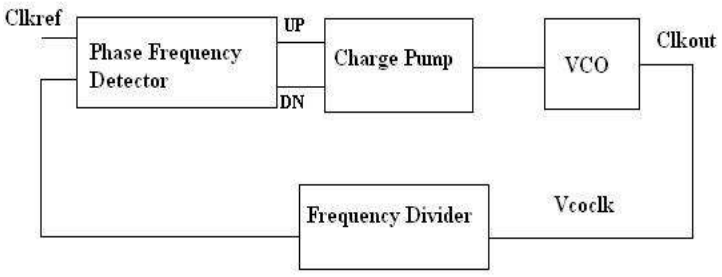

Fig -1: Phase Locked Loop System

1.1 Phase Frequency Detector

Phase frequency detector is one of the important part in PLL circuits. PFD (Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal [2]. PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signals. Fig. 2 shows a PFD with its inputs and outputs and Fig. 3 [3] shows the schematic circuit of PFD. The output signals of the PFD are fed to the charge pump. The output voltage of the charge pump controls the output frequency of the VCO, so with a change happens at the input of the CP the output voltage will change which will change the output frequency of the VCO. In this case the sensitivity of the phase and frequency difference detection of the PFD is very crucial. Sensitivity of the PFD means the smallest difference the PFD can detect and produce UP or DOWN signals that will affect the charge pump [3].

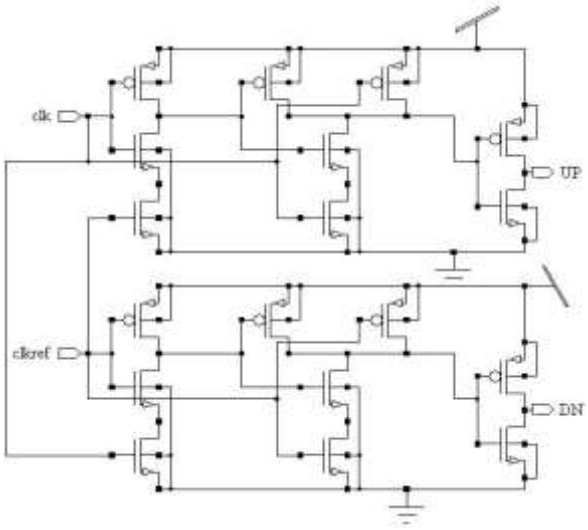

Fig -2: Phase Frequency Detector

1.2 Charge Pump

Charge pump is the next block to the phase frequency detector. The output signals - UP signal and DOWN signal generated by the PFD is directly connected to the charge pump. The main purpose of a charge pump is to convert the logic states of the phase frequency detector into analog signals suitable to control the voltage-controlled oscillator (VCO). Basically, the charge pump consists of current sources and switches. The output of the charge pump is connected to a low pass filter that integrates the charge pump output current to an equivalent VCO control voltage (V_{CNTL}). Fig. 3[4] shows the conventional circuit of the charge pump. It consist basic three stages as:

State 1: Charging current: $+I_{CP}$
State 2: Discharging current: $-I_{CP}$
State 3: Zero current

The PFD needs to produce a certain amount of pulse width of the UP and DN signal in the beginning of the period. In this condition, ideal charge pump will give zero current which is state 3 since the charging current is equal to the discharging current. When the VCO output frequency is leading the reference frequency, the PFD will activate the DOWN signal and deactivate the UP signal. Hence, switch S1 will be opened and switch S_2 will be closed. This time, current I_{CP} will flow out and reduce the V_{CNTL}. Consequently, the VCO output frequency is decreases. The lock condition of the PLL is established when the VCO output frequency is the same as the reference-frequency. During this period, the PFD will deactivate both up and down signals. Hence switches S_1 and S_2 will be opened until the VCO output frequency changes. Since switches are open, there is no current path formation, hence no current will flow into or out. Fig. 3 [5] shows schematic of charge pump.

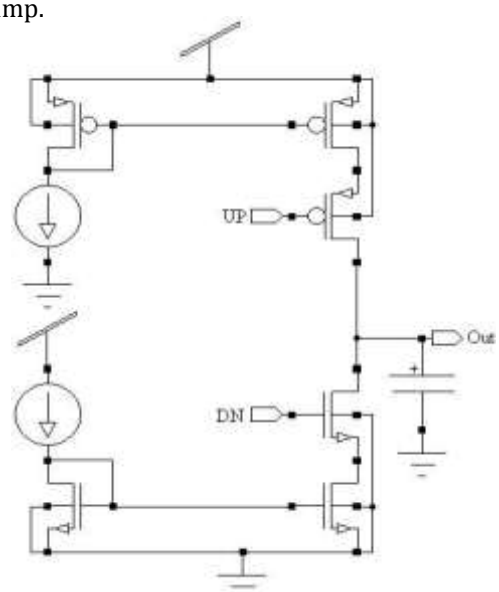

Fig -3: Charge Pump

1.3 Proposed Current Starved VCO

A voltage controlled oscillator or as more commonly known, a VCO, is an oscillator where the control voltage controls the oscillator output frequency. The VCO's output is an AC waveform whose frequency is dependent upon the input voltage. Voltage-controlled oscillator or VCO is an electronic circuit that uses amplification, feedback, and a resonant circuit to generate a repeating voltage waveform. The most popular type of the VCO circuit is the current starved voltage controlled oscillator. In this circuit the number of inverter stages is fixed. The simple way to control the charge and discharge time of an inverter is to control the current through the inverter, via a voltage controlled current source, Vcrtl, as depicted in Fig. 4[6]. This current source is driven by the control voltage and the current will determine the charge up and discharge

time of the inverter. This topology is called current-starved inverter, as the regular inverter is short of the current they are normally allowed to consume. With correct sizing and current levels, an odd number of stages of these current starved inverters can make a decent VCO. This design is simple and the oscillation frequency can achieve reasonably fast and due to the square law change in current levels in the footer device. We can size the footer device wider so that it doesn't affect the output swing much [7]. The operation of current starved VCO is similar to the ring oscillator. Fig. 5 [8] shows five stage Current Starved VCO.

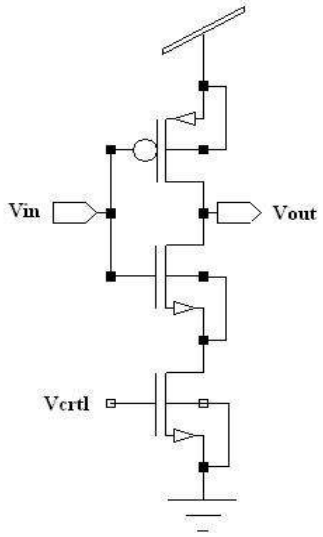

Fig -4: Basic Current Starved VCO

Each delay cell consists of one pMOS and nMOS which operate as inverter, while upper pMOS and lower nMOS operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first nMOS and pMOS are mirrored in each inverter current source stage. pMOS and nMOS drain currents are the same and are set by the input control voltage. There are different types of voltage controlled oscillators used in PLL, one is Current starved VCO.

Traditionally sub threshold leakage current is reduced by introducing nMOS sleep transistor in the pull down path and pMOS sleep transistor in the pull up path of a CMOS circuit. In sleep transistor technique, an nMOS sleep transistor is connected in the pull down path and pMOS transistor is connected in the pull-up path shown in Fig. 5[9]. Consider sleepy inverter operation. During normal operation the sleep signal slp is held at logic 1 voltage level and complementary sleep signal slpb is held at logic 0 voltage level. The circuit comprising of transistors M2 and M3 functions as a traditional inverter. During normal operation the transistors M1 and M4 are also on and hence the node VG is at ground potential and node VP is at V_{DD}. Thus the inverter produces inverted output. When inverter has to function in stand-by or sleep mode the signal slp is held at logic 0 and signal slpb is held at logic 1.

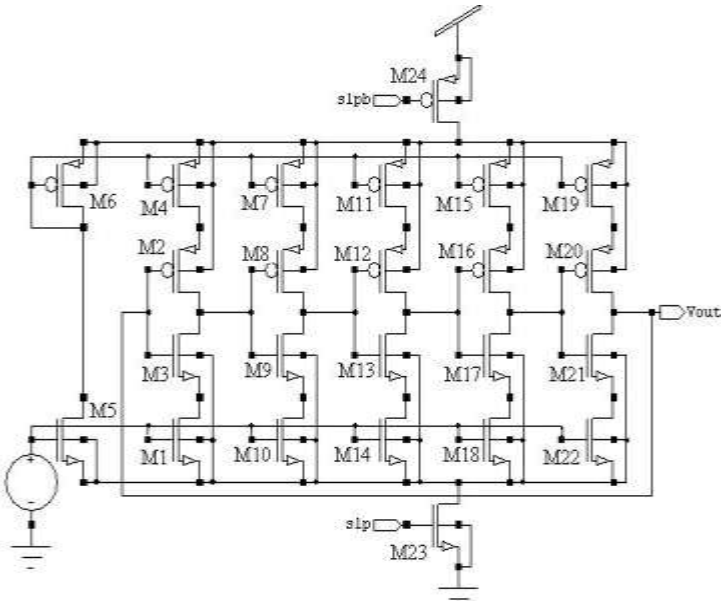

Fig -5: Proposed Current Starved VCO

This makes the two transistors M1 and M4 to enter into cut-off state. Thus the node VG is at a virtual ground potential and node VP is at a virtual power potential. Thus the inverter enters in to sleep mode. Due to the cut off transistors M1 and M4 the potential VG increases; the potential VP drops. The source to body potential of transistor M3 increases and causes threshold voltage of transistor M3 to rise. Thus sub threshold current of transistor M3 reduces [10]. Fig. 6 shows the layout diagram and Fig. 7 shows the output waveform of proposed CS VCO using sleepy inverter and graph defines the relation of power at different bias voltage.

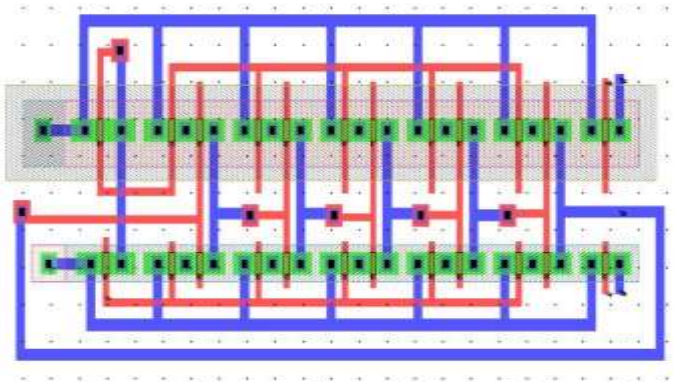

Fig -6: Layout Diagram of Proposed Current Starved VCO

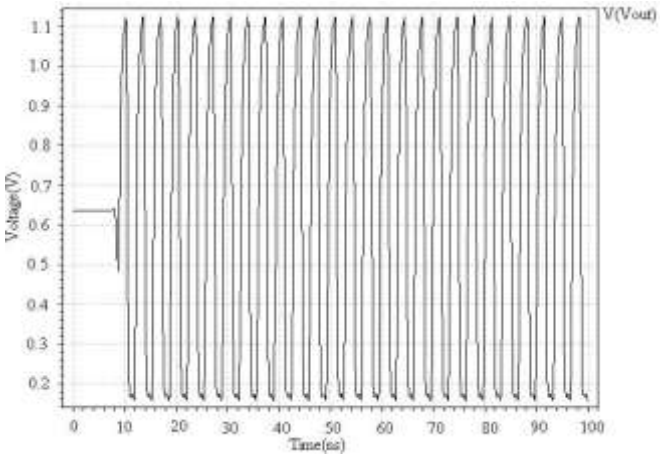

Fig -7: Output Waveform of Proposed CS VCO

1.3 Frequency Divider

The output of the VCO has to be divided before it is fed back to the input of the PLL. A basic frequency divider circuit as shown in Fig. 8, which receives a clock signal of a predetermined frequency and is structured to divide the reference clock signal by N and provide an output pulse signal for every N cycles of reference clock signal [11].

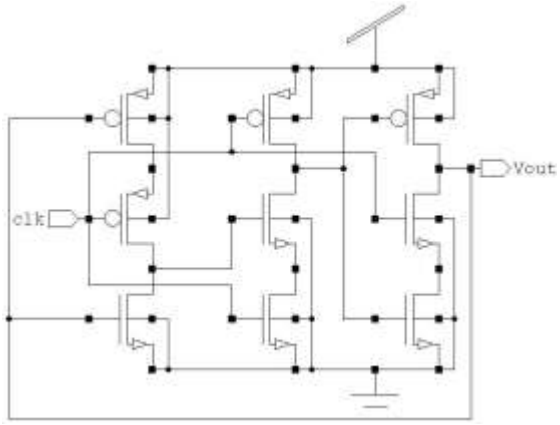

Fig -8: Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. On the other side, such a frequency divider has the advantage of low power consumption. Fig. 8 [11] shows the schematic diagram of frequency divider circuit.The first two inverters operate as dynamic latches controlled by CLK, and the third inverter provides the overall inversion required in the negative feedback loop.

3. SIMULATION RESULTS

Fig. 9 depicts the schematic diagram of proposed phase locked loop system with current starved voltage controlled oscillator using sleepy inverter [12]. Extremely low power consumption is achieved when using sleepy inverter VCO in the PLL system while using simple current starved voltage controlled oscillator. Proposed PLL as shown in Fig. 9 consume power of about 0.065mW.

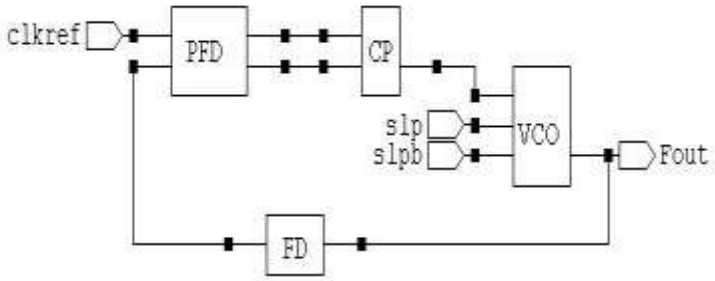

Fig -9: Proposed PLL

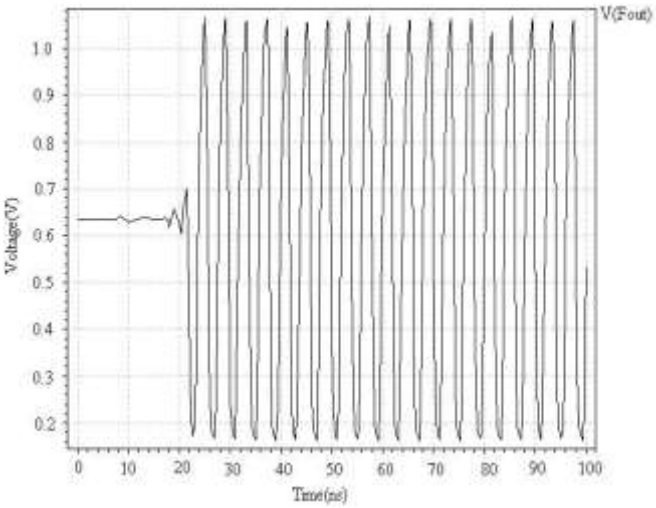

Fig -10: Output Waveform of Proposed PLL

4. CONCLUSION

The main focus of this paper is to design of low power low Voltage CMOS PLL. The main source which makes PLL low is the VCO. The other blocks, such as Phase Frequency Detector, Charge-Pump and Frequency Divider contribute to making low power Phase Locked Loop system. Understanding the techniques of low power in VCO and other PLL blocks are also discussed with their simulation work to design low power PLLs. In this paper, the low power techniques of VCOs using current starved voltage controlled oscillator were deeply studied and analyzed. Current Starved VCO using Sleepy Inverter turned out to be the best for the low power PLL system because after simulation and calculated power, it is observed that it

consumes less power as compare with the conventional circuit. Proposed PLL using Sleepy Inverter is simulated at 180nm CMOS technology.

Table -1: Calculated Parameters

Performance Parameters	Proposed Parameters
Supply Voltage (VDD)	1.5v
Power Consumption	0.065mW
Maximum Power	0.2mW
Minimum Power	1.14µW
Temperature	25ºC
Technology	0.18µm

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BIOGRAPHIES

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