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Signal Integrity Analysis of High Speed Interconnects in SATA Connector

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Abstract - *In this upcoming high speed digital interconnecting world, the differential signaling has become a wide sense choice. When more than two differential pairs run in parallel coupling occurs which is the case in conventional differential lines in PCB? To surmount this problem, we put forth the idea of Twisted Differential Line (TDL) structure on a multilayer high speed PCB. It reduces both near end crosstalk and far end crosstalk approximately 30dB.*

Key Words: Twisted Differential Line, Differential signalling, crosstalk, Radiated emission

1. INTRODUCTION

SATA interconnect, a high speed connector, is widely employed for faster data rate and is potentially cost efficient. In this SATA replaces PATA by transmitting data twice as fast as the other. SATA delivers a point-to-point signalling and provides a consistent platform for the ongoing development of direct attached and network storage applications [4]. It lays a road map for scalable performance and system design improvement that will benefit end users and system vendors. Poor design, configuration, cable/connector quality can lead to "device not found" failures, poor performance like training to a lower speed or throughout degradation, non-interoperability with certain SATA end points, EMI causes a wireless device, such as a mouse, to work intermittently.

Generally there are several aspects in crosstalk reduction of high speed data rate interconnects system in enhancing the performance at transmission. These include filter and balancing capacitor for crosstalk reduction [1]. In the SATA interconnect system, there are two pairs of differential traces are connected to the sata pins, in the four trace two differential for write and other two trace for read application in the SATA connector. In this paper, the problem focusing on crosstalk reduction in the SATA interconnect traces configuration for maintaining good signal quality throughout high density and high speed interconnects at multi-gigabit data rates. The problem investigates with the conventional traces and the SATA connector pins are analyzed in return and insertion loss parameters [3].

Its goal is to provide "Margin Headroom" such that SATA based systems perform optimally even in the presence of adverse conditions. Hardware designers improve their design by paying careful attention to equalization tuning and hardware design. In this paper SATA connector is analyzed using EMpro and its characterized by S Parameters. In this paper we propose a twisted differential line trace for a specific application is designed the signal integrity is improved for high speed interconnections in PCB at a frequency of 5GHz

2. SIGNAL INTEGRITY ANALYSIS IN SATA CONNECTOR

Signal integrity (SI) rates the quality of the signal. It addresses two aspects say space integrity and time integrity. Space integrity also known as signal amplitude integrity, which predicts the signal quality, should meet the minimum input peak level and maximum input low level. Time integrity which indicates the signal timing, should satisfy lower establish able and maintainable time.

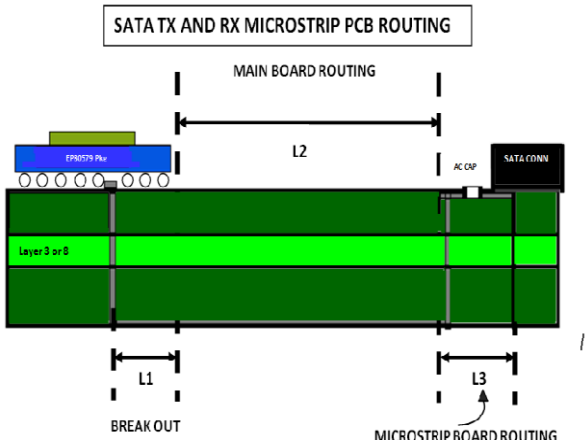

Fig -1: SATA Transmitter and Receiver Microstrip routing with mother board

SI ensures the signals to reach their destination in good condition. Also application of SI finds solutions for the following critics such as Crosstalk: Unnecessary coupling which may be capacitive or inductive. Secondly, Power distribution: It directly influences the high speed system performance and reliability. It should offer reduced noise power in PCB including Vcc and ground. Finally, Reflection, Overshoot, Ringing: Undesired characteristics such as Isochronous Switching Noise, impedance mismatch, discontinuous interconnection [1].

Traces between circuit board components are more than just copper. These interconnects have an inherent delay that, depending on the signal's edge rate, can cause signal integrity problems, such as crosstalk electromagnetic emission. The fast edge rates of today's smaller silicon nodes make virtually every PCB trace like a transmission line each with a potential for SI issues [2].

With a rapid evolution of high speed interconnect technology, the size of cables becomes smaller and smaller and the I/O amount becomes more, corresponding to the package type of pins in the cable. As a result, the crosstalk and radiation are reduced with the advancement of traces in the cable, in the figure 1 shows the SATA connector and TX and RX microstripline interconnect traces connected to motherboard configuration.

3. RESULTS AND DISCUSSION

A 3D model of the SATA connector shown in figure 2, and its pins are validated using EMpro simulation in the frequency range of 5 GHz [3]. SATA connector pin details are shown in figure 3, in this four pins are employed as two pair of differential signals. Among them, two pins (port1 and port2) are used to receive and the other two pins (port3 and port4) are used to transmit the signals. The left out three pins are ground pins. The SATA connector discussed and analyzed using 3D electromagnetic software

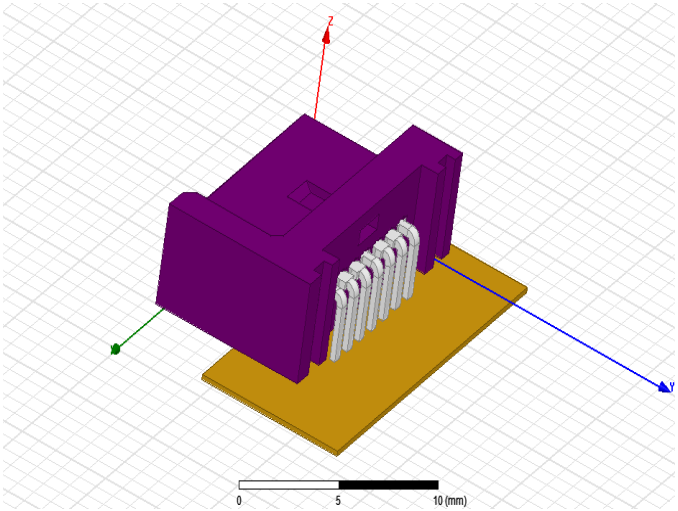

Fig -2: Simulated 3D model of SATA connector

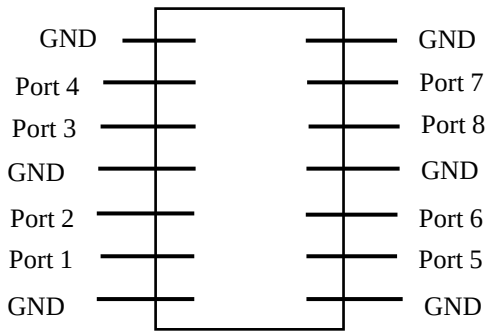

Fig -3: Pin diagram of SATA Connector

In the SATA connector the insertion loss is represented as S21 in S-parameter while the return loss is denoted by S11 which is the reflection co-efficient and the near end coupling is given as S31. In the figure 4 shows that the return loss for all SATA connector pins are analyzed figure 5 shows that insertion loss of sata connector while the near field coupling of all connector pins are shown in figure 6.

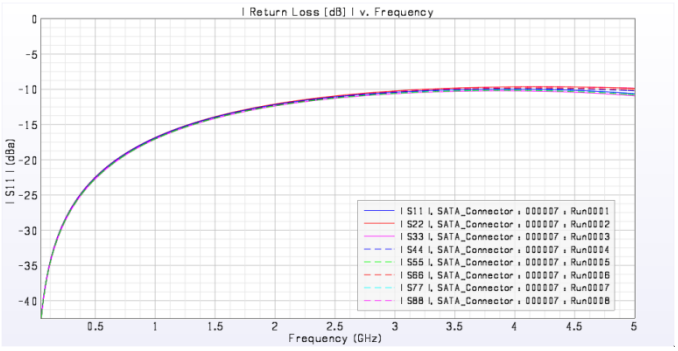

Fig -4: Return loss of SATA connector Pins

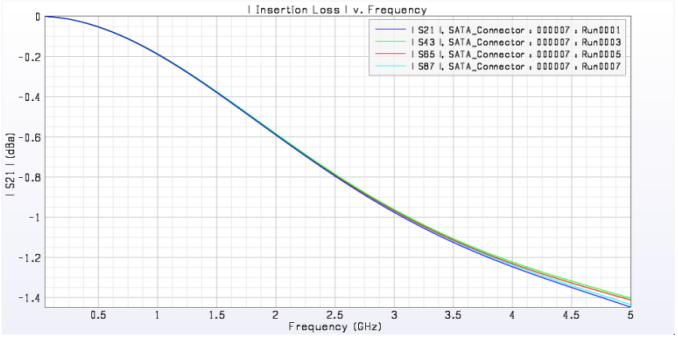

Fig -5: Insertion loss of SATA connector Pins

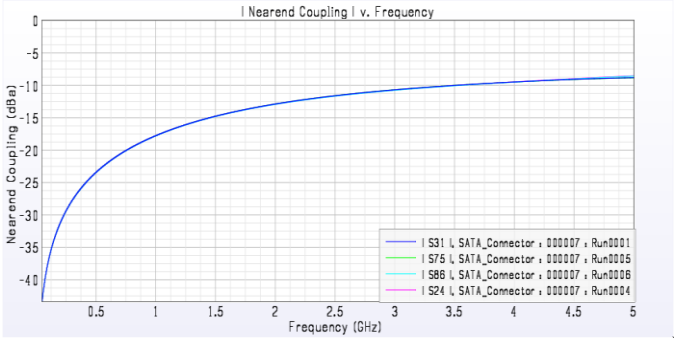

Fig -6: Near end coupling of the Differential pair pins of SATA connector.

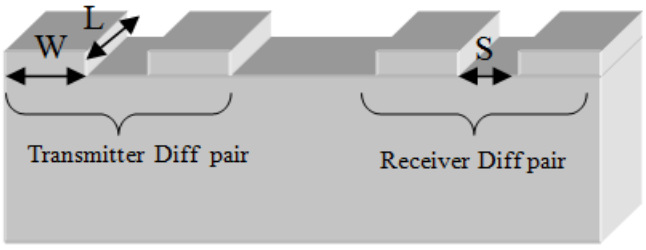

Fig -7: Differential trace connected with SATA connector

The geometry under study is shown in figure7, its two layer differential trace configuration, in the interconnect traces the two pair of differential pair traces are shown the dimension of the trace are the width of the trace is 4.75 mils the length of the traces are 1500 mils and edge to edge gap of the trace are 5.25 mils. The differential traces are used to connect the SATA connector to the computer peripheral for high speed data transmission in the gigabit range. The conventional differential trace and proposed twisted trace are analysed and its characterized by near and far end crosstalk.

Figure 8 represents the near end and far end crosstalk of conventional trace configuration. In conventional tracing, the traces run in parallel which causes crosstalk and thus is crucial for good performance in the desired frequency band, in the figure 8 the near and far end crosstalk was analyzed.

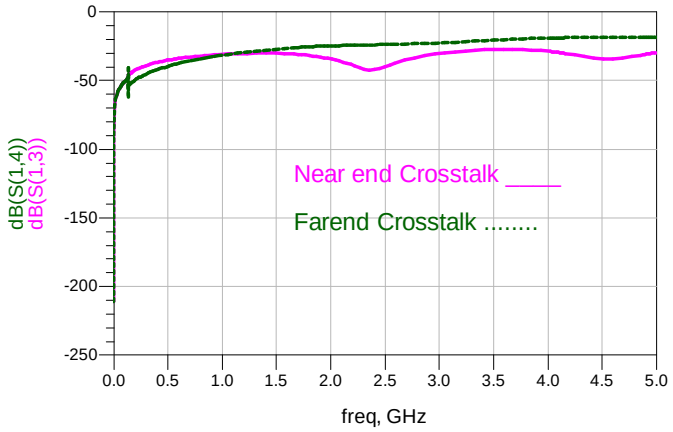

Fig -8: Near end and Far end crosstalk of conventional trace configuration.

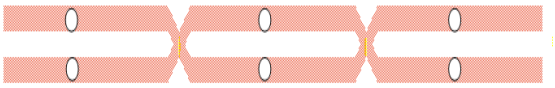

Fig -9: Noval Twisted pair differential for SATA connector

The figure 4 delivers the main board routing, which has been changed in the design suggested below. The proposed design is the Twisted Differential Line (TDL) structure in which twisted pair concept is implemented in the multilayer PCB. It uses a two segmented conducted traces on both the layers of PCB in a crisscross pattern with several vias. When more than two differential lines run in parallel as shown in figure, a line is mainly coupled to the other line because all the lines are parallel. In order to avoid this coupling the twisted differential line was introduced in the SATA high speed connector interconnects, the twisted differential line has more advantage major one is physical configuration that configuration is reduce the loop area. The differential trace width, spacing and routing are properly characterized. Impedance mismatch is analyzed as a major factor for signal integrity. In order to minimize its effect, the connector contact geometry is designed to maintain the impedance profile constant. A multilayer data transfer RF board with differential traces which connects to a chip is then designed and simulated using EM MoM solver. At the end, the signal integrity is analyzed to validate the crosstalk and quality. The twisted differential line also increases the spacing between the neighboring differential pairs in an efficient way and thus reduces the average mutual inductance and capacitance. In addition to that it provides an offset TDL, which is a quarter of a period offset scheme, affords a balanced operation in each differential pair resulting in the reduction of cross talk in differential pairs.

Figure 10 depicts the result of near death and far end crosstalk in the proposed differential pair configuration.

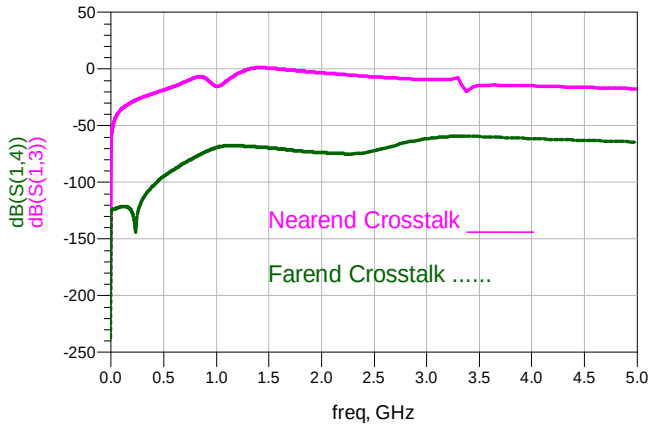

Fig -10: Near end and Far end crosstalk of proposed trace configuration.

In the intended configuration, physical parameter such as length, width and spacing are altered . Also several vias are employed in order to minimize crosstalk. When compared to the conventional model, the resulted crosstalk is found to be scaled down.

3. CONCLUSION

As the required data rate has been continuously increasing, the crosstalk and the differential signaling are the major drawbacks. Hereby, the concept of a twisted pair in cable interconnections in terms of Twisted Differential Line(TDL) on high speed PCB is proposed. The proposed configuration delivers a solution for high speed interconnection designs, despite the increased cost. TDL can support data transmission at a very high rate without a ground reference plane. It retains the transmission bandwidth, in addition reduce the crosstalk more than 30dB.

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