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Switch Level Implementation of a 4-Bit Logical Unit using Mixed Logic Design Method

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Abstract – *This paper introduces a logical unit by means of low power gates which is executed by switch level modeling. The ALU entails of a logical unit and arithmetic unit. The logical unit performs operations such as decision making etc. The low power structure of the two-to-four decoder is modified and prolonged to form four bit logical unit to implement AND,OR,XOR,XNOR operations. Finally the simulations are carried out by switch level modeling. The layout of the logical unit was acquired by Microwind 2 design layout software.*

***Key Words*: ALU, Mixed-logic, switch level modeling, Low power gates, transmission gates**

1. INTRODUCTION

An ALU is the figuring and basic leadership hardware of any chip or microcontroller. ALUs of different piece widths are frequently required in extensive scale incorporated circuits (VLSI) from processors to application explicit coordinated circuits (ASICs). ALU is getting littler and progressively complex these days to empower the advancement of an increasingly prevailing however littler PC. The ALU consists of arithmetic and logical unit. The logical unit accomplishes various operations which are used for decision making, error detection, error correction, generating combinational functions. The 74181 is a distinctive four-bit ALU, commercially reachable as an integrated circuit chip. This IC is built using TTL technology. It performs arithmetic operations, bit manipulations, and logical operations. Few of its logical operations are the four bit AND, OR, XOR, and XNOR.

Pass transistor was mostly settled in 1990s and few plan styles were explained [3-6].A logical unit can be implemented using a variety of technologies. Different methodologies are utilized for the logical unit implementation such as reversible gates, for example GDI-approach; pass transistor logic etc. D. Balobas and N. Konofaos in [1] present a new technique for the line decoders. They consolidated transmission gates, dual value logic and static CMOS and obtain four new designs and comparison has been done. For then simulation process all the circuits designed were simulated at 3 diverse operational frequencies and 3 distinctive supply voltages with various temperatures. The comparison results demonstrates that there is 7.4%, 6.5% and 6.0% lower power, 4.5%, 9.3% and 2.3% lower delay and 11.1%, 15.3% and 7.9% lower PDP, individually. Reto Zimmermann and Wolfgang fichter in [2] conducts a logic style comparison which was based on full adder circuits. They found from the results that complementary CMOS can be used for the execution of arbitrary combinational if low voltage , low power and small power delay are taken into account. Suzuki, et al. in [4] introduces 1.5 ns 32b CMOS ALU which is fabricated at 0.25µm CMOS technology and 2.5V supply. They utilized double pass transistor logic and carry ahead adder circuit for the expansion time.

This proposed paper consists of two parts. Firstly, the functional simulation and verification of all the structures proposed in [1].Secondly, the implementation of a four-bit logical unit using mixed-logic designs method. The functional simulation and verification of all these structures were carried out by switch level modeling, using Verilog HDL.The functional verification of the LP, LPI, HP and the HPI structures of the two-to-four and four-to-sixteen decoders were carried out. The input-output vector pairs of the functional simulation were verified and found to be precise. Further, the LP structure of the two-to-four decoder is improved and is extended to form a four-bit logical unit to execute AND, OR, XOR and XNOR operations. The LP structure of the 4-bit logical unit was instigated using 198 transistors.

The rest of the paper is organized as follows: Section 2 gives a brief overview on the existing including low power gates, mixed logic design method. Section 3 provides an explanation about the proposed system using low power gates. Section 4 provides simulation results of the four bit logical unit. Section 5 provides the conclusion of the work presented.

2. EXISTING SYSTEM

An innovative mixed-logic design method involving TGL, DVL, and static CMOS was proposed in [1] to build four structures of two-to-four decoder. These structures are the low power (LP and LPI) and the high performance (HP and HPI) which are simulated by them using BSIM 4- based SPICE software at schematic level with 32 nm technology. To compare the performances of the mixed-logic method, they constructed a two-to-four decoder. At first, they designed a low power (LP) and low power inverting (LPI) structure, using fourteen transistors. Moreover, they designed a high performance (HP) and high performance inverting (HPI) structure using

fifteen transistors. The above four structures are implemented using two topologies namely 14- transistor 2-4 low power topology and 15-transistor 2-4 high performance topology.. Further they compared these structures with standard CMOS inverting and non-inverting structures consisting of twenty transistors. Further, they extended these two-to-four decoders to implement a four-to-sixteen decoder having LP, LPI, HP, HPI structures. By using this mixed -logic design method, they achieved a decrease in the number of gates, reduction in propagation delay and reduction in power dissipation and subsequently reduction in power delay product.

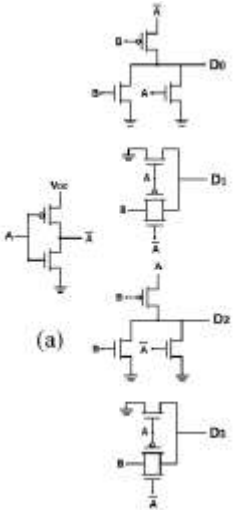

Fig-1: Existing System

3. PROPOSED WORK

In this work, we propose a logical unit using mixed logic design method. The proposed framework is as follows. Here A0B0, A1B1, A2B2, A3B3 are the inputs and Y0, Y1, Y2, Y3 are the outputs. S0 and S1 are the select lines used. When select lines '0' and '0' are selected, OR task should be executed. When select lines '0' and '1' is selected, either AND or XOR task should be performed. When '1 'and '1' select lines are selected XNOR task should be achieved. The fundamental target is to make consistent activities quicker.

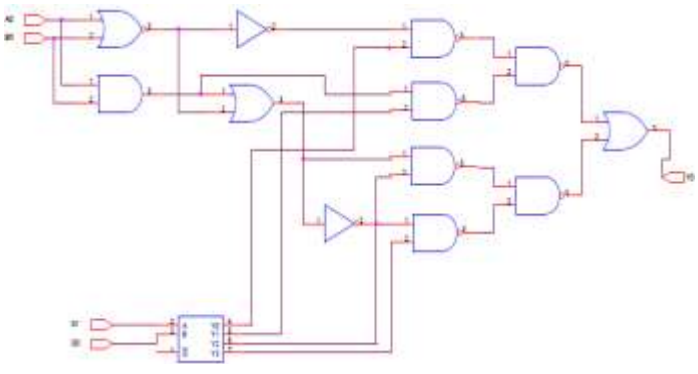

Fig -2: First Bit of the Logical unit

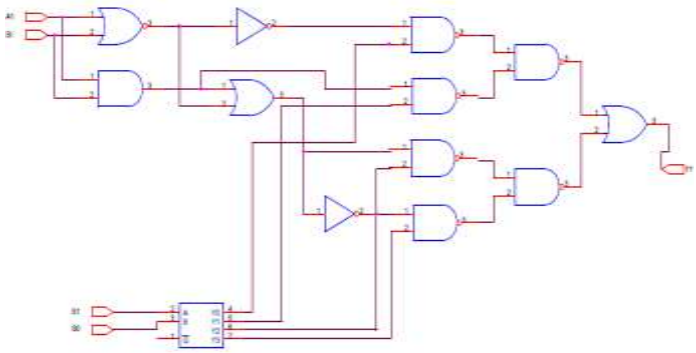

Fig -3: Second Bit of the Logical unit

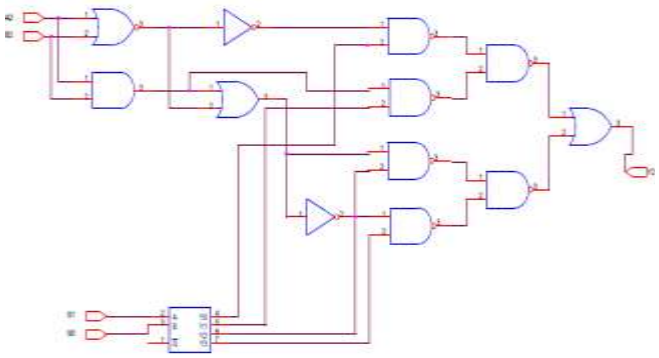

Fig -4: Third Bit of the Logical unit

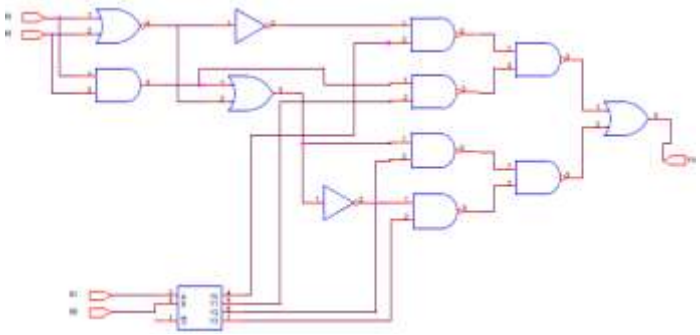

Fig -5: Fourth Bit of the Logical unit

4. SIMULATION RESULTS

In this proposed work, we use low power structure from the current framework for the further procedure. In order to perform the simulations, we use ModelSim simulator, and the functional simulation and verification of these structures were carried out by switch level modeling, using Verilog HDL. The low power structure from two-to-four decoder is modified and extended to execute four bit logical unit. The functionality of logical unit is tested using Verilog test bench. The layout of the logical unit was obtained by importing Verilog code to Microwind 2 layout design software. The two-to-four decoder low power waveforms are gotten and glued beneath in fig-3.

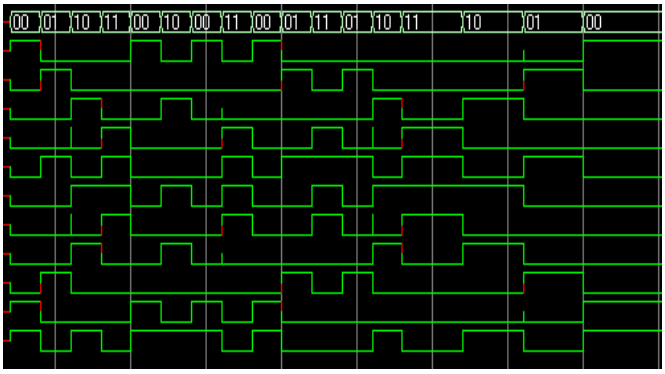

Fig-6 2:4 decoder low power result

Fig-7: Result of proposed logical unit

The fig-7 demonstrates a 4 bit logical unit using mixed logic design method. Since mixed logic method is utilized for the execution procedure. This consistent unit can works at a quick speed.

5. CONCLUSION

This paper introduces a 4-bit logical unit using mixed logic design method. Using this technique it helps to present a logical unit. The ModelSim simulator is used to execute the logical unit. With the help of low power gates in the mixed logic design method is used and the simulation is carried out by switch level modeling in Verilog HDL. The primary concern of the low power gates is to reduce area and also helps in the power minimization. The low power gates are modified and extended to implement logical operations such as OR, AND, XOR, XNOR. This logical unit has benefits such as error detection, error correction, generating hamming codes etc.

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