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Comparative Analysis of Various Sense Amplifiers in 45nm CMOS Technology

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Abstract - *This paper presents the delay and power measurement on transmission gate voltage mode sense amplifier and voltage mode sense amplifier. The first objective is to design the 8T SRAM and sense amplifier .The second objective is to identify the better performance analysis in terms of power, speed and area. This paper also contains the comparative analysis of different types of sense amplifiers like as voltage mode sense amplifier (VMSA), current mode sense amplifier (CMSA), and charge transfer sense amplifier (CTSA). My proposed circuit is transmission gate voltage mode sense amplifier (TGVMSA) and compare with VMSA. Sense amplifier plays an important role in semiconductor memories which used to sense the stored data in memory cell. Sense amplifier reduces the overall sensing delay and voltage. In this paper all circuit design analysis using Tanner 14.1 version simulation tool at 1.5v/45nm CMOS Technology. This result shows lower delay and power dissipation when compared with TGVMSA and VMSA. The TGVMSA has higher cell area but lower power dissipation and delay.*

Key Words: Sense amplifiers - VMSA, CMSA, CTSA, Delay, Power Dissipation, Transmission gate voltage mode sense amplifier.

1. INTRODUCTION

Static random access memories plays an important role in microprocessor and system on chip because SRAMs are important components of microprocessor and it serve as storage element in system on chip such as graphics, audio, video and image processors and this is also used in high performance graphics chips and microprocessors which requires high speed. This paper present different types of sense amplifier are used like as voltage mode sense amplifier (VMSA), current mode sense amplifier (CMSA) and charge transfer sense amplifier (CTSA). The proposed circuit is transmission gate voltage mode sense amplifier (TGVMSA). Sense amplifiers are use to detect the data from the selected memory array and this is require less power and give high performance which burning minimum amount of power. When increase the size of SRAM array the bit-line capacitance also increases which is the drawback of big performance of any sense amplifiers [1]-[2].

2. Related Work

2.1. Voltage Mode Sense Amplifier (VMSA)

Voltage mode sense amplifier detects the voltage difference between bit-line and bit-line bar. There are different type's sense amplifiers like as single ended sense amplifiers, differential amplifiers and cross-coupled sense amplifiers. Different types of sense amplifiers are used for different types of memory cells [1].

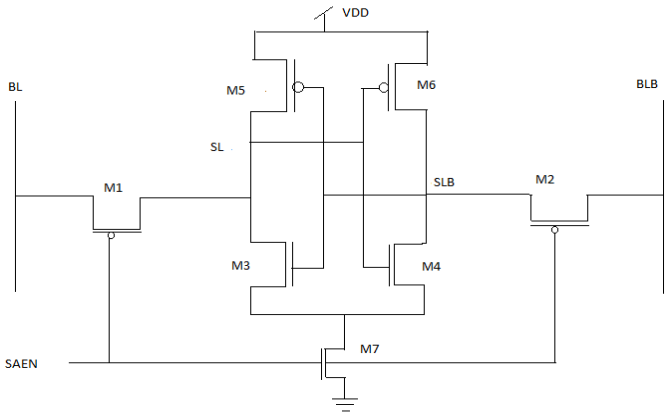

Fig -1: Cross-coupled voltage mode SA [4]

It is essential latch type cross-coupled voltage mode sense amplifier, once the decision process completed the current flow automatically stops. This sense amplifier is used to read the contents of various types of memory because achieve fast decision due to a strong positive feedback [2]. When SAEN goes to low then access transistors turned ON and then connected to bit-line and bit-line bar and this transferred to nodes SL and SLB respectively. Due to positive feedback, the maximum voltage goes to VDD and lower voltage goes to zero. The nodes SL and SLB show input and output at the same time [1].

2.2. Current Mode Sense Amplifier (CMSA)

When scaling the technology and increasing the number of cells which are attached to the column, the capacitances of bit-line is increasing [1]. Due to the increase of bit-line capacitance, which result time and delay also increases. So we preferred current mode sense amplifier because this is independent of bit-line capacitance and have low impedance to the inputs and give the differential current

rather than voltage between them. Which result to reduce the interconnect delay in long wire due to this improve the speed [3]. For reducing the voltage swings, cross-talk and substrate currents, applied the small input impedance the bit-lines [1]. The Ysel nodes select the sense amplifier and current will flow through the transistors via the bit-line loads node. The transistors T3 and T4 drain terminals connected to the data line which are very close to zero level [3].

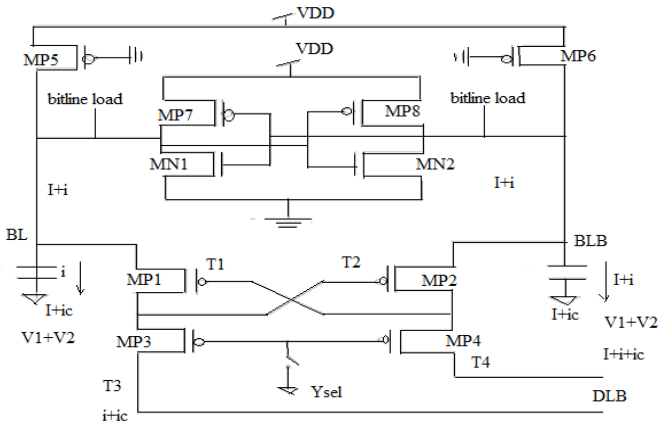

Fig -2: Current mode SA [3]

2.3. Charge Transfer Sense Amplifier (CMSA)

In this sense amplifier the charge is redistribution from high bit-line capacitance to low capacitance of the node of Sa and Sa#. This result gives the high speed and low bit-line swing. The second part of CTSA formed the cross-coupled inverter from transistors M7 through M11 and latches the output of common gate amplifier nodes Sa and Sa#. When SAen goes to low then CTSA enabled. Suppose initially bit-line bl# goes to low and its voltage goes to Vb + |Vtp| due to this voltage M1 goes into sub-threshold region of operation and this stop the charging of output node Sa# while the other bit-line remains the high and node Sa charged high [4].

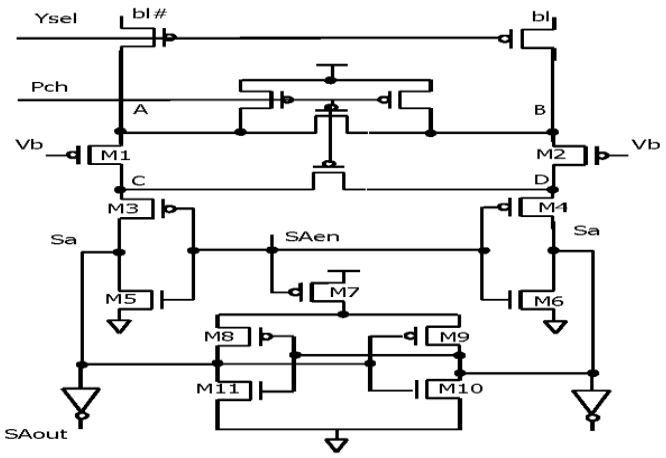

Fig -3: Charge transfer SA [3]

3. Proposed Circuit

3.1 Transmission Gate VMSA

This circuit contains two transmission gates which are replaced by two access transistors which is connected to bit-line and bit-line bar. The working of this circuit similar to voltage mode sense amplifier but only changes in transmission gate in place of access transistors which is very important role play for working of sense amplifier. This circuit is also called the cross-coupled transmission gate voltage mode sense amplifier. The transistors M3-M6 form the cross-coupled inverters. This circuit detects the voltage difference between bit-line and bit-line bar so this is called voltage mode sense amplifier.

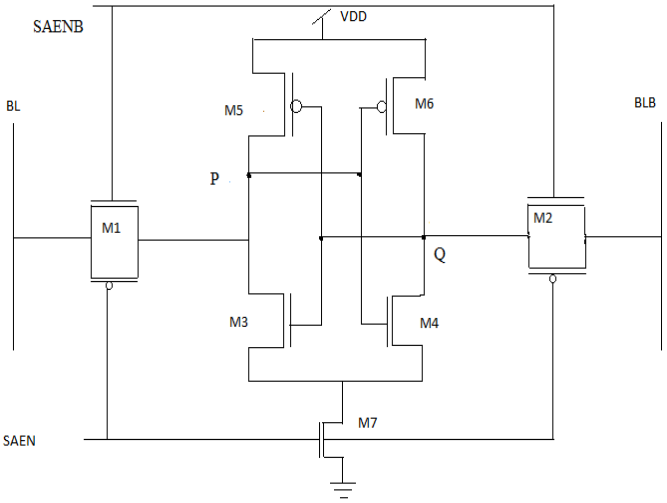

Fig -4: Transmission Gate VMSA [3]

The speed of this proposed circuit improves and minimizes the dynamic power dissipation. So the performance of this circuit better than voltage mode sense amplifier. Transmissions gate basically the combination of PMOS and NMOS which is connected to SAEN and SAENB respectively. The transistors M7 works as sense transistor when SAEN goes to low the PMOS transistors ON and NMOS transistors OFF. Then the PMOS transistors connected to bit line and bit-line bar and sensing the voltage difference between them and transferred to P and Q nodes. Due to positive feedback the higher voltage goes to VDD and lower goes towards the zero. The nodes P and Q called input and output terminals at the same time.

4.0. Design and Simulation Results

4.1 Schematic of Voltage Mode SA

Table -1: Voltage Mode SA Dimensions

	Length(L)	Width(W)
MN1,MN2,MN3	45nm	135nm
MP1,MP2,MP3,MP4	45nm	90nm

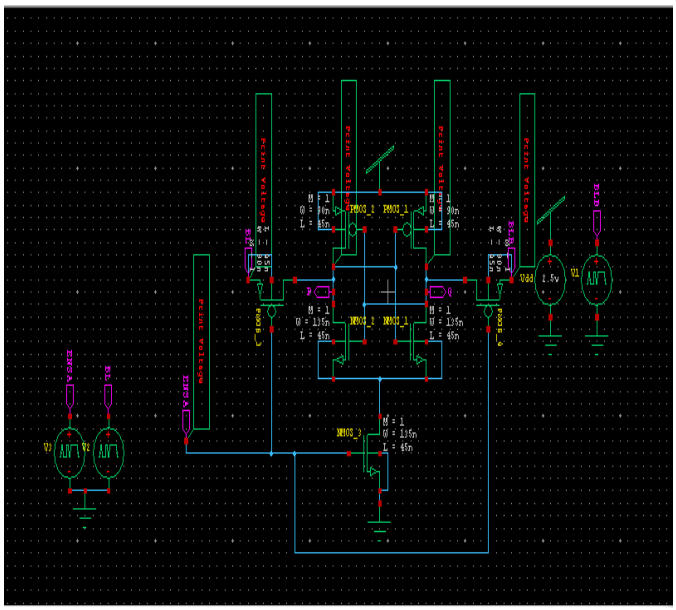

Fig -5: Schematic of Voltage Mode SA

4.2 Output Waveform of Voltage Mode SA

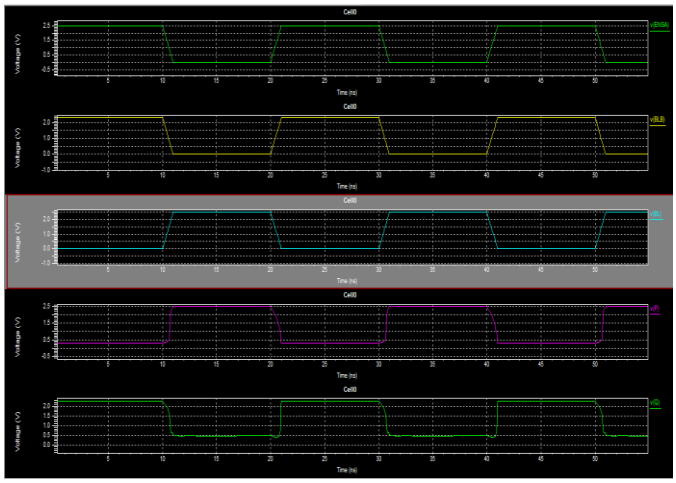

Fig -6: Output Waveform of VMSA

4.3 Schematic Diagram of Transmission Gate Voltage Mode Sense Amplifier

Table -2: TGVMSA Dimensions

	Length (L)	Width(W)
MP1,MP2,MP3,MP4,MP5,MP6,MP7, MP8	45nm	90nm
MP9,MP10,MP11,MP12,MP13,MP14 ,MP15,MP16	45nm	135nm
MN1,MN2,MN3,MN4,MN5,MN6	45nm	180nm

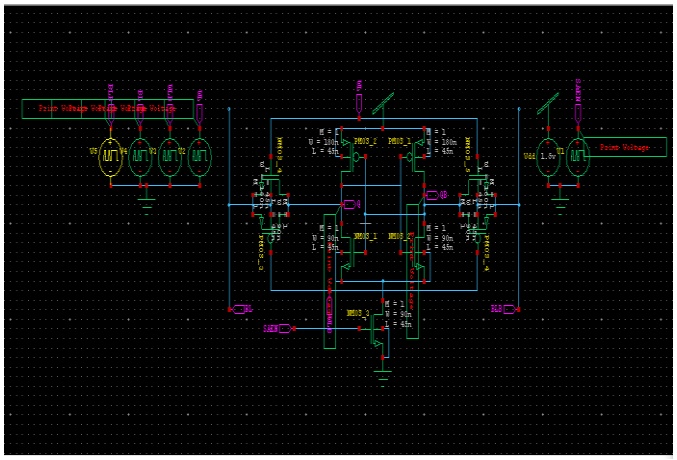

Fig -7: Schematic Diagram of Transmission Gate VMSA

4.4 Output Waveform of Transmission Gate VMSA

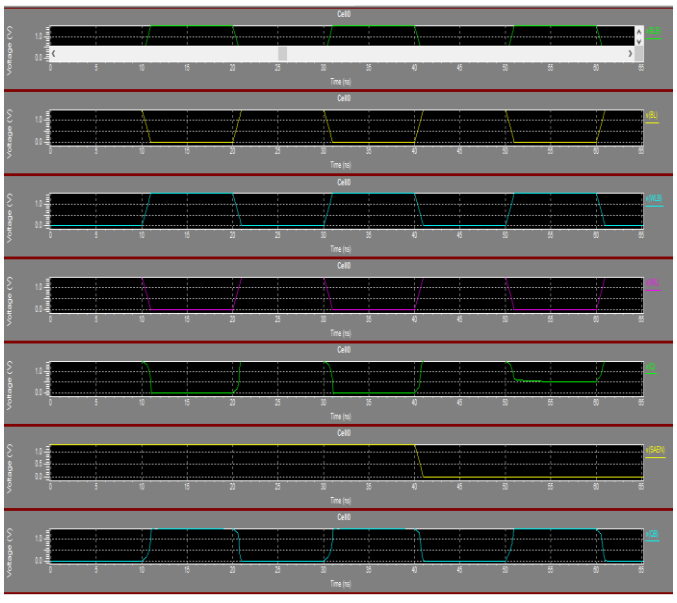

Fig -8: Output Waveform of Transmission Gate VMSA

Table -3: Power Comparison Table

Power Supply	Voltage Mode Sense Amplifier	TGVMSA
1.0V	$2.015502e^{-005}$ Watt	$8.576412e^{-006}$Watt
1.5V	$6.782127e^{-006}$ Watt	$5.726068e^{-006}$Watt
2.0V	$2.355809e^{-005}$ Watt	$2.083784e^{-005}$Watt
2.5V	$1.496455e^{-004}$ Watt	$1.148314e^{-004}$Watt
3.0V	$6.362099e^{-004}$ Watt	$5.204229e^{-004}$Watt
3.5V	$6.306575e^{-003}$ Watt	$6.165399e^{-003}$Watt
4.0V	$4.668120e^{-002}$ Watt	$4.109383e^{-002}$Watt
4.5V	$1.570941e^{-001}$ Watt	$1.205080e^{-001}$Watt

4.5 Comparison Graph

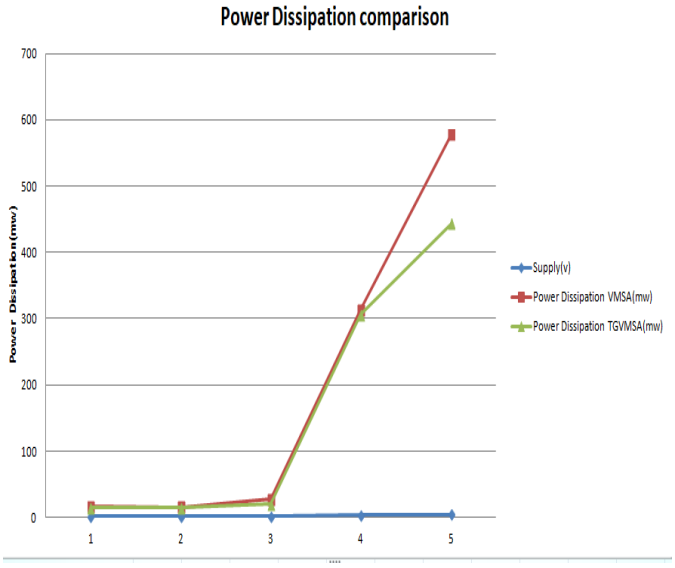

Fig -9: Comparison Graph between VMSA and TGVMSA

This graph shows the power comparison between voltage mode sense amplifier and transmission gate voltage mode sense amplifier. When increase the supply voltage then increases the power in voltage mode sense amplifier but in transmission gate voltage mode sense amplifier the power is decreases.

Table -4: Propagation Delay Time Comparison Table

Supply Voltage(v)	VMSA(µs)	TGVMSA(µs)
1.5	1364.22	1028.76
2.0	1367.01	1031.54
2.5	1368.11	1033.22
3.0	1369.79	1034.33
3.5	1370.59	1035.13
4.0	1371.20	1035.74

4.6 Comparison Graph

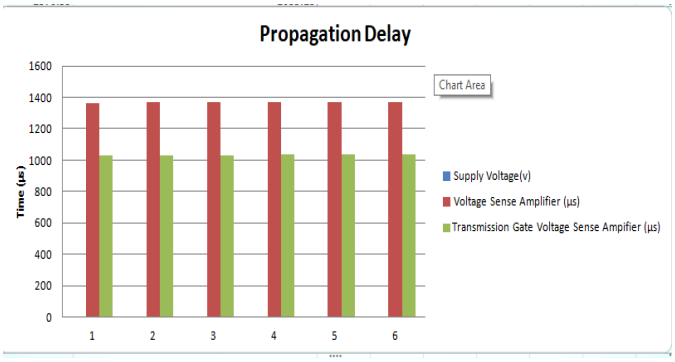

Fig.10. Comparison Graph between VMSA and TGVMSA

5. CONCLUSION:

This paper presents the delay and power measurement on transmission gate voltage sense amplifier and voltage mode sense amplifier. In this paper all circuit design analysis using Tanner 14.1 version simulation tool at 1.5v/45nm CMOS Technology. The TGVMSA has higher cell area but lower power dissipation and delay. The result is minimizing the power dissipation and propagation delay in comparison to voltage mode sense amplifier. So this proposed circuit gives the better performance.

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BIOGRAPHIES

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