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DESIGN OF MEMRISTOR BASED MULTIPLIER

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Abstract - *Memristor is a novel technology, the fourth fundamental passive element to overcome the limitations faced by the CMOS technology. Memristor has the capacity of memory but cannot store energy[9]. Multiplier is one of the basic circuits in the field of digital signal processing and are used in various applications such as FFT. In this paper, a 4 bit multiplier is realised and implemented using the memristor-cmos hybrid technology and the results are analysed in the LTspice tool.*

Key Words: **Memristor, window function, state variable, array multiplier, xnor, full adder.**

1. INTRODUCTION

In 1971,Professor Leon Chua discovered the existence of the fourth fundamental passive element known as the memristor. But its research had not progressed untill 2008 because of the absence of physical prototype of the memristor. With the invention of physical modelling of memristor device in 2008 by the HP Labs, there has been a drastic increase in the research to realise various existing circuits in memristors. Multiplication is one of the key operation in digital signal processing algorithms like digital filtering, linear transformation, correlation and wavelet compression.Various effiicient array and parallel multipliers have been proposed and many of them boost the speed of multiplication at the cost of large VLSI area and high power dissipation[1]. In recent years, several power reduction techniques have been proposed for low power digital design, including the reduction ofsupply voltage, multi-threshold logic and the clock speed, the use of signed magnitude arithmetic and differential data encoding,the parallisation of operations and the timing if input bit patterns to reduce switching[2]. A basic multiplier can be divide into 3 parts 1).partial product generation 2).partial product addition and 3).final addition. It has been recognised that full adder circuits have significant impact on the overall power and area consumption and the speed of multipliers built on these adders. Many new full adder circuits have been proposed and here,xnor based full adder is implemented in array multiplier which can be extended to other multipliers and studied.

In this paper, we implemnt an area efficient array multiplier that uses memristor-cmos hybrid technology. The rest of the paper is organised as follows.section II consists of brief description of memristor working. Section III explains the concept of window functions for memristor and the various window functions experimented in this project and its outcome. Section IV implements the 2 bit and 4 bit array multiplier structure with the memristor-cmos hybrid technology.The results are analysed analysed in LTspice tool in section V. section VI presents the conclusion of the work.

2. MEMRISTOR WORKING

In 2008, the HP laboratory team developed the memristor element with typical resistive features successfully. The range of memristor value reflects the memory effect and is equal to the time integration of the currents that cross through the memristor before the time instant[6].

Memristor reflects the relationship between the charge and the magnetic flux, and accordingly to these fundamental circuit variables, a memristor can be divided into two types, the charge controlled memristor and the flux controlled memristor[6].

The titanium-dioxide memristor nano-structure is described by Strukov and William as in figure 1.The left region if the TiO2 memristor structure with a length l is partially doped with process with oxygen vacancies using an initial electroforming process with a high constant voltage and has low resistance[8]. The second sub-layer of the memristor is prepared of pure TiO2 and it has very high resistance. The length of the whole memristor nano-structure is denoted with D [8].

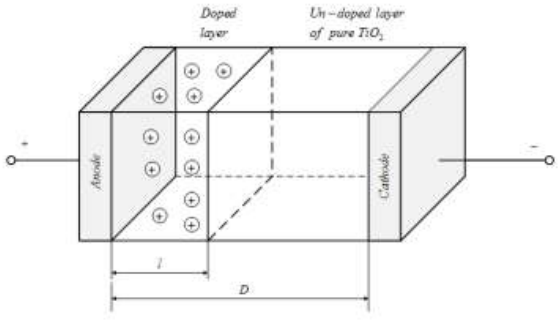


Fig-1: memristor nano structure

The equivalent resistance of the memristor element could be expressed as assumption of series connection of doped and undoped regions[8] as given in figure 2.

R=Rdoped + Rundoped

=Ron.x + Roff(1-x)

Where x is the state variable of the memristor.

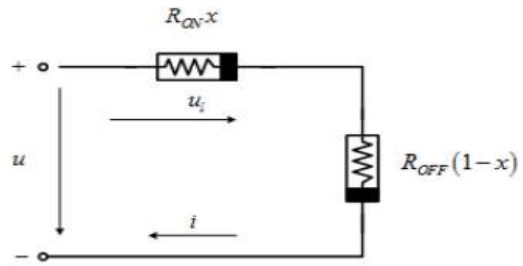


Fig- 2: resistance of memristor layers.

3. WINDOW FUNCTION

Window function is the additional term in the state equation of the memristor which models the non linear behavior at the device boundary[9]. Various window functions are proposed to construct the non linear drift model such as a simple window function, switching window function[6]. An effective window function has to have certain features to make the memristive device work well. Those properties are as follows. 1).boundary conditions at either end of the device are taken into account. 2). Non linear ionic transport of the memristor is described. 3). Provide linkage between linear and non linear model. 4). Flexible scalability to adjust the maximum value of the function between 0 and 1. 5). Resolve boundary lock problem[6]. A basic or gate simulation is run with different window functions and the results are as follows.

3.1. Joglekar window function

F(x) = 1- (2x-1)^2p ; x=w/D, p is a positive integer.

The function guarantees zero speed of the boundary when approaching either zero or D. The disadvantage is that when the device is at the boundary, it becomes difficult for the state variable to change and no external stimulus can change this.

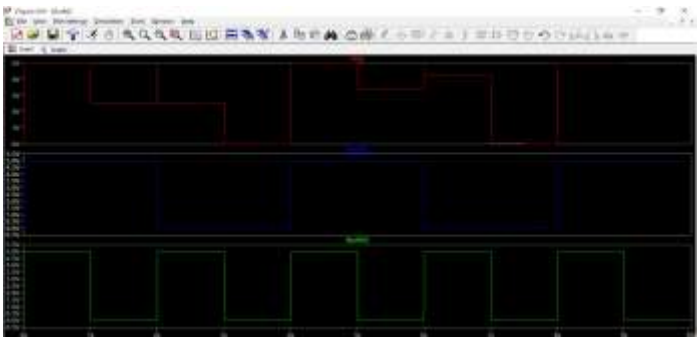


Fig-3: OR gate using Joglekar window function

3.2 Jinxiang window function.

F(x) = j(1-[a(w-stp(-i)^2p + (1-a)]^p)

Where w is the state variable.

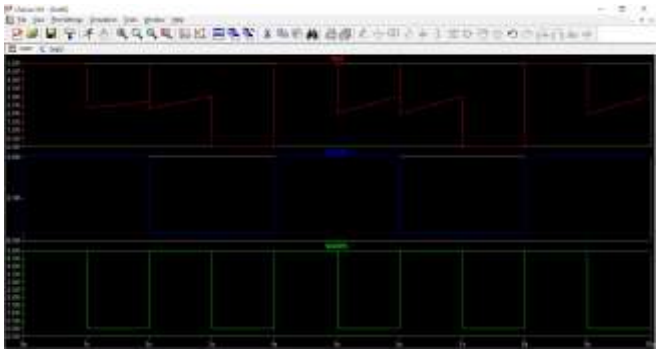


Fig-4 :OR gate using jinxiang function

3.3.Prodromakis window function.

F(x) = j[1-(x-0.5)^2 + 0.75] ^p

J is the control parameter that specifies the value of the function.

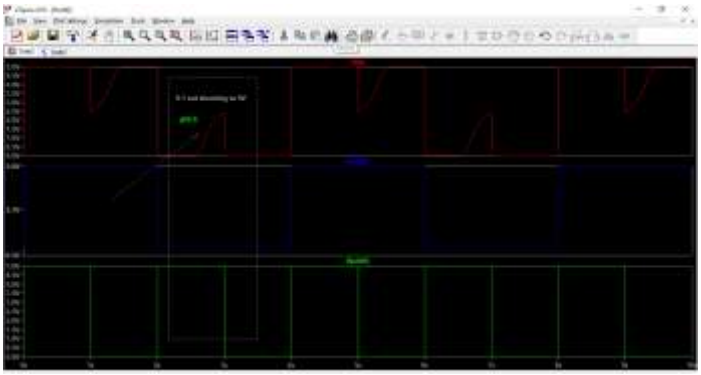


Fig-5: OR gate using prodromakis function.

3.4 Biolek window function.

F(x)= 1-(x-sgn(-i))^2p

sgn(-i) = 1 when i>=0

sgn(-i) = 0 when i<0

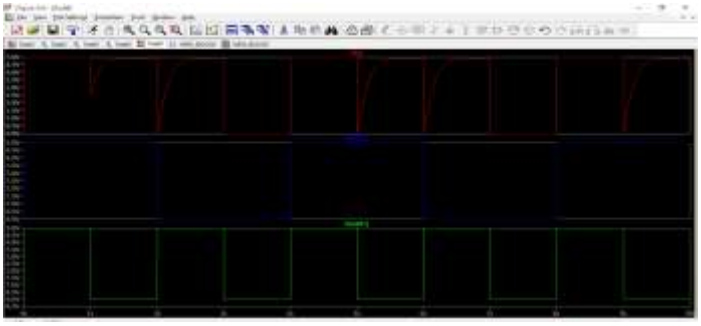
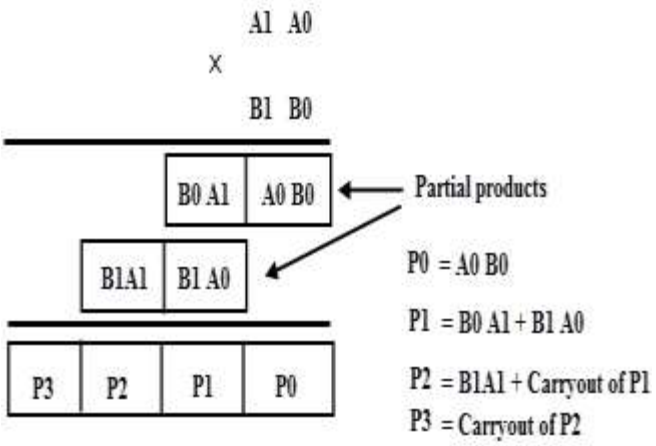


Fig- 6: OR gate using biolek function

From the analysis and results, it is suggested that the choice of the biolek window function for the further process.

4. METHODOLOGY AND IMPLEMENTATION

The two bit multiplier is mathematically done as following



Out of the three logic families the MRL logic family[15] is chosen and 2 bit array multiplier is built as shown in the figure7.

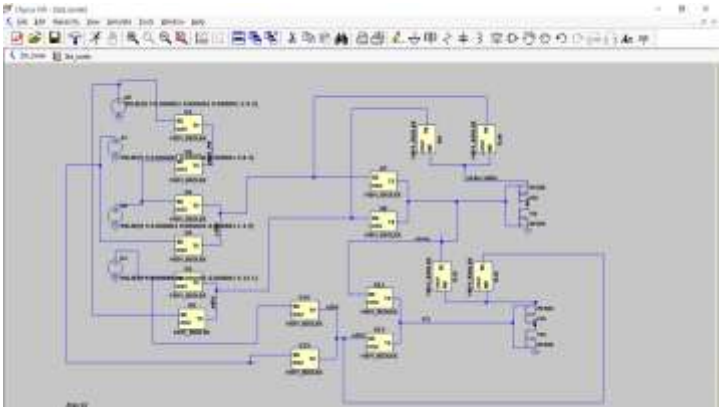


Fig-7: schematic of 2 bit array multiplier

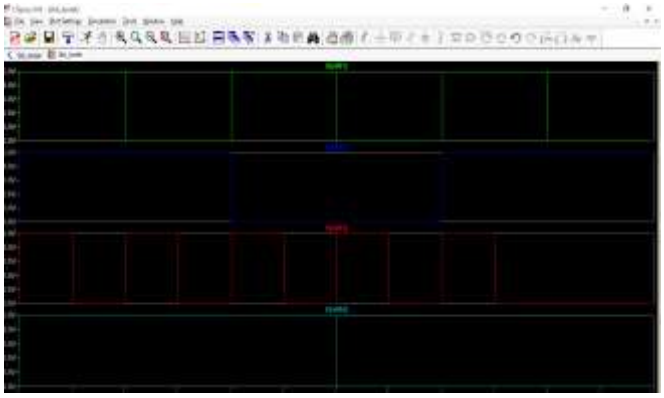


Fig-8: input to the 2 bit multiplier

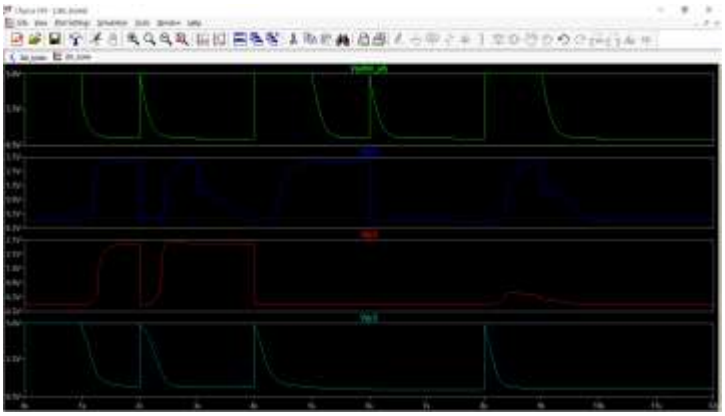


Fig-9: output of the 2 bit multiplier

The input to the multiplier and the result is given in fig. 8 and fig. 9. The circuit suffers from the problems of glitches and degradation. There are two reasons for the glitches to be present.

1. Dynamic hazard causing situation is when the initial resistance is high as Roff. In that case current is small , therefore settling time increases providing a dynamic hazard. To overcome this problem the full adder is implemented in terms of xnor[14]. The sum and carry of full adder can be realized as

$$S = A \odot B \odot Cin$$

$$Cout = A \odot BCin' + A \oplus B\,Cin$$

The truth table of the full adder is as shown in fig 10. The NAND,NOR logic is implemented as shown in fig 11 a,b. For nor simulation in LTSPICE choose the nmos to have high Ron greater than2000 and Vds around 100-250. BSP89, BSS123, RK7002BM, MDC2007002N, RHU002N06, R0C002N05 are the part numbers of the nmos that can selected for nor simulation. For nand simulation in LTSPICE, keep the Vds value close to 100 and Ron less around 6. The nmos BSC060N10n53 is used in this simulation.

X	Y	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig-10: truth table of full adder

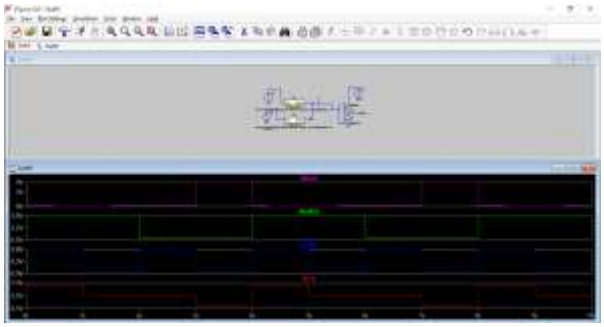


Fig-11(a): NOR circuit and simulation output

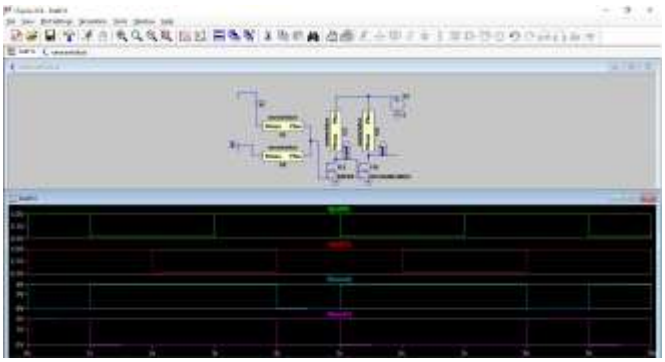


Fig-11(b): NAND circuit and simulation result

The xnor based 1bit full adder[14] is as shown in the figure 12a and its output transient analysis is given in figure 12b. The 4 bit array multiplier as proposed in[2] is implemented using the xnor based full adder.

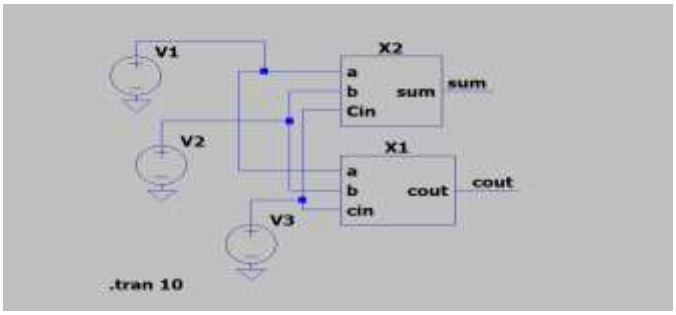


Fig -12(a): 1 bit full adder

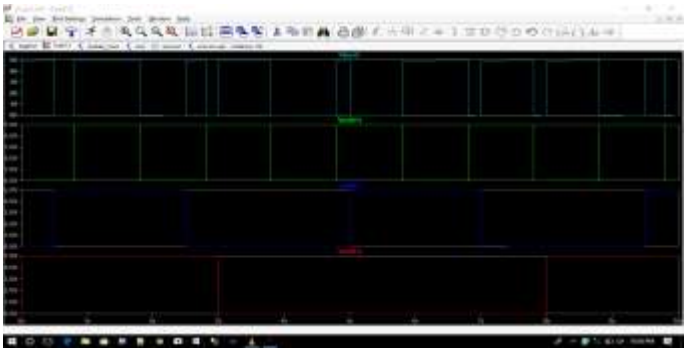


Fig- 12(b): simulation of 1 bit full adder.

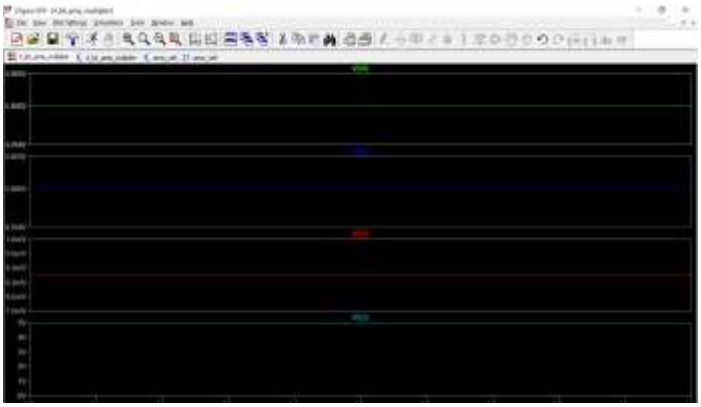


Fig -13(a): 4 bit multiplicand

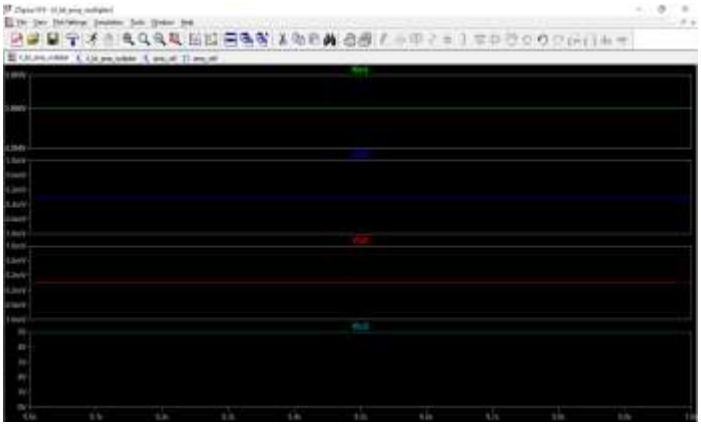


Fig -13(b): 4 bit multiplier

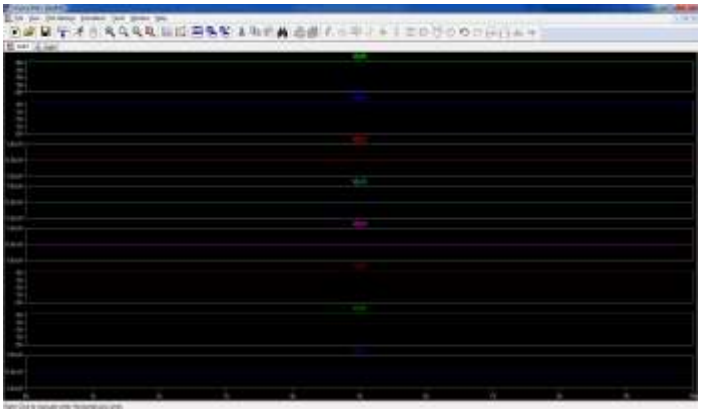


Fig- 14: 4 bit result

5. PROPOSED DESIGN

In the proposed design, the conventional modified gate diffusion input technique is modified and uses only one memristor and nmos to implement various logic gates. The various gates implemented using this method is as shown in figure15.

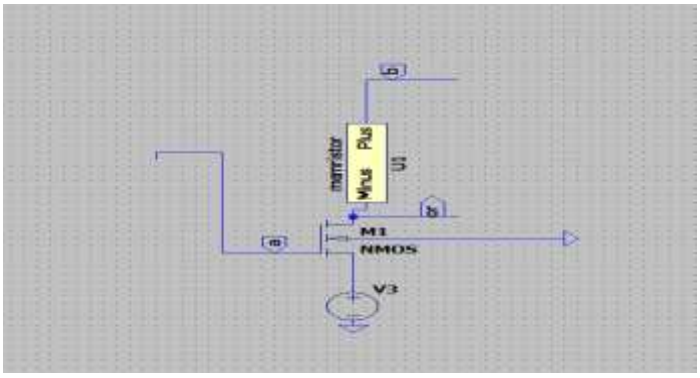


Fig -15(a): OR gate

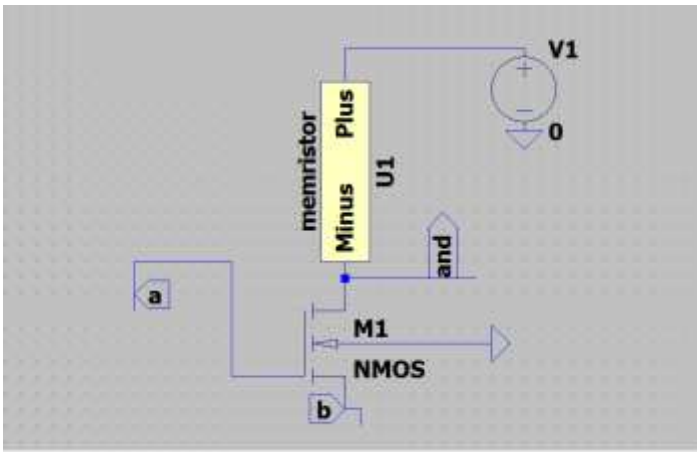


Fig -15(b): AND gate

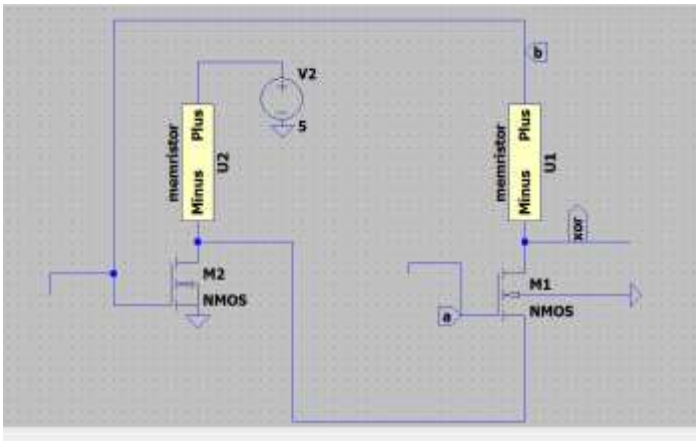


Fig -15(b): XOR gate

Using the above gates, we can implement the full adder and hence the 4 bit array multiplier in Ltspice. The schematic of the 4 bit multiplier and its output is shown in the following figures for the following bit pattern.

A3 A2 A1 A0 * B3 B2 B1 B0

0 1 0 1 0 0 1 1

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0 1 0 1

0 1 0 1

0 0 0 0

0 0 0 0

---

0 0 0 0 1 1 1 1

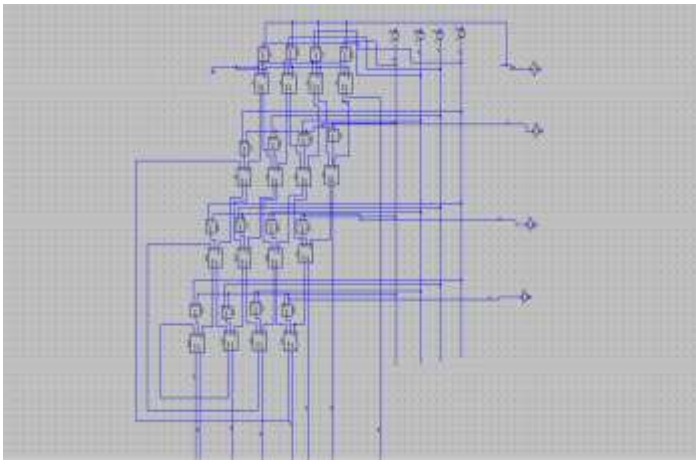

Fig -16(a): 4 bit array multiplier

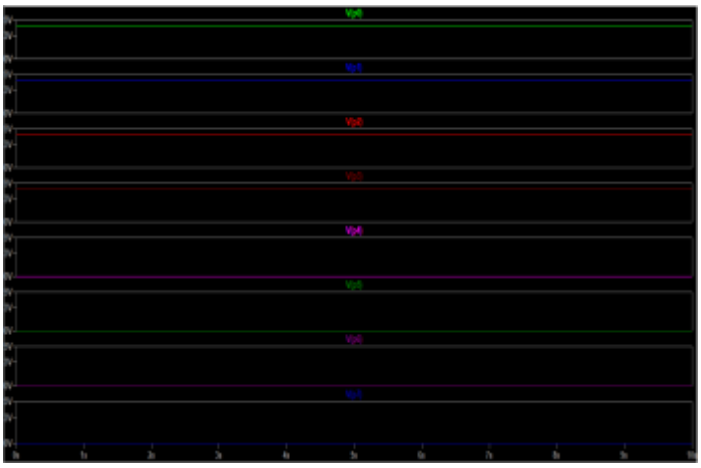

Fig -16(b): 4 bit array multiplier

6. RESULTS AND DISCUSSION

The array multiplier architecture implemented with carry save adder requires 16 full adders and 12 and gates. To implement the said architecture in the conventional cmos technology:

1 full adder by cascading 2 half adders requires 21 nmos and 21 pmos.

1 and gate realization involves 3 nmos and 3 pmos.

Therefore for 16 full adders and 12 and gate, the number of mosfets used

=372nmos + 372 pmos= 744 mosfets.

To implement the said architecture in xnor based full adder:

1 full adder requires 15 nmos and 15 memristors,

1 and gate requires 4 memristors and 2 nmos.

For 16 full adder, we require 240 memristor and 240 nmos

For 12 and gates ,we require 48 memristor and 24 nmos.

Therefore, the total number of nmos and memristors used=552.

To implement the 4 bit array multiplier architechture in the proposed design:

1 full adder requires 5 memristors and 5 nMOSFETS.

1 AND gate requires 1 memristors and 1 nMOSFET.

Therefore, for 16 full adders, we require 80 memristors and 80 nMOSFETS.

12 AND gates require 12 memristors and 12 nMOSFETS.

Totally, to implement a 4 bit array multiplier design we require 92 memristors and 92 nMOSFETS with a total count of 184 including both memristors and nMOSFETS.

Table -1: Comparison of various design against component count

LOGIC/DESIGN	nMOS	pMOS	Memristors	Total
CMOS	372	372	0	744
MRL	32	32	184	248
XNOR based full adder	264	0	288	552
Proposed	92	0	92	184

All the methods adopted reduces the area consumed by the multiplier with the same functional efficiency. Memristors have been used in place of pmos in and circuit. In cmos technology, conventionally , to match the mobilities of the holes and the electrons, the size of pmos is chosen twice that of the nmos size. The size of the memristor is nano scale and is merely 10nm, as compared to the bulk cmos technology. The use of memristors helps to achieve area reduction by the reduction in the number transistors required.

7. CONCLUSION

The array multiplier is implemented for 2 bit and 4 bit in LTspice tool. The reduction in the transistor count becomes significant when higher bit multiplication in implemented. The less transistor count can trade off power consumption and area. In recent years, many new full adder designs have been developed that has lesser transistor count. Integration of memristors to such full adders is future scope of work.

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