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# MODELLING AND SIMULATION OF HYBRID CASCADED H-BRIDGE MULTILEVEL INVERTER

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**Abstract:** In recent years, a number of noteworthy researches have been carried out to design multilevel inverters (MLI) to produce a high number of levels with reduced total harmonic distortion (THD). Multilevel inverters are used to extract power from renewable energy sources. This research focuses on improving the efficiency of the multilevel inverter and quality of output voltage waveforms. Moreover, this research work is devoted to calculating the total harmonic distortion and its minimization. In this research, the performances of a symmetric 7 level, binary asymmetric 15 level, trinary asymmetric 27 level cascaded multilevel inverter and 27 level semi cascaded multilevel inverter topologies with respect to the output voltage, total harmonic distortion, number of levels, number of switches and switching stresses on the switches have been discussed. This paper proposes a modified hybrid sub-multi-level cell inverter model with a lesser number of switches while it can attain a higher number of voltage levels. MATLAB simulations are carried out to verify the proposed topology and compared with other conventional inverter models.

### *Key words:* Multilevel Inverter (MLI), total harmonic distortion (THD), symmetric, asymmetric.

#### 1. INTRODUCTION

An inverter is basically a power device that converts DC to AC. A normal inverter is limited to two-level which usually has some drawbacks as it gives rises to harmonic distortions and flickering in the output voltage and creates problem in applications where low distortion is required. Hence, recently the concept of multilevel inverters has emerged in the field of power electronics since it can produce more voltage levels causing lower harmonic distortion from a medium source voltage. The more the number of levels the smoother the ac waveform. The topology of a multilevel inverter can be expressed as a series combination of H-bridge inverters consisting of several switches.

A multilevel inverter includes several topologies out of which three topologies are common which include Cascaded H-bridge multilevel inverter (CHB-MLI), diode clamped multilevel inverters and flying capacitor multilevel inverter [1]. Amongst these MLIs the most preferred one is the cascaded H-bridge multilevel inverter due to its simplicity in configuration and usage of basic method of multilevel inverter [2].

#### 1.1 Cascaded H-Bridge Multilevel Inverter

Cascaded H Bridge multilevel inverter, also known as multicell inverter is supplied by isolated dc source on its DC side [3]. It can be used for single phase as well as three phase conversion. Solar panels, batteries or fuel cells are used as isolated DC sources. The total output voltage is the sum of voltages produced by each H-bridge connected in series.

Cascaded H- bridge multilevel inverters (CHB-MLI) have two different structures: symmetric and asymmetric.

When the isolated DC sources supplied to each cell of a CHB-MLI have equal magnitude, the structure is symmetric whereas asymmetrical multilevel inverters have an advantage of producing more number of output level without increasing the number of cells [4]. They are further subdivided into binary asymmetric inverter and trinary asymmetric inverter.

- a) If dc voltage sources are in the ratio of 1:2, the inverter is known as binary asymmetric multilevel inverter.
- b) If dc voltage sources are in the ratio of 1:3, the inverter is known as trinary asymmetric multilevel inverter.

# 1.2 Comparison Table Between Symmetric and Asymmetric MLI

Table -1: Comparison table

Parameters	Symmetric	Asymmetric					
		Binary	Trinary				
No. of levels	2n+1	2 <sup>(n+1)</sup> -1	3 <sup>n</sup>				
No. of switches	4n	4n	4n				
Max. output voltage	$nV_{ m dc}$	(2 <sup>n</sup> -1)V <sub>dc</sub>	3				

Here, n is the number of input DC sources. The parameters in the above table have been carried out by geometric progression.

**Table- 2:** Comparison table for n=3

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Parameters	Symmetric	Asymmetric				
		Binary	Trinary			
No. of levels	7	15	27			
No. of switches	12	12	12			
Max. output voltage	$3V_{dc}$	$7V_{dc}$	13V <sub>dc</sub>			

Here, considering, number of input sources n=3, the parameters have been calculated for further analysis.

From the above table, it is seen that the trinary asymmetrical multilevel inverter produces more voltage levels and higher maximum output voltage with the same number of bridges as compared to symmetrical and binary asymmetrical structure. To verify this, the performances of these cascaded H-bridge MLIs are observed using MATLAB/Simulink.

# 1.3 Basic Structue of Conventional Cascaded n-input MLI

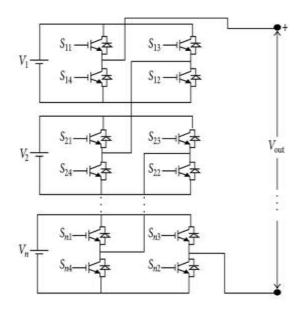


Fig-1: Single phase conventional n-input CHB-MLI

The conventional CHB-MLI consists of n number of H-bridges connected in series, each consisting of four switches and four voltage sources with equal and unequal magnitude for symmetric and asymmetric configuration respectively. For simulation purpose the DC input voltage  $V_{\rm dc}$  is taken to be 12 volts

### 2. SIMULATION WORK FOR 7 LEVEL, 15 LEVEL AND 27 LEVEL CHB-MLI

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#### 2.1 Switching Scheme

#### 2.1.1 Seven Level Symmetric CHB-MLI

Table- 3: Switching scheme for 7 level CHB-MLI

Levels	S1	S2	<b>S</b> 3	S4	S5	<b>S</b> 6	<b>S</b> 7	<b>S</b> 8	<b>S</b> 9	S10	S11	S12
1	1	1	0	0	1	1	0	0	1	1	0	0
2	1	1	0	0	1	1	0	0	0	1	0	1
3	1	1	0	0	0	1	0	1	0	1	0	1
4	0	1	0	1	0	1	0	1	0	1	0	1
5	0	0	1	1	0	1	0	1	0	1	0	1
6	0	0	1	1	0	0	1	1	0	1	0	1
7	0	0	1	1	0	0	1	1	0	0	1	1

#### 2.1.2 Fifteen level Binary Asymmetric CHB-MLI

Table- 4: Switching scheme for 15 level CHB-MLI

Levels	<b>S</b> 1	S2	<b>S</b> 3	S4	S5	<b>S</b> 6	<b>S</b> 7	<b>S</b> 8	<b>S</b> 9	S10	S11	S12
1	1	1	0	0	1	1	0	0	1	1	0	0
2	0	1	0	1	1	1	0	0	1	1	0	0
3	0	0	1	1	1	1	0	0	1	1	0	0
4	0	1	0	1	0	1	0	1	1	1	0	0
5	0	0	1	1	0	1	0	1	1	1	0	0
6	0	1	0	1	1	1	0	0	0	1	0	1
7	1	1	0	0	0	1	0	1	0	1	0	1
8	0	1	0	1	0	1	0	1	0	1	0	1
9	0	0	1	1	0	1	0	1	0	1	0	1
10	0	1	0	1	0	0	1	1	0	1	0	1
11	1	1	0	0	0	1	0	1	0	0	1	1
12	0	1	0	1	0	1	0	1	0	0	1	1
13	0	0	1	1	0	1	0	1	0	0	1	1
14	0	1	0	1	0	0	1	1	0	0	1	1
15	0	0	1	1	0	0	1	1	0	0	1	1

#### 2.1.3 Twenty Seven Level Trinary Asymmetric CHB-MLI

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Table 5: Switching scheme for 27 level CHB-MLI

Levels	S1	S2	S3	S4	S5	S6	<b>S</b> 7	S8	<b>S</b> 9	S10	S11	S12
1	1	1	0	0	1	1	0	0	1	1	0	0
2	0	O	0	0	1	1	0	0	1	1	0	0
3	0	O	1	1	1	1	0	0	1	1	0	0
4	1	1	0	0	0	0	0	0	1	1	0	0
5	O	O	0	0	0	0	0	0	1	1	0	0
6	0	0	1	1	0	0	0	0	1	1	O	O
7	1	1	0	0	O	0	1	1	1	1	0	0
8	0	O	0	0	O	O	1	1	1	1	0	0
9	0	O	1	1	0	0	1	1	1	1	O	O
10	1	1	0	0	1	1	0	0	0	0	O	O
11	0	O	0	0	1	1	0	0	O	0	0	0
12	0	0	1	1	1	1	0	0	0	0	O	O
13	1	1	0	0	O	0	0	0	O	0	0	0
14	0	O	0	0	O	0	0	0	O	0	0	0
15	0	O	1	1	O	0	0	0	O	0	0	0
16	1	1	0	0	0	0	1	1	0	0	O	O
17	0	O	0	0	O	0	1	1	O	0	0	0
18	0	0	1	1	0	0	1	1	0	0	O	O
19	1	1	0	0	1	1	0	0	0	0	1	1
20	0	O	0	0	1	1	0	0	O	0	1	1
21	0	O	1	1	1	1	0	0	O	0	1	1
22	1	1	0	0	0	0	0	0	O	0	1	1
23	0	0	0	0	0	0	0	0	0	0	1	1
24	0	O	1	1	0	0	0	0	O	0	1	1
25	1	1	0	0	1	1	0	0	O	0	1	1
26	0	0	0	0	0	0	1	1	O	0	1	1
27	O	0	1	1	O	O	1	1	O	0	1	1

#### 2.2 OUTPUT WAVEFORM

# 2.2.1 Seven Level Symmetric CHB-MLI 2.2.2

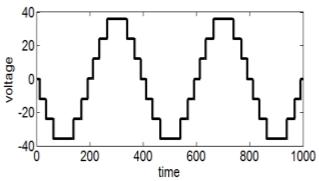


Fig- 2: Output waveform of 7 level CHB-MLI

#### 2.2.2 Fifteen Level Binary Asymmetric CHB-MLI

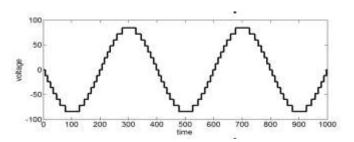


Fig-3: Output waveform of 15 level CHB-MLI

# 2.2.3 Twenty-seven Level Trinary Asymmetric CHB-MLI

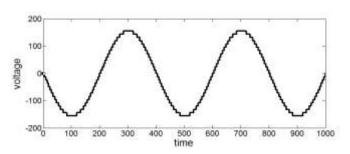


Fig-4: Output waveform of 27 level CHB-MLI

#### 2.3 Total Harmonic Distotation by FFT Analysis

#### 2.3.1 Seven Level Symmetric CHB-MLI

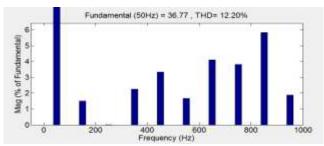


Fig-5: THD (12.20%) of 7 level CHB-MLI

#### 2.3.2 Fifteen Level Asymmetric CHB-MLI

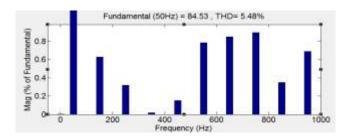


Fig-6: THD (5.48%) of 15 level CHB-MLI

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#### 2.3.3 Twenty-Seven Level Asymmetric CHB-MLI

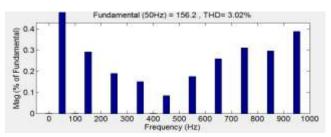


Fig-7: THD (3.02%) of 27 level CHB-MLI

Comparing the voltage levels, maximum voltage and THD of 7 level,15 level and 27 level CHB-MLI, it can be analyzed that the 27 level trinary asymmetric inverter is found to be the most efficient among the other three inverters. With the same number of DC input sources and switches i.e. 3 and 12 respectively, the output waveform produced by 27 levels CHB MLI has been found to be more similar with sinusoidal waveform. It produces a maximum output voltage of 13V<sub>dc</sub> other than  $3V_{dc}$  and  $7V_{dc}$  in 7 and 15 level CHB-MLIs respectively. Moreover, it produces a very less THD as compared to the other two inverters. But there lies an issue in terms of the switching frequency of the 27 level inverter. Due to frequent switching of the switches there will be switching losses and hence the life of the switches will be reduced. Thus, in those cases frequent maintenance of the inverter will be required.

So, to overcome this problem a 27 level semi cascaded inverter is designed.

## 3. SIMULATION OF 27 LEVEL SEMI CASCADED H-BRIDGE MLI

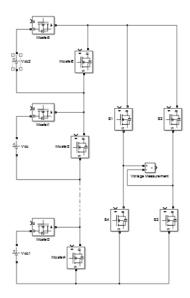


Fig-8: Conventional n-input semi cascaded MLI

**Table-6:** Table to calculate different parameters for n-input semi cascaded MLI

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Parameters	Symmetric
No. of DC sources	n
No. of switches	2n+4
No. of output levels	2n+1
Maximum voltage	$nV_{de}$

A symmetric semi-cascaded model is designed in MATLAB which comprises of 13 input voltage sources each of 20V and 30 switches. The figure below represents the semi-cascaded inverter.

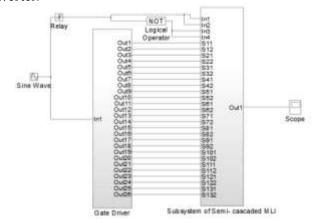
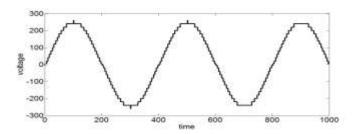


Fig-9: Simulink model of semi-cascaded H-bridge inverter

The 27 level semi-cascaded model consists of one H-bridge comprising of four switches and 13 input voltage sources, each of them connected to two switches with a total of 30 switches.

**Table-7**: Switching scheme for 27 level semi-cascaded Hbridge MLI

	In1&I	In3&I													
LV	n2	n4	S1	S2	S3	S4	S5	S6	<b>S7</b>	S8	S9	S10	S11	S12	S13
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	٠.
2	1	0	1	1	1	1	1	1	1	1	1	1	1	1	C
3	1	0	1	1	1	1	1	1	1	1	1	1	1	0	•
4	1	0	1	1	1	1	1	1	1	1	1	1	0	0	·
5	1	0	1	1	1	1	1	1	1	1	1	0	0	0	·
6	1	0	1	1	1	1	1	1	1	1	0	0	0	0	•
7	1	0	1	1	1	1	1	1	1	0	0	0	0	0	•
8	1	0	1	1	1	1	1	1	0	0	0	0	0	0	Ī
9	1	0	1	1	1	1	1	0	0	0	0	0	0	0	
10	1	0	1	1	1	1	0	0	0	0	0	0	0	0	
11	1	0	1	1	1	0	0	0	0	0	0	0	0	0	
12	1	0	1	1	0	0	0	0	0	0	0	0	0	0	
13	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
14	0	00	0	0	0	0	0	0	0	0	0	0	0	0	
15	0	1	1	0	0	0	0	0	0	0	0	0	0	0	Ī
16	0	1	1	1	0	0	0	0	0	0	0	0	0	0	Ī
17	0	1	1	1	1	0	0	0	0	0	0	0	0	0	Ī
18	0	1	1	1	1	1	0	0	0	0	0	0	0	0	Ī
19	0	1	1	1	1	1	1	0	0	0	0	0	0	0	Ī
20	0	1	1	1	1	1	1	1	0	0	0	0	0	0	Ī
21	0	1	1	1	1	1	1	1	1	0	0	0	0	0	Ī
22	0	1	1	1	1	1	1	1	1	1	0	0	0	0	Ī
23	0	1	1	1	1	1	1	1	1	1	1	0	0	0	Ī
24	0	1	1	1	1	1	1	1	1	1	1	1	0	0	Ī
25	0	1	1	1	1	1	1	1	1	1	1	1	1	0	Ī
26	0	1	1	1	1	1	1	1	1	1	1	1	1	1	Ī
27	0	1	1	1	1	1	1	1	1	1	1	1	1	1	



**Fig-10**: Output waveform of 27 level semi-cascaded H-Bridge MLI

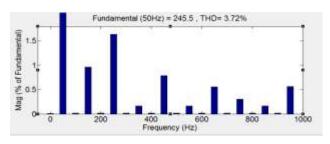


Fig-11: THD (3.72%) of 27 level semi-cascaded H-bridge MLI

It can be observed from the switching pattern that the frequency of switching of the switches is much lesser as compared to the previously discussed schemes. As a result, in this scheme, the switches experience lesser stress and hence the life of the device gets extended. The inverter produces a maximum voltage of  $13V_{\rm dc}$  with THD of 3.72% which is almost same as the 27-level asymmetric CHB-MLI. But the complexity of the circuit increases as it uses more number of voltage sources and switches. To avoid these limitations, a novel approach has been taken.

#### 4. SIMULATION WORK OF THE NOVEL HYBRID MLI

A novel hybrid inverter is so modeled that it produces more number of levels only with a few switches to eliminate the issue of complexity in configuration. The number of levels can be calculated as:

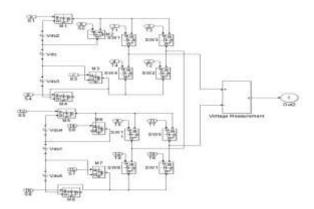
No. of levels= 
$$(2n+1)^m$$

where 'n' is the number of non-isolated voltage source in each sub multi level cell and 'm' is the number of sub multi level cells.

The DC input voltages can be calculated as:  $V_{dc}(k) = (2n+1)^{k-1}.V_{dc}$ 

where k= 1,2,3,....

The proposed inverter is modeled using two sub multi-level cells each comprising of three input voltages. The circuit configuration is accomplished using only sixteen switches. The number of levels produced by this hybrid inverter is forty-nine with a maximum output voltage of  $24V_{\rm dc}. \label{eq:voltage}$ 



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**Fig-12**: Simulation model of the proposed inverter

The switching scheme of the inverter is tabulated in table 8

Table-8: Switching scheme of 49 level hybrid inverter

LEVELS	<b>S1</b>	<b>S2</b>	S3	S4	S5	S6	<b>S</b> 7	S8	T1	T2	Т3	T4	T5	Т6	T7	Т8
1	1	0	33 0	34 1	35 1	0	0	36 1	1	1	0	0	1	1	0	0
2	0	1	0	1	1	0	0	1	1	1	0	0	1	1	0	0
3	0	1	1	0	1	0	0	1	1	1	0	0	1	1	0	0
4	<del>  0</del>	<del> </del>	<u></u>	0	1	H 0	-	1	0	1	0	1	1	1	<del> </del> 0	0
5	<del> </del> 0	1	1	o	1	0	0	1	0	0	1	1	1	1	0	0
6	0	1	ō	1	1	0	o	1	o	o	1	1	1	1	0	0
7	1	0	0	1	1	0	0	1	ō	0	1	1	1	1	0	0
8	1	0	О	1	1	0	1	О	1	1	О	О	1	1	О	0
9	0	1	0	1	1	0	1	0	1	1	0	0	1	1	0	0
10	0	1	1	О	1	0	1	0	1	1	О	О	1	1	0	0
11	0	0	0	0	1	0	1	0	0	1	0	1	1	1	0	0
12	0	1	1	0	1	0	1	0	0	0	1	1	1	1	0	0
13	0	1	0	1	1	0	1	0	0	0	1	1	1	1	0	0
14	1	0	0	1	1	0	1	0	0	0	1	1	1	1	0	0
15	1	0	0	1	0	1	1	0	1	1	0	0	1	1	0	0
16	0	1	0	1	0	1	1	0	1	1	0	0	1	1	0	0
17	0	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0
18	0	0	0	0	0	1	1	0	0	1	0	1	1	1	0	0
19	0	1	1	0	0	1	1	0	0	0	1	1	1	1	0	0
20	0	1	0	1	0	1	1	0	0	0	1	1	1	1	0	0
21	1	0	0	1	0	1	1	0	0	0	1	1	1	1	0	0
22	1	0	0	1	0	0	0	0	1	1	0	0	0	1	0	1
23	0	1	0	1	0	0	0	0	1	1	0	0	0	1	0	1
24	0	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1
25	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
26	0	1	1	0	0	0	0	0	0	0	1	1	0	1	0	1
27	0	1	0	1	0	0	0	0	0	0	1	1	0	1	0	1
28	1	0	0	1	0	0	0	0	0	0	1	1	0	1	0	1
29	1	0	0	1	0	1	1	0	1	1	0	0	0	0	1	1
30	0	1	0	1	0	1	1	0	1	1	0	0	0	0	1	1
31	0	1	1	0	0	1	1	0	1	1	0	0	0	0	1	1
32	0	0	0	0	0	1	1	0	0	1	0	1	0	0	1	1
33	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1
34	0	1	0	1	0	1	1	0	О	0	1	1	О	0	1	1
35	1	0	0	1	0	1	1	0	О	0	1	1	О	0	1	1
36	1	0	0	1	1	0	1	0	1	1	0	0	0	0	1	1
37	0	1	0	1	1	0	1	0	1	1	ō	0	0	0	1	1
38	0	1	1	0	1	0	1	0	1	1	0	0	0	0	1	1
39	0	0	0	0	1	0	1	0	0	1	0	1	0	0	1	1
40	0	1	1	0	1	0	1	0	0	0	1	1	0	0	1	1
41	6	1	0	1	1	6	1	0	0	0	1	1	0	0	1	1
41	1	<u></u>	0	1	1	0	1	0	0	0	1	1	0	0	1	1
43	1	0	0	1	1	0	0	1	1	1	0	0	0	0	1	1
43	0	1	0	1	1	0	0	1	1	1	0	0	0	0	1	1
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
45	0	1	1	0	1	0	0	1	1	1	0	0	0	0	1	1
46	0	0	0	0	1	0	0	1	0	1	0	1	0	0	1	1
47	0	1	1	0	1	0	0	1	0	0	1	1	0	0	1	1
48	0	1	0	1	1	0	0	1	0	0	1	1	0	0	1	1
49	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1

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### 5. SIMULATION RESULTS OF THE PROPOSED INVERTER

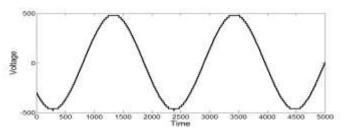


Fig-13: Output voltage waveform of 49 level MLI

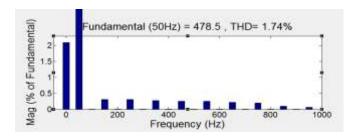


Fig-14: THD (1.74%) of 49 level hybrid inverter

From the above figures it is observed that the new proposed inverter produces forty nine levels only with sixteen switches. Moreover, the THD is found to be less which is about 1.74 %.

#### 6. CONCLUSION

The proposed inverter scheme uses lesser number of switches while it produces larger number of voltage levels as compared to other MLIs discussed. Also the total harmonic distortion has been found to be much lesser than others. The research work claims that by using this type of MLIs the stress on the inverter switches can be reduced and hence the lifetime of the semiconductor switches increase. Therefore, these types of inverters can be very economical and sustainable.

#### REFERENCES

- [1] Dr. Asha Gaikwad and Pallavi Apasso Arbune, "Study of Cascaded H-Bridge Multilevel Inverter," 2016 International Conference on Automatic Control and Dynamic Optimization Techniques (ICACDOT)International Institute of Information Technology (I<sup>2</sup>IT), Pune.
- [2] Prabaharan .N, Hina Fathima .A and Palanisamy .K, "New Hybrid Multilevel Inverter With Reduced Switch Count Using Carrier Based Pulse Width Modulation Technique," 2015 IEEE Conference on Energy Conversion (CENCON).
- [3] Aparna Prayag and Sanjay Bodhke, "A comparative study of symmetrical and asymmetrical cascaded H-Bridge Multilevel Inverter Topology for Industrial Drive,"

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e-ISSN: 2395-0056

- [4] Y. Suresh, J. Venkataramanaiah, Anup kumar Panda, C. Dhanamjayulu and P. Venugopal, "Investigation on cascade multilevel inverter with symmetric, asymmetric, hybrid and multi-cell configuration," Ain Shams Engineering Journal Volume 8, Issue 2, June 2017.
- [5] Thirumalai.M and Prakash.V, "Design and Implementation of Hybrid Multilevel Inverter for High Output Frequency," 2013 International Conference on Smart Structures & Systems (JCSSS-20 13), March 28 29, 2013, Chennai, INDIA.
- [6] Ebrahim Babaei and Seyed Hossein Hosseini, "New Cascaded multilevel topology with minimum number of switches," Energy Conversion and Management Volume 50, Issue 11, November 2009.