International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 04 | Apr 2019 www.irjet.net p-ISSN: 2395-0072

VLSI Architecture for Reversible Radix-2 FFT Algorithm using Programmable Reversible Gate

Deepnarayan Choudhary[1], Prof. Suresh S. Gawande[2], Prof. Satyarth Tiwari[3]

[1]*Research scholar, Electronics & Communication Department, Bhabha Engineering Research Institute, Bhopal*
[2,3]*Professor, Electronics & Communication Department, Bhabha Engineering Research Institute, Bhopal*

Abstract - *The Discrete Fourier Transform (DFT) is a critical procedure in the field of Digital Signal Processing (DSP) and Telecommunications, particularly for applications in Orthogonal Frequency Division Multiplexing (OFDM) frameworks. The Fast Fourier Transform (FFT) is an effective calculation to process the DFT and its reverse. The FFT processor assumes a key job in the field of correspondence frameworks, for example, Digital Video or Audio Broadcasting, Wireless LAN with Standards of IEEE 802.11, High Speed Digital Subscriber Lines and so forth. In this paper includes the execution of a zone proficient 8-point, 16-point and 32-point radix-2 DIT FFT calculation with the assistance of DKG reversible Gate. Two strategies are utilized to plan radix-2 FFT calculation. In firest strategy is plan radix-2 FFT with the help of reversible Peres gate and TR gate. Second method is design radix-2 FFT with the help of reversible DKG Gate. The all structure are usage vertex-4 gadget family Xilinx programming and looked at past calculation.*

Key Words: FFT, Reversible Gate, DKG Gate, Peres Gate, TR Gate

1. INTRODUCTION

The Fourier Transform is an inescapable methodology in flag handling, especially for applications in OFDM frameworks [1]. The Discrete Fourier Transform decays a lot of qualities into various segments of recurrence. The FFT is a fitting strategy to do control of DFT. The calculation of FFT was concocted by Cooley and Tukey so as to diminish the measure of multifaceted nature as for time and calculations [2].

The equipment of FFT can be executed by two sorts of groupings memory design and pipeline engineering. The memory engineering contains a solitary handling component and different units of memory [3]. The benefits of memory design incorporate low power and minimal effort when contrasted with that of different styles. The explicit bad marks are more noteworthy idleness and lower throughput. The above bad marks of the memory engineering are completely killed by pipeline design to the detriment of additional equipment in a satisfactory way. The different sorts of pipeline engineering incorporate Single defer criticism (SDF), Single postpone commutator (SDC) and various postpone commutator (MDC). The pipeline engineering is an ordinary structure which can be embraced by utilizing equipment portrayal dialect in a simple way. In the ongoing years, the correspondence frameworks need to transmit voice and video signs of high caliber in a productive way. In present day the effective module is a rapid, solid innovation of correspondence [4].

Symmetrical OFDM is such a solid choice to achieve the above necessity. The calculations of FFT can be gathered into settled radix, blended radix and split radix calculations in an unpleasant way [5]. The essential classes of calculations of FFT incorporate - Decimation in-frequency (DIF) and the Decimation-in-time (DIT) as appeared in Figure 1. Both of these calculations rely upon crumbling of change of a N-point grouping into numerous subsequences in a progressive way. There is no real distinction between them to the extent intricacy of calculation is concerned. For the most part DIT manages the info and yield backward arrangement and ordinary grouping separately, while DIF manages information and yield in typical succession and turn around arrangement individually. Just DIT calculation will be contemplated.

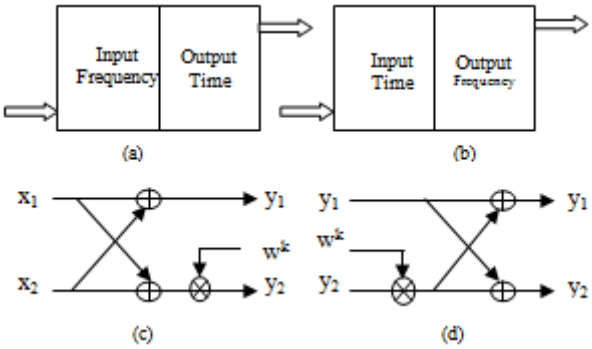

Fig -1: Time and frequency signal

2. FAST FOURIER TRANSFORM

There are two sorts concerning FFT calculation formulated by Cooley and Tukey - Decimation-in-Time calculation (DIT) and Decimation-in-Frequency calculation (DIF). The calculation of an arrangement of N-point can be acquired by methods for a double methodology. The info succession x(n) of size 'N' is disintegrated into tests of odd and even and the comparing sub-groupings f1(n) and f2(n) are given by:

$$f_1(n) = x(2n) \quad (1)$$

$$f_1(n) = x(2n+1),\ n = 0,1 \ldots\ldots\ldots \frac{N}{2} - 1 \quad (2)$$

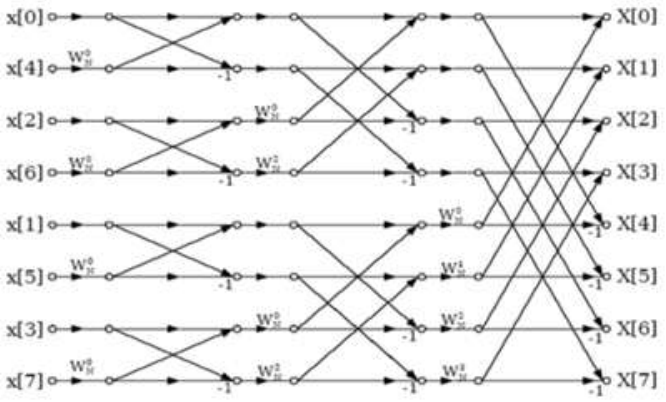

Fig -2: 8-point DIT-FFT Radix-2 Butterfly

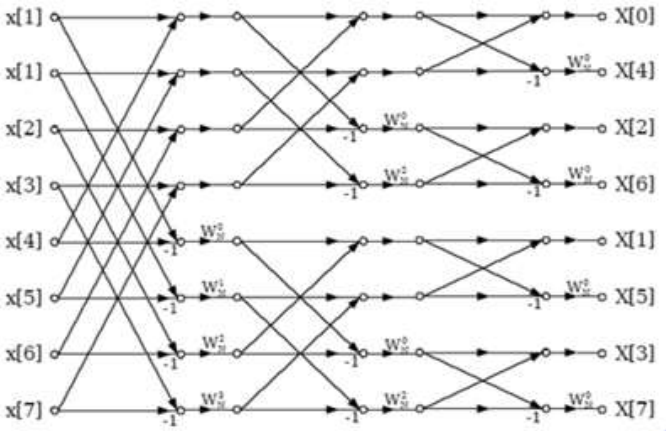

Fig -3: 8-point DIF-FFT Radix-2 Butterfly

In figure 2, demonstrate the butterfly of radix-2 DIT FFT calculation. In this figure we utilized eight sources of info and eight yields. If there should be an occurrence of DIT the info test is utilized piece inversion arrange while the yield of DIT FFT coefficients is produced in normal request. In Figure 3, demonstrate the butterfly of radix-2 DIF FFT calculation. In the event of DIF the information test is utilized in common request while the yield of DIF FFT coefficient is produced in bit turned around request.

3. REVERSIBLE GATE

Several reversible logic gate (RLG) are utilized in past structure. Figure 4 demonstrates the Peres door (PG). A bit of the 3x3 entryways are planned for executing some basic combinational limits despite the basic limits.

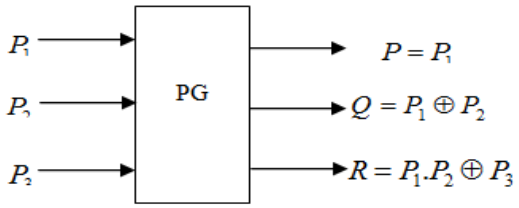

Fig -4: Block Diagram of PG

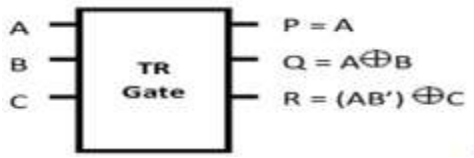

Fig -5: Block Diagram of TRG

Figure 5, shows the TRG with 3×3 system. TRG gate as working of half sub-tractor, when third input assume '0'. The RDKG is presented by figure 6. RDKG is 4×4 system representation. RDKG is working on full adder and full sub-tractor when first input assumes '0' and '1'.

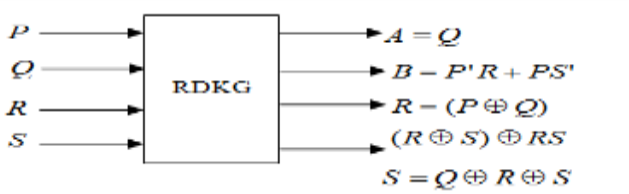

Fig -6: DKG Gate

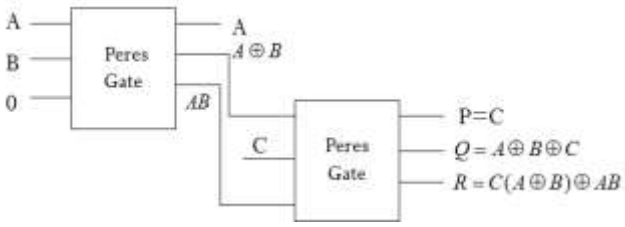

Fig -7: Block Diagram of 1-bit Full Adder

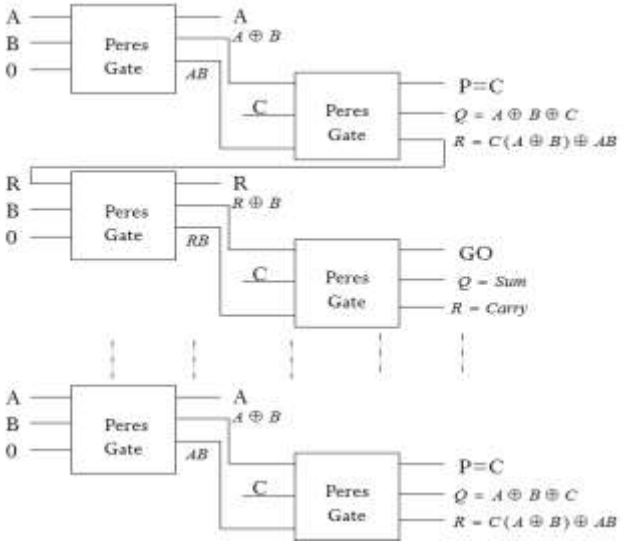

Fig -8: Block Diagram of n-bit Full Adder

4. PROPOSED METHODOLOGY

The expense and defer figurings are indistinguishable to the 4-bitb snake/sub tractor in figure 9. We have design 4-bit

full sub-tractor/adder with the help of DKG Gate. If the fourth input of the DKG Gate is '0' then output of the DKG Gate as a adder and fourth input of the DKG Gate is '1' then output of the DKG Gate as a sub-tractor.

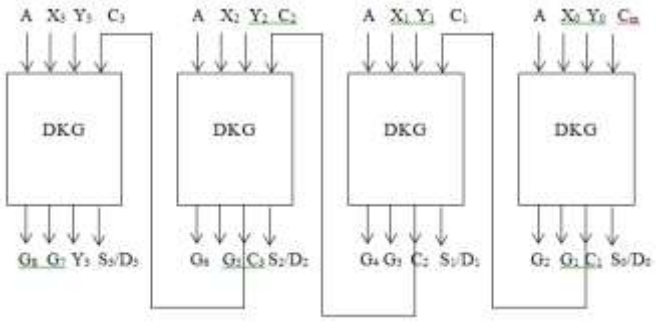

Fig -9: Reversible 4-bit Adder/ Sub tractor using DKG Gate

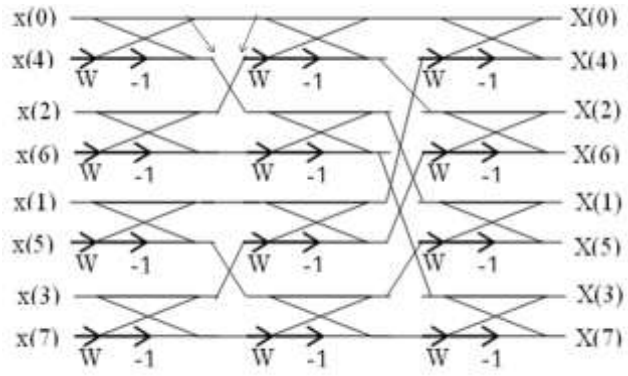

Fig -10: Proposed DIT Radix-2 FFT algorithm using Radix-2 Butterfly

Example of 8-point FFT

Then the 8-point FFT can be rewritten as

$$X(0) = h_0 + Wh_1$$
$$X(1) = h_0 - Wh_1$$
$$X(2) = h_2 + Wh_3$$
$$X(3) = h_2 - Wh_3$$
$$X(4) = h_4 + Wh_5$$
$$X(5) = h_4 - Wh_5$$
$$X(6) = h_6 + Wh_7$$
$$X(7) = h_6 - Wh_7$$

Where

$$h_0 = g_0 + Wg_1$$
$$h_1 = g_0 - Wg_1$$
$$h_2 = g_2 + Wg_3$$
$$h_3 = g_2 - Wg_3$$
$$h_4 = g_4 + Wg_5$$
$$h_5 = g_4 - Wg_5$$
$$h_6 = g_6 + Wg_7$$
$$h_7 = g_6 - Wg_7$$

Where

$$g_0 = x(0) + Wx(4)$$
$$g_1 = x(0) - Wx(4)$$
$$g_2 = x(2) + Wx(6)$$
$$g_3 = x(2) - Wx(6)$$
$$g_4 = x(1) + Wx(5)$$
$$g_5 = x(1) - Wx(5)$$
$$g_6 = x(3) + Wx(7)$$
$$g_7 = x(3) - Wx(7)$$

In the modified equation in second stage

$$k_n = g_n \pm Wg_{n+2} \quad for\ n = 1$$
$$k_{n+1} = g_n \pm Wg_{n+2} \quad for\ n = 2$$
$$k_{n+2} = g_{n+2} \pm Wg_{n+4} \quad for\ n = 3$$
$$k_{n+3} = g_{n+2} \pm Wg_{n+4} \quad for\ n = 4$$

And third stage

$$X_n = k_n \pm Wk_{n+4} \quad for\ n = 1$$
$$X_n = k_n \pm Wk_{n+4} \quad for\ n = 2$$
$$X_n = k_n \pm Wk_{n+4} \quad for\ n = 3$$
$$X_n = k_n \pm Wk_{n+4} \quad for\ n = 4$$

A fast Fourier transform (FFT) is an algorithm that computes the discrete Fourier transform (DFT) of a sequence, or its inverse (IDFT). Fourier analysis converts a signal from its original domain (often time or space) to a representation in the frequency domain and vice versa. The DFT is obtained by decomposing a sequence of values into components of different frequencies. This operation is useful in many fields, but computing it directly from the definition is often too slow to be practical. An FFT rapidly computes such transformations by factorizing the DFT matrix into a product of sparse (mostly zero) factors. The difference in speed can be enormous, especially for long data sets where *N* may be in the thousands or millions. In the presence of round-off error, many FFT algorithms are much more accurate than evaluating the DFT definition directly.

5. SIMULATION RESULT

The reproduction results for different FFT calculations have been tried basically by executing in the Vertex-4 Xilinx programming. Additionally these product yields can be confirmed with reproduction results got utilizing MODELSIM. A portion of the previews of results in the Xilinx programming and reenactment are as per the following

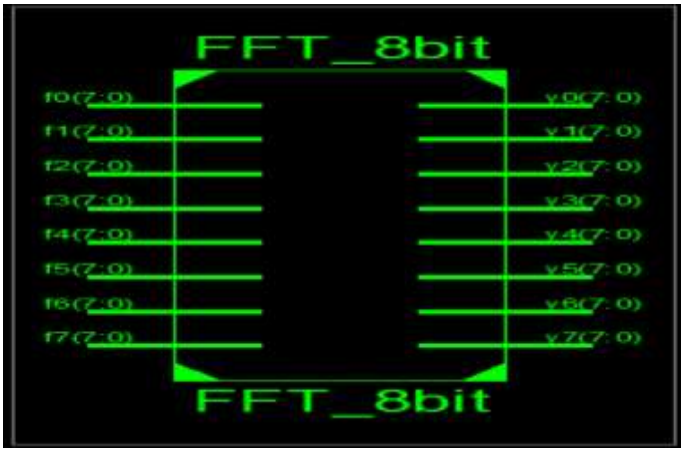

Fig -11: View Technology Schematic of 8-point DIT-FFT algorithm

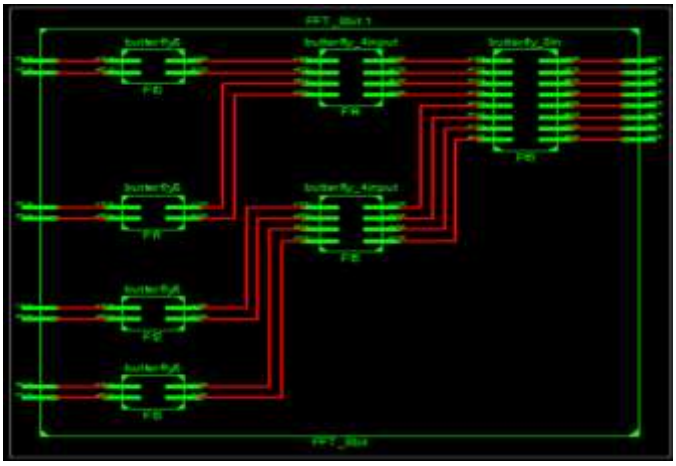

Fig -12: RTL View of DIT 8-point DIT-FFT algorithm

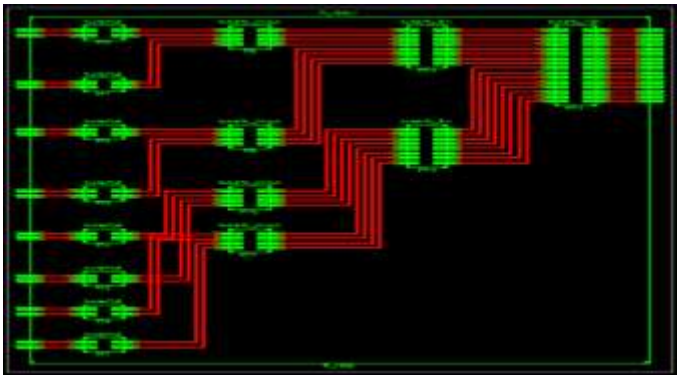

Fig -13: RTL View of 16-point DIT-FFT algorithm

6. CONCLUSIONS

FFT is an often utilized DSP calculation for the utilizations of OFDM. The blend of OFDM with Multiple Input Multiple Output (MIMO) flag handling is a distinct methodology of upgrading the information rates of different correspondence frameworks, for example, Wireless LAN, e Mobile, 4G and so forth.

The discrete Fourier transform (DFT) is one of the most powerful tools in digital signal processing. The DFT enables us to conveniently analyze and design systems in frequency domain; however, part of the versatility of the DFT arises from the fact that there are efficient algorithms to calculate the DFT of a sequence. A class of these algorithms are called the Fast Fourier Transform (FFT). This article will, first, review the computational complexity of directly calculating the DFT and, then, it will discuss how a class of FFT algorithms, i.e., decimation in time FFT algorithms, significantly reduces the number of calculations.

REFERENCES

[1] Shashidhara. K. S and H.C. Srinivasaiah, "Low Power and Area efficient FFT architecture through decomposition technique", International Conference on Computer Communication and Informatics (ICCCI -2017), Jan. 05 – 07, 2017, Coimbatore, INDIA.

[2] Fahad Qureshi, Jarmo Takala, Anastasia Volkova, Thibault Hilaire, "Multiplierless Unified Architecture for Mixed Radix-2/3/4 FFTs", 2017 25th European Signal Processing Conference (EUSIPCO), IEEE 2017.

[3] Fahad Qureshi, Muazam Ali, and Jarmo Takala, "Multiplierless Reconfigurable Processing Element for Mixed Radix-2/3/4/5 FFTs", 978-1-5386-0446-5/17/$31.00 ©2017 IEEE.

[4] Ms. A. Anjana and Mrs. A.V Ananthalakshmi, "Design of Reversible 32-Bit BCD Add-Subtract Unit using Parallel Pipelined Method", International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB16) 978-1-4673-9745-2 ©2016 IEEE.

[5] Matthew Morrison and Nagarajan Ranganathan, "Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures", 2015 IEEE Computer Society Annual Symposium on VLSI.

[6] Lekshmi Viswanath and Ponni.M, "Design and Analysis of 16 Bit Reversible ALU", ISSN: 2278-0661 Volume 1, Issue 1 (May-June 2014), PP 46-53.

[7] Akanksha Dixit and VinodKapse, "Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit", International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2014.

[8] Mr. Abhishek Gupta, Mr. UtsavMalviya and Prof. VinodKapse, "Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors", 2012 IEEE Computer Society Annual Symposium on VLSI.

[9] H. Thapliyal and N. Ranganathan, "Design of Efficient Reversible Binary Subtractors Based on A New Reversible Gate," Proc. of the I ComputerSociety Annual Symposium on VLSI, 2009.

[10] M. Morrison and N. Ranganathan, "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," IEEE International Symposium on VLSI, 2011, pp. 126-131.