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Design of an Inductive Source Degenarative Low Noise Amplifier using 180nm CMOS Technology

M. Kiran Kumar[1], Amrita Sajja[2], Katti Blessy Beulah[3] ,K. Sree Deepthi [4], Ravalika D[5]

[1,2]Assistant Professor, Dept. of ECE Anurag Group Of Institutions,Hyderabad
[3,4,5]Research scholar & Anurag Group Of Institutions, Hyderabad

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Abstract - *In this paper attributes a design of cascaded narrowband low noise amplifier (LNA) operated at 2.4GHz using inductive source degeneration with a shunt connected inductor and resistance transformer matching. This design implementing with CMOS transistor from gpdk180nm technology. By introducing inductive source degeneration will degrade the gain while improving the stability and maintaining the noise figure of the overall system. With shunt connected transformer provides narrow band characteristic and good input and output return loss on the desired frequency band. The LNA achieves input and output return loss of less than -20 dB, gain 25dB and noise figure less than 0.6dB respectively.*

Key Words: Source degeneration, noise figure, low noise amplifier, common gate, CMOS

1.INTRODUCTION

In the receiver front end, Low Noise Amplifier is the main component. UWB technology gives the capability to deliver and collect message in a widespread frequency spectrum, segmented into the lower frequency (3-5 GHz) and the upper-frequency band (6-10.6 GHz)[1-3]. The main advantages of UWB network are its ability to transmit digital signals in high data rate with low power consumption, low complicacy, and high immunity. Low noise figure and high gain of amplifying weak input RF signal, low chip area, high stability, low power consumption, high linearity are maintained by LNA[2]. Capacitor cross-coupled is the enhancement of CG LNA. Based on the noise performance and input matching network characteristics common source, common gate LNA. The high quality factor of their input matching network at a resonance frequency, while this later should decrease to assuage the UWB matching requirements in terms of bandwidth is the main disadvantage in CS LNA's.

Inductive source degeneration method undergoes from the high noise figure and is suitable for narrowband applications and current reuse approach occupies a large chip area. Shunt series feedback technique needs high power consumption and creates a higher noise figure[3-5]. Due of parallel resonant network and knowing that the gate to source capacitance is proportional to transistor size, a quality factor of input matching network of CG LNA would decrease when the technology should be scaled down and bandwidth shows wideband demeanor. So CG LNA has a constant wideband input impedance matching without using additional components while preserving area consumption and avoiding from more resistance losses of on-chip inductors. In extension, the CG-LNA has more linearity and stability performance, low power consumption, better input-output isolation, more immunity to PVT variations by providing a simple input match network with a wide bandwidth[6-8].

2. DESIGN METHODOLOGY

In this paper inductively degenerated common source CMOS LNA topology is developed. The circuit design is carried out while deriving source inductor L_s so that the simultaneous gain and input matching can be achieved at any amount of power. The design starts with the selection of proper W value of circuit input impedance close to the value of noise input impedance. This is in order to get the NF that is close to NFmin. Fig.1 shows the design methodology of the LNA described above.

Once the W has been determined, the transconductance of gm and the gate-source capacitance Cgs can be calculated by setting the bias current and the gate voltages. V_ds (sat) must be above the difference between threshold voltage and gate to source voltage to maintain the proper bias current. All the transistors should be in the saturation region. If V_ds (sat) goes down for the same Ibias; then the transconductance value goes down. If we increase device size bigger and bigger than the transonductance will increase; device size also relates to linearity; if the device is in weak inversion region it's not good for linearity.

$$(W/L)_{in} = \frac{2I}{k_w(V_{ds}{}^2(sat))}$$

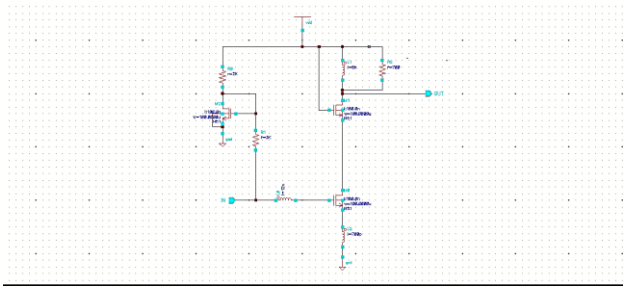

Fig -1: Proposed LNA with Current Mirror

Table.1 Comparison of different LNA Topologies

Characteristic	Common source	Cmmon Gate	Cascode
Noise Figure	Lowest	Rises rapidly with frequency	Slightly higher han CS
Gain	Moderate	Lowest	Highest
Linearity	Moderate	High	Potentially Highest
Bandwidth	Narrow	Fairly Broad	Broad
Stability	Required compensation	Higher	Higher

2.1 Small Signal Analysis of LNA:

The equivalent circuit of the CS LNA is as shown in the Fig.2

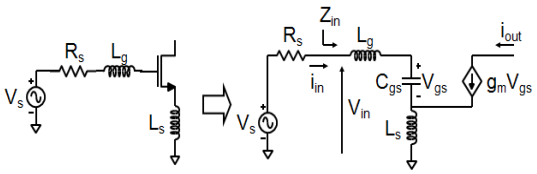

Fig. 2 Equivalent Circuit of LNA

2.1.1 Analysis of Noise Figure:

Noise Figure is a critical parameter of the LNA. The noise figure is a measure of signal to noise ratio degradation when the signal transfer from transmitter to receiver. The expression(2) of the Noise Figure is as shown below. The following expression is derived from the concept of overall transconductance of the LNA.

$$NF\big|_{\omega\approx\omega_0} = \frac{N_{device} + G\cdot N_{in}}{G\cdot N_{in}} \qquad (2)$$

Where G is the total transconductane of the LNA, it can be obtained while applying KVL around the equivalent circuit

$$V_{in} = I_{in}sL_g + I_{in}\frac{1}{sC_{gs}} + (I_{in} + g_m V_{gs})sL_s$$

$$= I_{in}sL_g + I_{in}\frac{1}{sC_{gs}} + (I_{in} + g_m I_{in}\frac{1}{sC_{gs}})sL_s$$

$$= I_{in}\left[s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}\right]$$

Then the Fig.2 can be modified with the above equation as shown in Fig.3

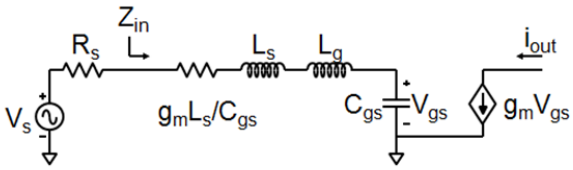

Fig.3 Modified Equivalent Circuit of LNA

Where input impedance is

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}$$

- $Z_{in} = R_s$
  - $IM\{Z_{in}\} = 0$
  - $RE\{Z_{in}\} = R_s$

$$\omega_0^2 = \frac{1}{(L_g + L_s)C_{gs}}$$

$$\frac{g_m L_s}{C_{gs}} = R_s$$

$$G_{eff} = \frac{I_{out}}{V_s} = \frac{g_m/(sC_{gs})}{R_s + Z_{in}}$$

$$= \frac{g_m}{1 + s(R_s C_{gs} + g_m L_s) + s^2 C_{gs}(L_g + L_s)}$$

$$G = \left|G_{eff}\right|^2 = \frac{g_m^2}{[1-\omega^2 C_{gs}(L_g + L_s)]^2 + \omega^2(R_s C_{gs} + g_m L_s)^2} \qquad (3)$$

2.1.2 Gain Analysis:

As we discussed in the previous section LNA is a front end amplifier in the receiver section. So there it required minimum amplification required to process further. As we are concentrating more on linearity and noise figure while maintaining minimum gain. So for finding overall gain in the LNA by considering the equivalent circuit of cascode LNA is as shown in the Fig. 4

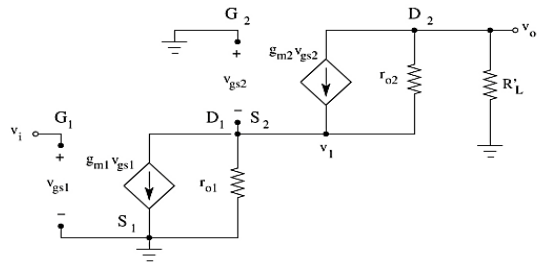

Fig.4 Equivalent Circuit of cascaded LNA

$$A_v \approx -g_{m1}(r_{O1} \parallel R_{L1})g_{m2}(r_{O2} \parallel R_{out})$$

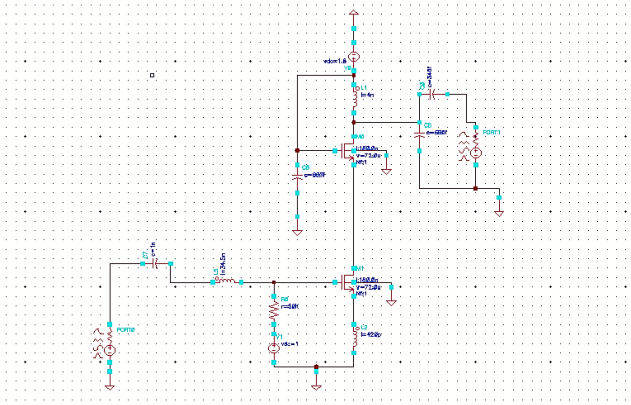

Fig.5 Capacitor Coupled CS LNA

Noise performance is enhanced by Capacitor Coupled (CC) technique, which is shown in the Fig.5 and it also degrades power consumption. But this technique will decline the CS-LNA's linearity, this problem is also seen in conventional gm-boosting technique also.

However, the power consumption will increase dramatically. By increasing the overdriving voltage we can improve an interesting characteristic of MOS transistors, Yet the power consumption will increase dramatically. When the transistor is biased from weak inversion region to strong inversion region, the g_m switches from positive to negative, this is an interesting characteristic of MOS transistors.

3. SIMULATION RESULTS

In the design of source degenerative CS LNA, the simulation was carried out using UMC180nm CMOS Technology.

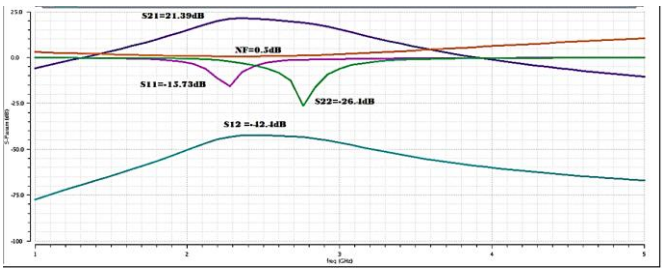

Fig.6 S-Parameter result of CS LNA

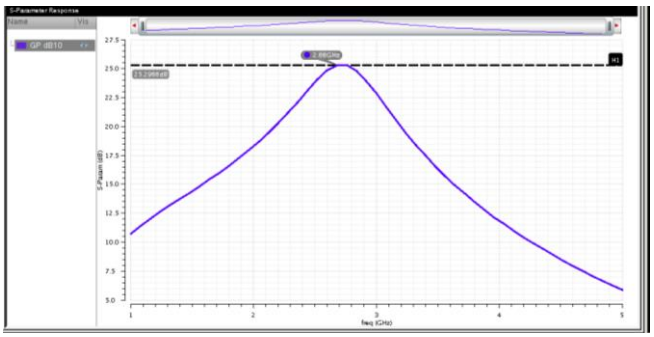

Fig.7 Power gain of CS LNA

Fig.6 shows S-parameters result of differential CMOS LNA. The LNA achieved a voltage gain of 21.39dB and the noise figure, NF is 0.5 dB. The input return loss, S11 is -15.73 dB and output return loss is -26.44dB. The attained value of NF is believed to be good as it exceeds the requirement which is typically below 1 dB without having to trade off the power gain which also satisfies the requirement.

This show that the designed LNA is able to achieve good noise and gain performance without sacrificing it's linearity. The LNA is supplied from 1.8V and consumed about 2.88 m W of power

4. CONCLUSION

A Source degenerated CS CMOS LNA is presented using UMC180nm technology and has been designed for 2.4GHz applications. The LNA operated with 1.8V power supply. The system Noise Figure of 0.5dB and power gain of 25.2dB as shown in Fig.7. The total power consumption is 2.88mW.

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