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Analysis of Proposed FinFET Based Full Adder using CMOS Logic Style

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Abstract - *With the innovation in technology, FinFETs are the new emerging transistors that can work in the nanometer range to overcome Short Channel Effects (SCE) as conventional CMOS has Short Channel Effects. The logic styles used for implementation are Gate Diffusion Input (GDI) and Static Energy Recovery Full (SERF) Adder. To improve the Full Adder architecture many improvements has been made. Hence, in order to reduce the Short Channel Effects, FinFET based Full Adder has proposed. The experiment designs are implemented in CADENCE VIRTUOSO software using 180nm technology GPDK tool kit and performance analyses were done with respect to Power, Delay and Power Delay Product (PDP). Here FinFET Based GDI Adder and FinFET Based SERF Adder results in less switching activity and area due to less number of transistors i.e. 10. The result shows that the power of FinFET SERF Adder is reduced to 58.86 % compared to FinFET GDI Full Adder. The Delay of FinFET SERF Adder is reduced to 24.98% compared to FinFET GDI Full Adder. The PDP of FinFET SERF Adder has reduced to 69.14% compared to FinFET GDI Full Adder. It is evident that the FinFET based SERF Adder using CMOS Logic Style helpful in digital application in respect of portable, reliable, energy efficient, consume low power and perform high speed.*

Key Words: **FinFET, Full Adder, GDI, SERF**

1. INTRODUCTION

Now a day, modern digital devices are of a great demand in many industrial applications because these devices are portable, reliable, energy efficient, consume low power and perform high speed. The most important feature of modern electronics is low power and energy efficient active block that enables the implementation of long lasting battery operated devices.

FinFETs are the new emerging transistors that can work in the nanometer range to overcome these Short Channel Effects and low power FinFET based Full Adder implemented by using CADENCE VIRTUOSO tools in 45nm technology [1]. Study of different full adder cells with two logic styles i.e. FinFET Based one bit Full Adder Cell using Transmission Gate (TG) and CMOS Logic Styles At 10, 22 and 32nm[2]. Moore's Law: Gordon Moore: co-founder of Intel. Predicted that the number of transistors per chip would grow exponentially [3]. He has set the pace for our modern digital revolution and utilized that the computing world increases in power and decreases in cost.
Ultra Low Power Based one bit Full Adder using different Nanometer Technologies and simulations were done at 45nm, 32nm technologies. [4]

Binary addition is the basic operation found in most arithmetic components. Computation needs to be achieved by using area efficient circuits operating at high speed with low power consumption. Addition is the fundamental arithmetic operation and most fundamental arithmetic component of the processor is adder. A full adder is a logical circuit that performs an addition operation on three one-bit binary numbers. Complementary Metal-Oxide-Semiconductor (CMOS) is a technology for constructing integrated circuits. To improve the Full Adder architecture many improvements has been made by researchers.

Full adders are fundamental cell in various circuits which is used to perform arithmetic operations and the VLSI design can be addressed at various design levels. *Conventional CMOS has Short Channel Effects* and difficult in implementation, thereby market demand retarding day by day. Hence, in order to reduce the Short Channel Effects, FinFET based Full Adder using CMOS logic style has been proposed. In this study, The logic styles used for implementation are Gate Diffusion Input (GDI) and Static Energy Recovery Full (SERF) Adder. The experiment designs are implemented in CADENCE VIRTUOSO software using 180nm technology GPDK tool kit and performance analyses were done with respect to Power, Delay and Power Delay Product (PDP).

2. CMOS LOGIC STYLES

2.1 Gate Diffusion Input Operation

Gate Diffusion Input (GDI) is nothing but Gate Diffusion Input Technique. This type of technique is suitable for lower delay and designing a circuit with reduced power. This is because the technique helps to decrease the transistor count when compared with CMOS and other obtainable low power methods. [1]

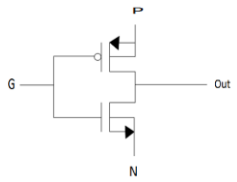

Fig-1: Basic GDI Cell [Ref 1]

GDI Cell method is based on the use of a simple cell as shown in Figure [1]. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences:

Gate Diffusion Input CELL) contains three inputs –

G (common gate input of NMOS and PMOS)

P (input to the source/drain of PMOS)

N (input to the source/drain of NMOS)

Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter.

This design can implement a wide variety of logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors, while improving logic level swing and static power characteristics and allowing simple top down design by using small cell library.

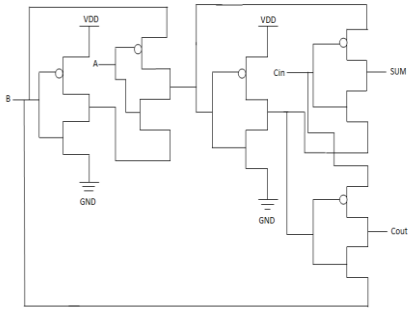

Fig- 2: GDI CMOS Full Adder [Ref 1]

GDI full adder contains three input pins A, B and Cin and two output pins sum and Cout. It is built from two XOR gates and one MUX.

2.2 Static Energy Recovery Full Adder (SERF)

As an initial step toward designing low power arithmetic circuit modules, we designed a Static Energy Recovery Full (SERF) adder cell module illustrated in Figure.3

The implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delays at the output of these gates. This leads to less spurious SUM and Carry signal. The energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. [6]

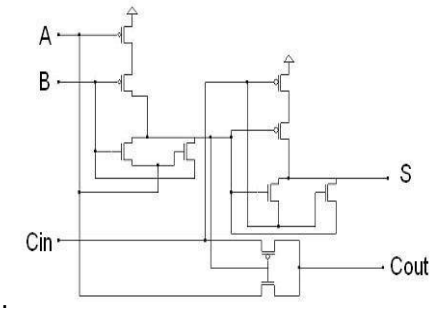

Fig-3: Block Diagram of SERF Adder [Ref 6]

In this section, The two new full adders consists of less number of transistors, because of less number of transistors results in less switching activity and area.

3. PROPOSED FinFET BASED FULL ADDER

3.1 FinFET GDI Full Adder

The Gate Diffusion Input Technique decreases both delay and power. FinFET GDI full adder consists of three input pins and two output pins. Here we are using shorted gate FinFET according to the modes of operation. The supply voltage is taken as 1.2V for FinFET GDI Adder using cadence Virtuoso tool at 180nm technology. In FinFET GDI Adder multiplexer is taken as selective input. Multiplexer looks like an inverter in order to generate the carry expression we definitely use multiplexer.

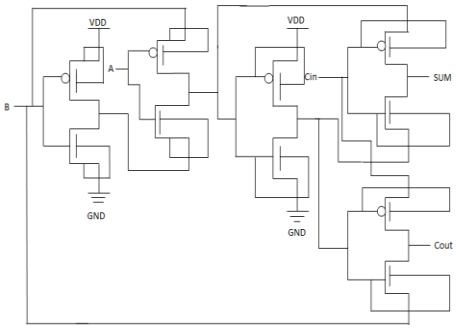

Fig-4: FinFET based GDI Full Adder [Ref 1]

FinFET GDI doesn't achieve full swing because of the threshold voltage loss. Another reason for FinFET GDI adder is taking three inputs without the use of VDD and GND. The Gate Diffusion Input Technique would possibly enrich the tool chest of VLSI Designers.

3.2 FinFET based SERF Adder

SERF design, FinFET Based full adder is implemented by using 10 transistors. Here we are using shorted gate FinFET according to the modes of operation. This circuit performs well at higher supply voltages, but the supply voltage is low this circuit fails to work.

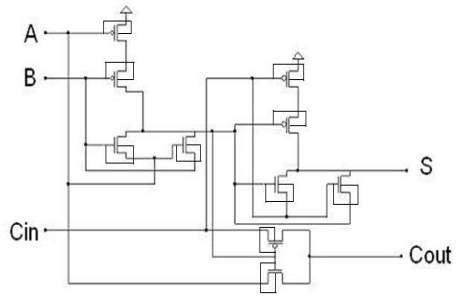

Fig-5: FinFET Based SERF Adder

The energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption. The combination of not having a direct path to ground and the re- application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design.

4. SIMULATION AND RESULTS ANALYSIS

All the FinFET based full adders simulations are done using Cadence Virtuoso in 180nm technology with supply voltage of 1.2V for GDI FinFET Full Adder and 1.5V for FinFET based SERF Adder. Power dissipation, delay and Power delay product (PDP) are measured for different design techniques.

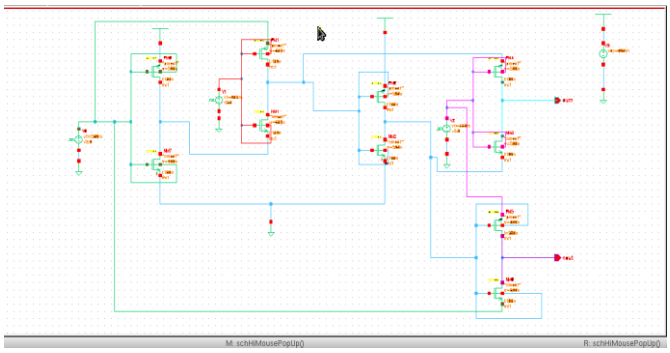

Fig-6: Schematic Diagram for FinFET GDI Full Adder

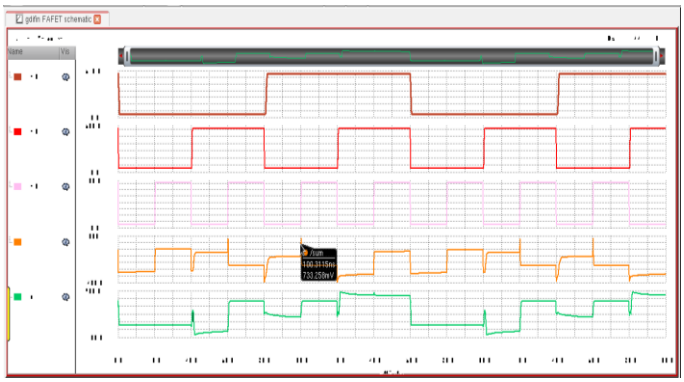

Fig-7: Transient response of Finfet based GDI Full Adder

When the input signal is ABCin="001", suppose that the circuit is operating at supply voltage VDD=1.2V and the threshold voltage for PMOS and NMOS circuit are -0.33 and 0.34 respectively. In this case, Fig.7 illustrate the problem which is even more degradation at lower supply voltages for the circuit.

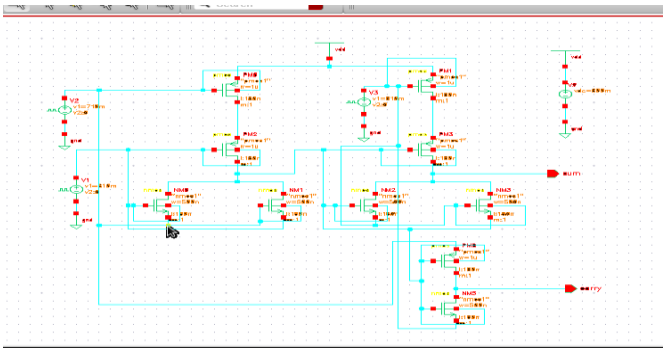

Fig-8: Schematic of Proposed FinFET Based SERF Adder

When Cin is high, Cout is charged to supply voltage, but when Cin is low, Cout discharged to threshold voltage of PMOS (Vtp) which is greater than threshold voltage of NMOS (Vtn) by using PMOS pass transistor. In this case the Sum signal is dependent on the value of Cin, for instance, if Cin is high, the Sum is equal to difference between supply voltage and threshold voltage cause a problem in sub threshold mode.

Fig-9: Transient response of Finfet based SERF Adder

This analysis shows the SERF adder is performs poorly at lower supply voltages. When ABCin="110" and "111" are applied. As seen from Fig (9), when A=1 and B=1, the E node voltage is difference between supply voltage and threshold voltage (Vdd-Vth). Now if Cin is low or logic '0' then Cout= Vdd-2Vth and the Sum signal is going to zero driven by a MOS transistor with its gate connected to Vdd-Vth. When Cin is equal to '1', Cout is connected to supply voltage (Vdd) and the SUM signal will equal to difference between supply voltage and threshold voltage. Another problem with this design is when input vector AB="01" or "10" then floating node connected to the ground.

5. COMPARISON VALUES

Table-1: Comparison Values for FinFET GDI Full Adder and Finfet SERF Adder [180nm Technology]

PARAMETERS	FinFET GDI Adder	FinFET SERF Adder
Technology	180nm	180nm
Supply Voltage	1.2 V	1.5V
Power(uW)	13.81	5.68
Delay(ps)	80.92	60.70
PDP 10^-21	1117.50	344.8367

Power consumption and delay time both are lowest for FinFET based SERF Adder. The FinFET based SERF Adder also has very low delay comparison to FinFET GDI Full Adder whereas FinFET Based SERF Adder has low Power Delay Product.

The results show that the PDP of FinFET SERF Adder is reduced to 69.14 % compared to FinFET GDI Full Adder. The Delay of FinFET SERF Adder is reduced to 24.98%compared to FinFET GDI Full Adder and the Power of FinFET SERF Adder is reduced to 58.86 % compared to FinFET GDI Full Adder.

6. CONCLUSION

In this project, it is revealed that two different Full Adder circuits are implemented by using FinFET based GDI Adder and FinFET based SERF Adder and Simulated in CADENCE VIRTUOSO TOOLS using 180nm Technology with the supply voltage of 1.2 V for FinFET GDI Full Adder and 1.5V for FinFET SERF Adder, however information available such combination using FinFET based SERF Adder. Here both the full adders consist of less number of transistors, because of less number of transistors results in less switching activity and area. A broad comparison of all the designs are showing the gradual improvement in respect of reducing power, delay and Power delay product (PDP). Based on analysis of Proposed FinFET Based Full Adder using CMOS Logic Style , it is conclude that the FinFET based SERF Adder using CMOS Logic Style helpful in digital application in respect of portable, reliable, energy efficient, consume low power and perform high speed.

REFERENCES

[1] M. Vamsi Prasad, K. Naresh Kumar, "Low Power FinFET Based Full Adder Design", International Journal of Advanced Research in Computer and Communication Engineering , Vol. 6, Issue 8, August 2017, pp.328-335.

[2] Shivani Sharma, Gaurav Soni, "Comparison analysis of FinFET based 1-bit full adder cell implemented using different logic styles at 10, 22 and 32nm", IOSR Journal of VLSI and Signal Processing, Volume 6, Issue 1, Jan.-Feb. 2016,pp.26-35.

[3] Sheenu Rana, Rajesh Mehra, "Optimized CMOS Design of Full Adder using 45nm Technology", International Journal of Computer Applications, Volume 142, No.13, May 2016.

[4] Anitesh Sharma, Ravi Tiwari, "Comparative Analysis of Ultra Low Power Based 1-bit Full Adder Using Different Nanometer Technologies", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 4, Issue 11, November 2015, pp.9307-9314.

[5] V. Dileep Chowdary, P. K. Prasad Babu, S. Ahmed Basha , M. Sreenivasulu , K. Sudhakar, "Design of Low Power CMOS Adder, Serf, Modified Serf Adder", International Journal of Innovative Science, Engineering & Technology, Vol. 2, Issue 7, July 2015,pp.1-10.

[6] S. Arif Basha & C.V. Subhaskara Reddy, "Low Power Highly Optimized Full Adder By Using Different Techniques With 10 Transistors", International Journal of Engineering Research, Volume No.3 Issue No: Special 2, March 2014, pp: 95-96 -

[7] Debika Chaudhuri, Atanu Nag, Sukanta Bose, "Low Power Full Adder Circuit Implemented In Different Logic", International Journal of Innovative Research in Science, Engineering and Technology, Volume 3, special issue 6, Feb. 2014,pp.124-129.

[8] Richa Saraswatal, Shyam Akashe and Shyam Babu, "Designing and Simulation of Full Adder Cell using FinFET Technique", Proceedings of 7th International Conference on Intelligent Systems and Control, 2013.